SONY

CXK581020AJ -20/25

131072-words x 8-bits High Speed CMOS Static RAM

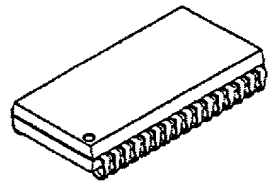
Description

The CXK581020AJ is a high speed CMOS static RAM organized as 131072-words by 8 bits.

It operates at 20ns/25ns access time from 5V single power supply.

The CXK581020AJ is suitable for use in high speed applications.

32 pin SOJ (Plastic)



Features

- Fast access time: (Access time)
  CXK581020AJ-20 20ns (Max.)
  CXK581020AJ-25 25ns (Max.)
- Low power consumption (operation)
  CXK581020AJ-20 990mW (Max.)
  CXK581020AJ-25 935mW (Max.)
- Single +5V supply: 5V±10%
- Fully static memory ··· No clock or timing strobe required
- Equal access and cycle time
- Directly TTL compatible all inputs and outputs
- Package
  CXK581020AJ 400mil 32pin SOJ Package

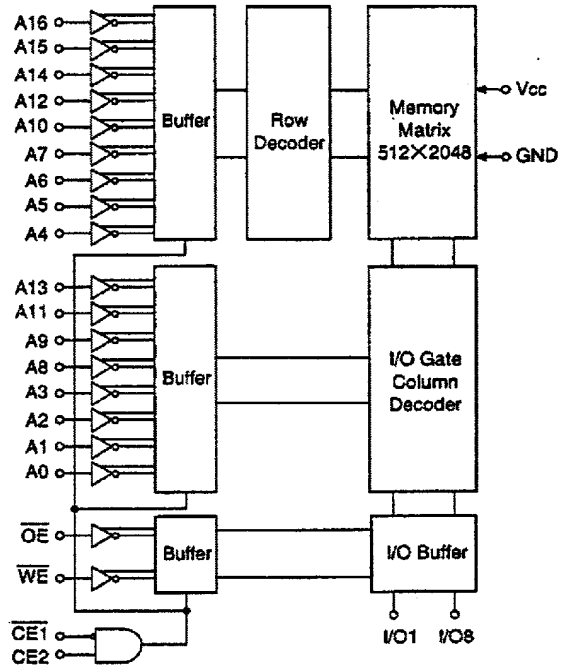
Function

131072-words x 8-bits static RAM

Structure

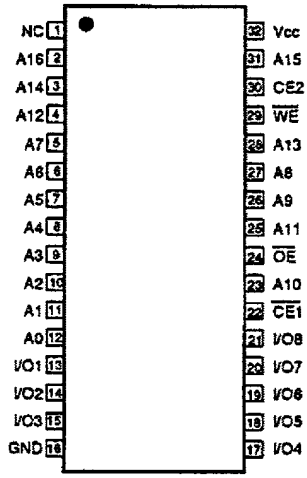
Silicon gate CMOS IC

Block Diagram



E95203—ST

Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	−0.5 to +7.0	V
Input voltage	V_{IN}	−0.5* to Vcc + 0.5	V
Input and output voltage	$V_{I/O}$	−0.5* to Vcc + 0.5	V
Allowable power dissipation	P_D	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−45 to +125	°C
Soldering temperature · time	Tsolder	235 · 10	°C · s

* Vcc, V_{IN}, $V_{I/O}$ = −3.0V Min. for pulse width less than 5ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O pin	Vcc current
H	X	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
X	L	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	Icc
L	H	L	H	Read	Data out	Icc
L	H	X	L	Write	Data in	Icc

X: "H" or "L"

DC Recommended Operating Conditions (Ta = 0 to +70°C, GND = 0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	Vcc + 0.3	V
Input low voltage	V_{IL}	−0.3*	—	0.8	V

* V_{IL} = −3.0V Min. for pulse width less than 5ns.

Electrical Characteristics

• DC characteristics (Vcc = 5V±10%, GND = 0V, Ta = 0 to +70°C)

Item	Symbol	Test conditions			Min.	Typ.*1	Max.	Unit
Input leakage current	I_{LI}	V_{IN} = GND to Vcc			−2	—	2	µA
Output leakage current	I_{LO}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to Vcc			−2	—	2	µA
Average operating current	I_{CC}	Min. cycle duty = 100%*2 I_{OUT} = 0mA	Write	20	—	—	180	mA
				25	—	—	170	
			Read	20	—	—	125	
				25	—	—	115	
Standby current	I_{SB1}	$\overline{CE1}$ ≧ Vcc − 0.2V or CE2 ≦ 0.2V, V_{IN} ≧ Vcc − 0.2V or V_{IN} ≦ 0.2V			—	—	2	mA
	I_{SB2}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, V_{IN} = V_{IH} or V_{IL}, Min. cycle		20	—	—	35	mA
				25	—	—	30	
Output high voltage	V_{OH}	I_{OH} = −4.0mA			2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0mA			—	—	0.4	V

*1 Vcc = 5V, Ta = 25°C

*2 Address is increased with binary count.

I/O Capacitance (Ta = 25°C, f = 1MHz)

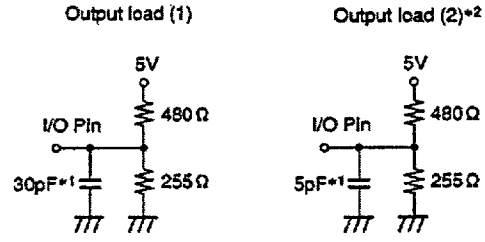
Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	—	7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	7	pF

Note) This parameter is sampled and is not 100% tested.

AC Characteristics

• AC test conditions (Vcc = 5V±10%, Ta = 0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	tr = 3ns
Input fall time	tf = 3ns
Input and output reference level	1.5V
Output load	Fig. 1



*1 This parameter includes scope and jig capacitances.

*2 For t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1.

• **Read cycle** ($\overline{WE}$ = "H")

Item	Symbol	-20		-25		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	20	—	25	—	ns
Address access time	t_{AA}	—	20	—	25	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	20	—	25	ns
Chip enable access time (CE2)	t_{CO2}	—	20	—	25	ns
Output enable to output valid	t_{OE}	—	10	—	12	ns
Output hold from address change	t_{OH}	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}*, t_{LZ2}*	5	—	5	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	2	—	2	—	ns
Chip disable to output in high Z ($\overline{CE1}$,CE2)	t_{HZ1}*, t_{HZ2}*	—	9	—	10	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	—	9	—	10	ns
Chip enable to power up time	t_{PU}	0	—	0	—	ns
Chip disable to power down time	t_{PD}	—	20	—	25	ns

* Transition is measured ±200mV from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

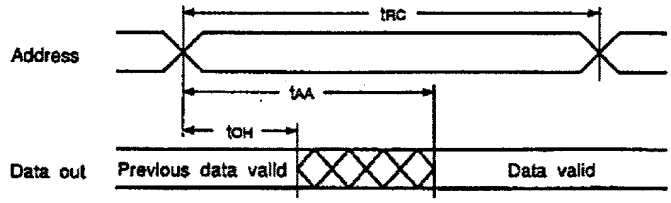
• **Write cycle**

Item	Symbol	-20		-25		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	20	—	25	—	ns
Address valid to end of write	t_{AW}	15	—	20	—	ns
Chip enable to end of write	t_{CW}	15	—	20	—	ns
Data to write time overlap	t_{DW}	10	—	12	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Write pulse width	t_{WP}	15	—	20	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	—	9	—	10	ns

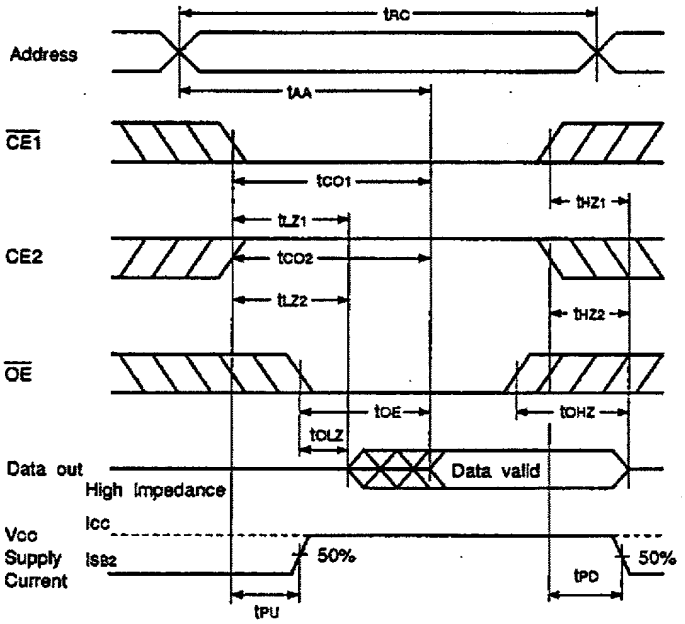
* Transition is measured ±200mV from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

Timing Waveform

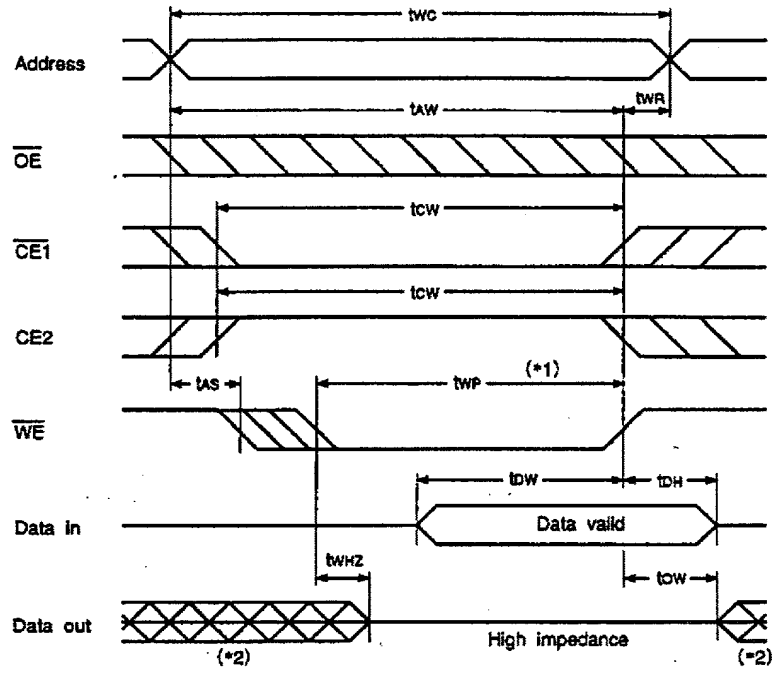
• **Read cycle (1) :** $\overline{CE1}$ = $\overline{OE}$ = V_{IL}, CE2 = V_{IH}, $\overline{WE}$ = V_{IH}



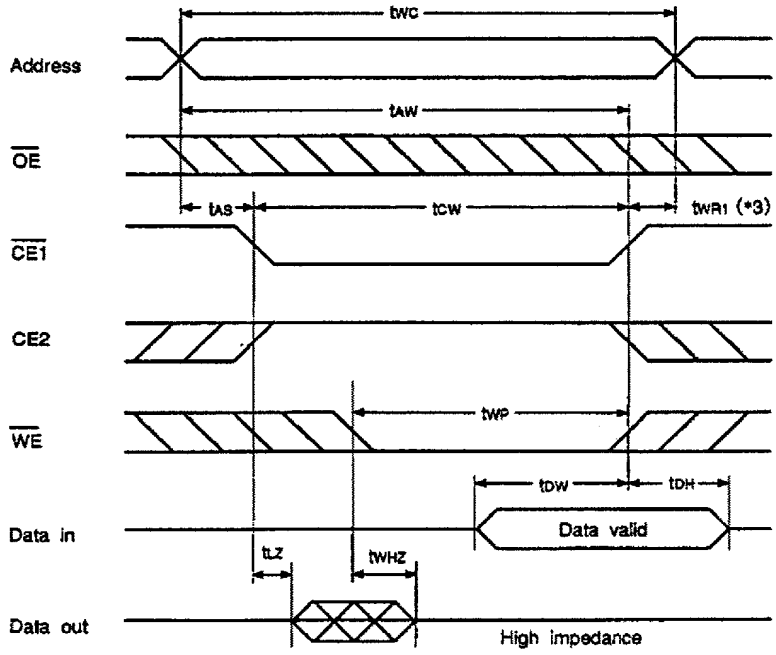
• **Read cycle (2) :** $\overline{WE}$ = V_{IH}



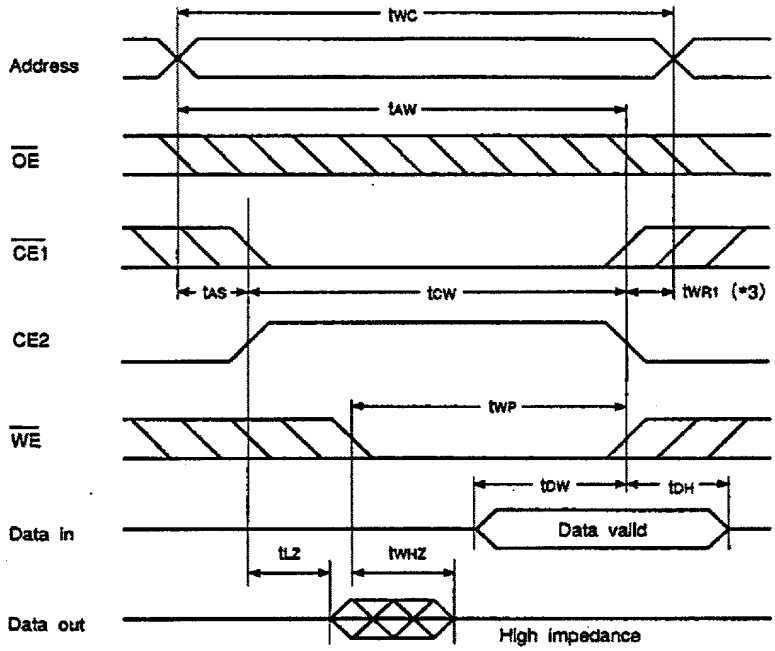
• **Write cycle (1) : $\overline{WE}$ control**



• **Write cycle (2) : $\overline{CE1}$ control**



• **Write cycle (3)** : CE2 control



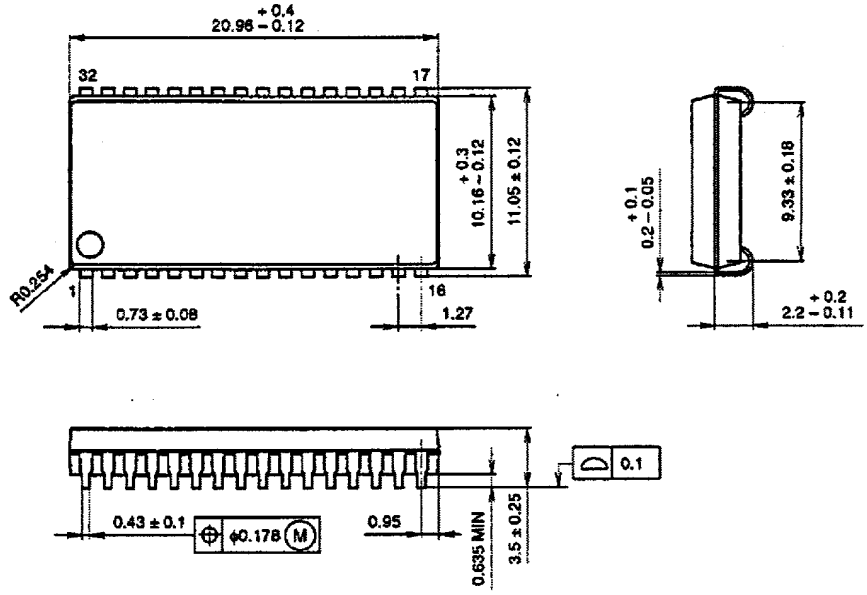
*1 Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.

*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

*3 t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Package Outline Unit : mm

32PIN SOJ (PLASTIC) 400mil



SONY CODE	SOJ-32P-01
EIAJ CODE	*SOJ032-P-0400-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 / COPPER ALLOY
PACKAGE WEIGHT	1.3g