IIT3204 MPPex

Extended MPEG Playback Processor and System Controller

OVERVIEW

The IIT3204 Extended Multimedia Playback Processor (MPPex) is a single-chip MPEG1 Video, Audio, System decoder designed for a wide range of digital video playback applications including Video CD, Karaoke players and PC MPEG playback cards. When combined with memory and video/audio DACs, it completes a highly integrated MPEG1 decoder system. This high level of integration results in an overall system cost significantly lower then previously achievable.

The MPPex chip is capable of decoding MPEG1 system layer bitstreams at up to 9 Mbits/sec at SIF resolution with a picture rate of 30 frames/sec. Two channels of MPEG layer 1 or layer 2 audio are simultaneously decoded. For embedded applications, the MPPex's internal RISC microprocessor can be used in place of a microcontroller to provide all system control and user features. On-chip, multi-tap, filters provide arbitrary scaling, video standards conversion and video post-processing.

The MPPex is based on IIT's programmable Multimedia Processor Architecture (MPA) technology and is an extension of the IIT MPP device. The MPPex maintains pin compatibility with the original MPP, but has additional features for automatic external boot ROM width detection, additional auxiliary control pins, On Screen Display (OSD), glueless 24 bit RGB video interface and an integrated audio DAC interface to reduce audio glue logic.

FEATURES

- Single-chip MPEG1 system/video/audio decoder
- Based on IIT's Multimedia Processor Architecture
- No external microcontroller required
- On-chip arbitrary video scaling
- VideoCD, CDi, Karaoke, CD-XA Compatible
- STC interpretation and A/V clock PLL control
- Includes CD Block decoder functions
- Direct connect to CD-ROM, audio/video DACs
- Drivers for OM1, MCI, VideoCD, CDi
- Video Interlacing hardware
- Bitstream error suppression/recovery
- PCI interface chip available (IIT3501 VPIC)
- Low Power Consumption
- Pin Compatible with IIT MPP
- On screen display (OSD)

Figure 1 shows a block diagram of a typical embedded decoder system. The MPEG system bitstream from a CD-Video disk is passed to the MPPex through the TDM (Time Division Multiplexed) serial bus or 16 bit parallel host interface. The MPPex parses the system layer and demuxes the audio and video channels. Audio is decoded and passed through the audio serial bus to an audio DAC and then to the speakers. Video is decoded and output as YUV or RGB digital pixels to an NTSC or PAL video DAC/Encoder and then to the screen. System control and housekeeping functions (keypad, remote control) are also provided by the MPPex.

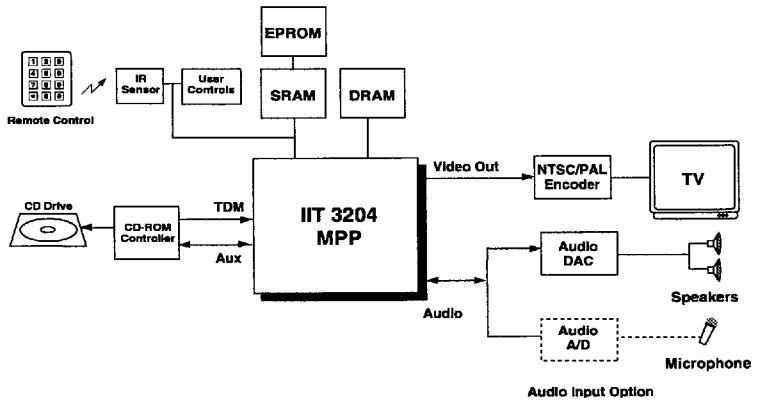

Figure 1. MPPex Stand-alone System

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MPEG is the Moving Picture Experts Group of the ISO/IEC. References to "MPEG" in this document refer to the ISO/IEC JTC1 SC29 committee draft ISO 11172 dated 9th Jan 1992.

H.261 refers to the International Standard described in recommendation H.261 of the CCITT Working Party 15-1.

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Introduction

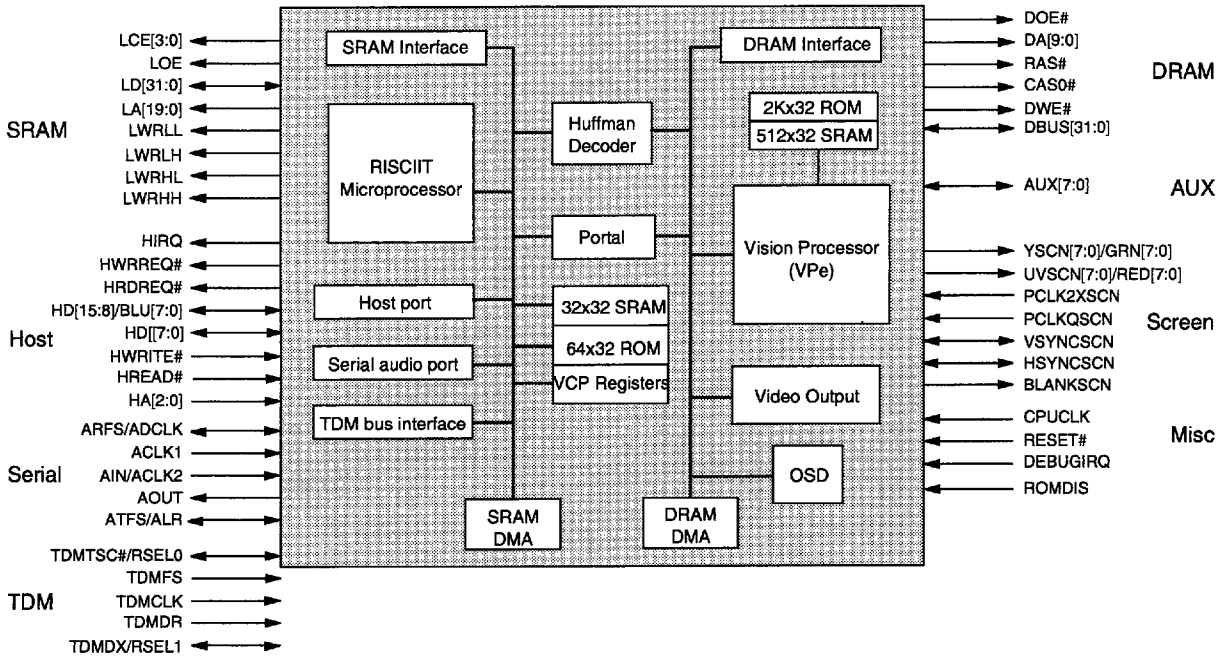

Figure 2. MPPex Block Diagram

INTRODUCTION

Figure 2 shows the internal architecture of the MPPex. In the left hand side of the diagram the SRAM bus and RISC section deal with compressed data types and command and control. The right hand side or DRAM DMA side handles uncompressed and intermediate data. The Video Out bus allows uncompressed video out of the chip. The Host Bus, TDM Bus and Audio Interface transfer low datarate compressed information or audio/ network data.

Passage of data through the system is controlled by the two DMA controllers (SRAM and DRAM) associated with the internal buses. These run under the supervision of the RISC processor.

The architecture of the MPPex is a subset of that of the VCP chip; it provides the same flexible video processing capabilities and general data transfer options between DRAM and SRAM. The VCP's H.320 specific BCH and H.221 functions are eliminated, as is the video capture port. The following sections describe the MPPex functional blocks in more detail.

RISC MICROCONTROLLER

The MPPex RISC (RISCiit) is a faster, enhanced version of the Stanford MIPS-X microprocessor. As in the original MIPS-X, it is a 32-bit instruction, 32-bit data pipelined RISC microprocessor. In addition to being clocked at least four times faster than the MIPS-X, the RISCiit adds a number of instructions which speed up byte and word accesses and has improved interrupt processing capabilities. The RISCiit does not have an instruction cache; rather it has a full 32-bit interface to external SRAM which improves code access time by a factor of two. The MPPex does not require an external boot ROM for power-up initialization; the RISCiit can boot from either on-chip ROM or through the external RAM interface. The RISCiit also has a small amount of on-chip SRAM in which it can keep commonly used data; access to this memory is overlapped with the next instruction fetch and has no cost. The RISCiit maintains the pipelined architecture of the MIPS-X and is programmed using an enhanced, optimizing 'C' language compiler.

SRAM INTERFACE

The SRAM interface controls all accesses to the MPPex SRAM; the primary use of this SRAM is for program, stack and data storage for the RISC. It is also used to implement buffer storage for video rate buffering. It provides a glue-less interface to SRAM chips and also provides four address decodes and byte enables to allow memory mapped I/O devices to be controlled by the RISC. These allow the RISC to supervise external programmable devices and allow the MPPex to act as the System Controller in embedded systems. The interface is 32-bits wide; 16-bit and 8-bit devices are also supported.

The MPPex is also able to boot directly from an external ROM or EPROM. To tell the MPPex to boot from external ROM the ROMDIS pin should be held high during the reset cycle. Normally, the MPPex will expect to boot from an 8 bit wide EPROM, however, 16 and 32 bit wide EPROMs can be used by clamping RSEL[1:0] at boot time.

SRAM DMA

The SRAM DMA controller is a ten channel DMA controller which moves data between the SRAM and the following sections:

- TDM
- Audio
- Portal
- Huffman decoder
- Host

Each of these sections has two channels, one for reading and the other for writing. Each channel has a fixed priority and operates under the supervision of the RISC. This architecture allows the external SRAM to act as FIFO storage for the numerous buffering operations required and eliminates on-chip FIFOs. The internal SRAM data bus is 32-bits wide, although some of the devices (TDM, Audio, Huffman, Host) are 16 bits or 8 bits (Host debug).

COMMUNICATION RESOURCES

The MPPex has three communication resources which are linked to the SRAM via the DMA channels. Each resource can be used for general purpose communication between the MPPex and other devices in the system and is under software control. In most IIT systems, the TDM port is connected to an WAN/LAN chipset and the audio serial port is connected to audio DACs or to a DSP for advanced audio processing. The Host port is connected to the source of command and control information and of any high or low speed data.

TDM INTERFACE

The TDM (Time Division Multiplexed) interface implements a high-speed, bidirectional serial bus which is intended to transfer the encoded bitstream to the network interface. It can implement a number of high-speed serial protocols including concentration highway interface (CHI), GCI, K2, SLD, MVIP and IOM2 formats. The TDM port can also act as a general purpose 16Mbit/sec serial link when not constrained by the TDM protocols, for example I2S serial interface for direct connection to a CD-ROM drive.

HOST INTERFACE

The Host Interface provides a general purpose parallel interface to the MPPex. It contains three ports, a debug port, a command port and a DMA port. It is used for communication between a Host processor and the MPPex, and can also be used to transfer the following:

- Bitstream input
- User data in/out

The Host Interface has three registers which control the operation of the interrupts and flags. Flags are used to indicate the MPPex's readiness to accept or supply data over the host port DMA channel. The interrupts may be used for exception indication from RISC to Host or from Host to RISC. The interrupts are maskable.

In 24 bit RGB video output mode, the 8 MSBs of the Host port are used for video data. In this mode the 16 bit DMA port is disabled and cannot be used for data transfer.

AUDIO INTERFACE

The Audio interface is a bidirectional serial port designed to connect to a DAC serial port for transfer of PCM audio data. Audio decompression is handled inside the MPPex. This close coupling allows accurate audio/video synchronization.

An additional audio mode has been added to the MPPex. This mode can be selected by a register inside the MPPex and allows direct connection to audio DACs without glue logic. This is done by changing AUDTFS (transmit frame sync) to ALR (audio left/right) and AUDRFS (receive frame sync) to ADCLK (audio DAC clock) outputs.

PORTAL

The Portal connects the DRAM and SRAM buses. It provides a 32-bit bidirectional gateway between the buses. Most transfers will be between functional blocks on the same bus (e.g. SRAM and Host Interface, DRAM and Video interface). However in some instances it is desirable to transfer between buses and the Portal provides the mechanism for doing this.

HUFFMAN DECODER

The Huffman decoder is a high-speed engine which decodes using MPEG Huffman tables. The decode tables are programmable and can be changed by the application. Zero-run length/amplitude (RLA) tokens are transferred on the DRAM bus to the Vision Processor core. The Huffman coded data is transferred by an SRAM DMA channel.

DRAM DMA CONTROLLER

The DRAM DMA controller has multiple channels which transfer 32-bit data between the DRAM and the following:

- Video interface
- Huffman decoder
- Portal
- Vision Processor
- DRAM Refresh

The Video interface, VPe and Huffman sections all contain memory which allows the DMA controller to transfer data in DRAM page mode. One DMA channel provides DRAM refresh.

EMBEDDED VISION PROCESSOR (VPe)

The Embedded Vision Processor (VPe) implements a super-set of the functions of the IIT Vision Processor (VP) chip. In addition to running at higher clock speeds, it includes a number of architectural improvements which provide additional performance and code compaction over the VP chip.

The VPe core implements a programmable video signal processor which executes the decompression operations required by the MPEG, JPEG and H.261 standards as well as some proprietary algorithms. Some of the improvements allow the VPe core to perform video pre- and post-processing functions in software. This provides much more flexible video processing than is offered by the circuits in the Vision Controller chip and enables the MPPex to perform arbitrary filtering and scaling of outgoing video.

The microcode program for the VPe is stored in 2K words of on-chip ROM; in addition 0.5K word on-chip SRAM is provided to allow new microcode subroutines to be downloaded. Most VPe instructions are 32-bits wide, in contrast to the 64 bit microcode word of the VP chips (vers. 2-4).

DRAM INTERFACE

The DRAM interface provides glue-less connection to DRAM memory chips. It supports from 512K bytes to 4 Megabytes of DRAM, implemented using x1, x4 or x16 chips. The DRAM interface is also configurable in depth to allow addressing of 16Mbit and EDO DRAMS. A wide variety of DRAM speed grades may be used.

The DRAM interface is 32-bits wide and, at high MPPex clock speeds, provides sufficient bandwidth to decode MPEG and display 1024x768 resolution images at 75 frames per second. For less demanding applications such as MPEG1 SIF resolution decode the bus can operate in a 16-bit mode. In this mode a single 256k x 16 DRAM chip can be used. The single DRAM, 16 bit, mode is able to display up to 800x600 video at 75Hz refreshate.

VIDEO OUTPUT

The Video Output section displays video frames stored in the DRAM. It also provides hardware post-processing functions which can be used in conjunction with software running on the VPe. In particular it contains storage to buffer outgoing video, color conversion circuitry, multi-tap decimation and interpolation filters and a Temporal filter. The decimation and interpolation filters allow conversion between SIF, CIF, QCIF or any commonly used format and display formats for computer and TV video

encoder chips such as CCIR601 and 640x480 VGA. The Video Output contains a programmable CRT controller which handles interlaced and progressive scanning. The CRT controller can be programmed to generate video syncs and blanks or can be genlocked to an external video source.

The video output section also includes dedicated on screen display (OSD) hardware. The OSD can have 2, 4 or 8 bits per pixel palletized colors including transparent and can take up full or partial screen area. It is muxed into the output video stream after scaling and color space conversion has been completed. The OSD bitmap is stored in the reference DRAM.

CLOCK GENERATORS

The MPPex relies on 4 external clocks for timing and synchronization between the I/O resources and the main processing and control elements. The external clocks are: ACLK to provide timing for the audio serial line, TDMCLK to provide timing for the TDM/Serial data port, PCLKSCN for video timing and CPUCLK for main processor timing.

Functional Description

VIDEO BUS

The MPPex video bus transfers digital video pixels out of the chip. In stand-alone applications the video bus will be connected to a monitor or LCD panel. In workstation applications the output bus will feed an overlay circuit so that the output video appears in a window of the Graphical User Interface.

The video bus has 16 data pins which transfer luminance and chrominance (YUV) pixels in CCIR601 pixel format (4:2:2). In this format, there are half as many chrominance (U or V) pixels per line as luminance (Y) pixels; there are as many chrominance lines as luminance. The video bus also has a mode for outputting 24-bit or 16-bit RGB pixels.

24 bit RGB mode makes use of the 8 most significant bits of the host port for BLU[7:0] databits. These pins take on the same timing as the RED and GRN pins. In 16 bit RGB mode the MPPex uses RGB565, red is allocated the 5 MSBs of the YSCN bus, G bridges between the LSBs of YSCN and the MSBs of UVSCN and blue takes up the LSBs of the UVSCN bus.

CRT CONTROLLER

The video bus is controlled by a pixel clock and horizontal and vertical synchronization (sync) signals. Pixels are clocked into and out of the MPPex by the pixel clock; the sync signals determine when the active video data is transferred. The timing of the active video and sync signals is determined by CRT Controller inside the MPPex. The output CRTC timing can be internally generated, or slaved to some other video sync source.

VIDEO PROCESSING

The MPPex contains circuitry to post-process video. This circuitry provides color conversion, scaling and filtering functions through a combination of special hardware and software. In order to match internal clock rates with external pixel clock rates the MPPex has internal line buffers which allow the display of MPEG SIF video at resolutions up to 1024x768 in either 4:2:2 YUV or fully sampled RGB color space.

The MPPex horizontal and vertical scaling may be set to any size up to 1024x768, the scaling ratio can be modified while MPEG video is being processed. Horizontal up-sampling and filtering is done with a programable, 5 phase, 7 tap filterbank for accurate non-integer interpolations. Vertical scaling is achieved by repeating the previous line in proportion to the scaling ratio.

The MPPex is also equipped with an output video interpolator, which enables flicker free display of SIF pictures on a normal, interlaced TV set.

VIDEO POST-PROCESSING

Figure 3 shows the video post-processing functional blocks. The first three processing steps are per-

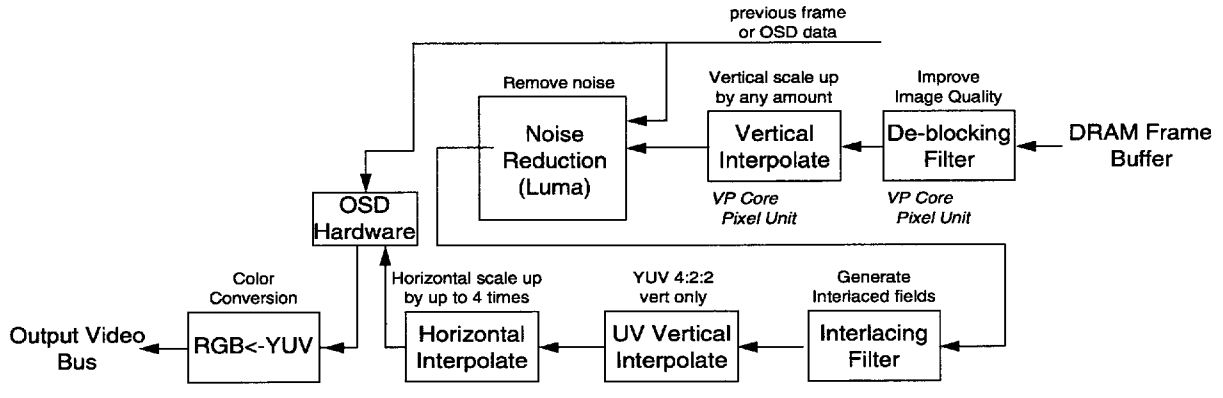

Figure 3. Video Post-processing

formed by the VPe core. A de-blocking filter can be applied to decoded images to improve the picture quality. This filter reduces blocking artifacts which can be visible at low bitrates. The VPe core can then interpolate any number lines to scale up the image; this can be used to convert from QCIF to CIF, or from CIF to NTSC or to allow the decoded image to fit in an arbitrary-sized window in a Graphical User Interface (GUI).

The scaled images are passed to the Noise Reduction stage. The Noise Reduction works by killing so called "mosquitos", or high frequency, low intensity, ringing around sharp, moving, edges.

The next stage in the processing is an interlacing filter which generates even and odd fields from decoded frames for applications which use TV screens. This improves both the spatial and temporal appearance of the decoded images on interlaced displays. Following the interlacing filter is an interpolation section which uses bi-linear interpolation to increase the resolution of the chrominance components by a factor of 2 in the vertical dimension. This interpolation section converts from the MPEG chrominance sub-sampling to that used by CCIR 601. The resulting YUV pixels can then be passed through a seven-tap horizontal interpolation filter which increases the horizontal resolution of the image by up to four times.

The horizontal filter can automatically choose between 5 sets of filter coefficients based on the fractional component of the new position of the pixel in the video data stream. The filter coefficients are 8 bits wide. The filter length is selectable 1, 3, 5 or 7 taps. The relationship between the PCLK2XSCN and CPUCLK is shown in table 2.

Taps	Restrictions
1	Pixel rate < (2xCPUCLK)/2
3	Pixel rate < (2xCPUCLK)/2
5	Pixel rate < (2xCPUCLK)/3
7	Pixel rate < (2xCPUCLK)/4

Table 2. PCLK2XSCN to CPUCLK Relationship

When used in conjunction with the software vertical interpolation, this allows the decoded image to fit in an arbitrary-sized window in a Graphical User Interface. Finally the YUV pixel output can optionally be converted to RGB (red, green, blue) color space for non-TV output applications. The RGB format can be either 16-bit or 24-bits multiplexed onto the 16-bit Video Out bus or 24 bit RGB making use of the host port MSBs for the blue channel.

VIDEO TIMING

Figure 4 shows the timing of HSYNC and VSYNC on the Video bus when using the doubled (PCLK2XSCN) clock and clock qualifier

(PCLKQSCN).

The Video Bus can be clocked either by double pixel clock and clock qualifier or by a single pixel clock. The double clock would typically be used for TV displays, the single for computer displays. Figure 6 shows the Video Bus Timing using a double pixel clock. Figure 5 shows the Video In/Out bus timing using a single pixel clock. PCLKQSCN is ignored in 1x clock mode.

The Video Bus maximum double and single pixel clock is 33 MHz or CPUCLK, whichever is lower.

The timing of the syncs, blanking and odd/even field indication are shown in Figures 6, 7 and 8. The output video field indication is done by modifying the relative positions of VSYNCSCN and HSYNCSCN. At the start of an even field the horizontal and vertical sync pulses will start on the same clock edge, in odd fields the horizontal sync pulse will be delayed by one clock cycle. The sense of both horizontal and vertical syncs is programmable.

Table 3 shows the detailed AC timing for the output bus.

ON SCREEN DISPLAY

The MPPex has on screen display capability that allows the user to overlay or blend a bit mapped graphic with the displayed video.

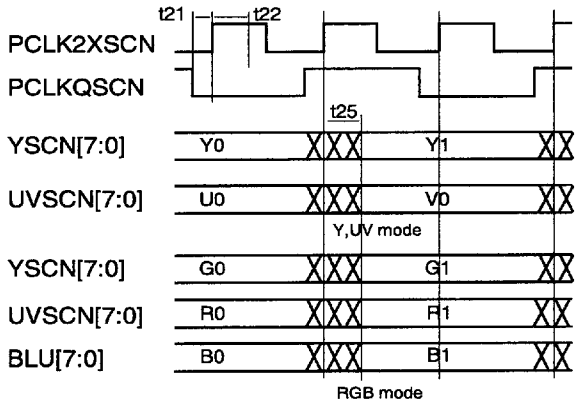

Figure 4. 2x Clock Video Out Bus Timing

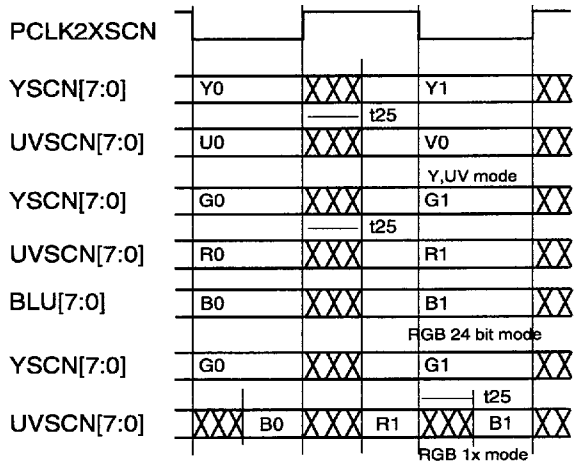

Figure 5. 1x Clock Video Out Bus Timing

Symbol	Description	30MHz		33MHz		40MHz	
		Min	Max	Min	Max	Min	Max
t6	PCLK2XSCN period	33ns	-	30ns	-	25ns	-
t21	PCLKQSCN setup time to PCLK2XSCN	6ns	-	6ns	-	4ns	-
t22	PCLKQSCN hold time to PCLK2XSCN	2ns	-	2ns	-	2ns	-
t23	Syncs setup time to PCLK2XSCN	6ns	-	6ns	-	4ns	-
t24	Syncs hold time to PCLK2XSCN	2ns	-	2ns	-	2ns	-
t25	Video data and syncs output delay time to PCLK2XSCN	4ns	12ns	4ns	12ns	3ns	9ns

Table 3. Output Bus Timing

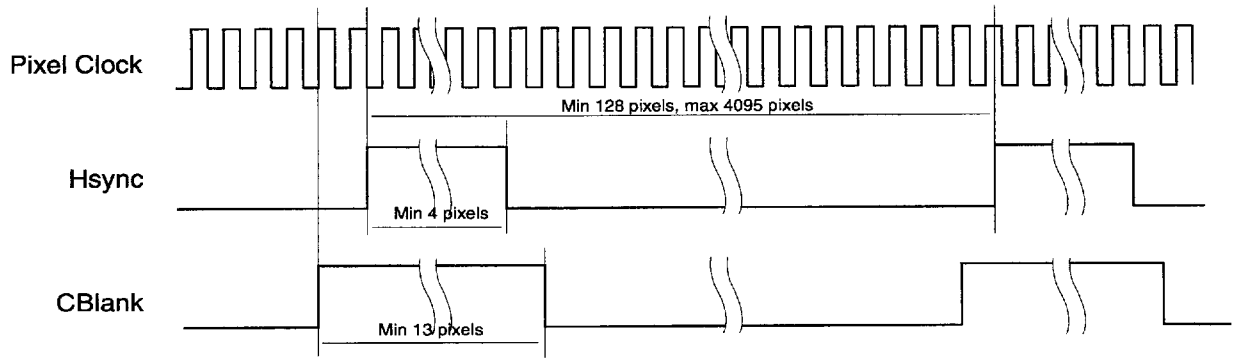

Figure 6. Horizontal Video Timing

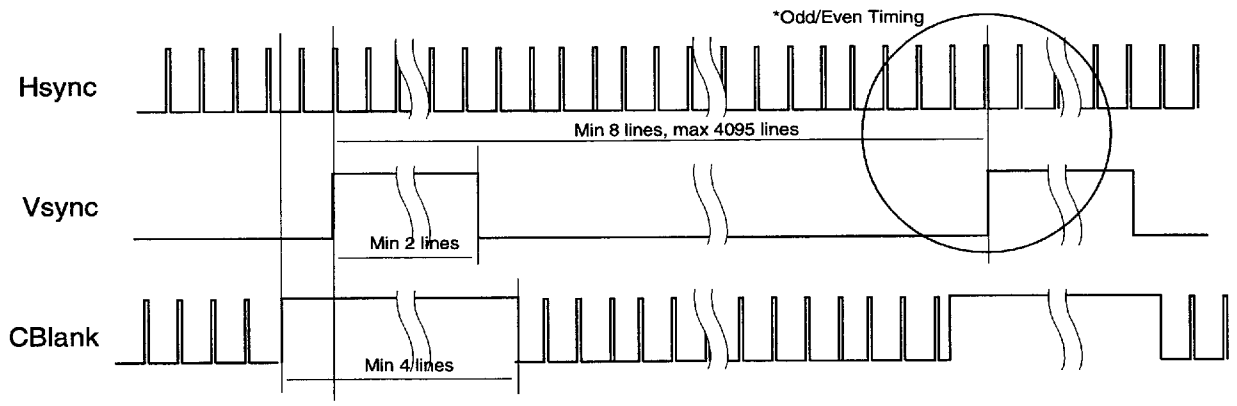

Figure 7. Vertical Video Timing

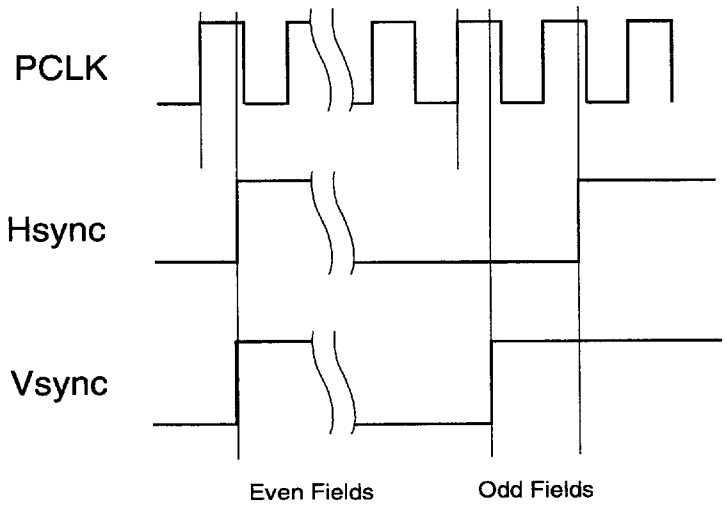

Figure 8. Odd/Even Video Output Timing

The OSD values stored in memory can be 2, 4 or 8 bits per pixel. These values are indexes into a LUT that can be programmed with 8 bits of color information 5 bits of brightness and 8 blending values.

The OSD channel has three operating modes and a bypass mode. Mode 1 uses 2 bits per pixel for 3 colors and transparent. Mode 2 uses 4 bits per pixel but is otherwise the same as Mode 1.

Mode 3 allows 8 bits per pixel. The most significant 4 bits are used as indices to the LUT, the least significant 4 bits select various blending values to allow the blend to vary from pixel to pixel.

The OSD channel makes use of the temporal noise reduction channel for the decoder. This means that, while the OSD is operating, temporal noise reduction is off.

DRAM BUFFER

The DRAM buffer is used for storing uncompressed images, reference frames and intermediate data. When the MPPex is decoding, the images to be displayed are held in the DRAM.

All DRAM control is provided by the MPPex DRAM bus. It can interface to DRAM chips organized x16, x4 and x1 bit wide. Figure 9 shows some example configurations. The DRAM interface is 32-bits wide and, at high MPPex clock speeds, provides sufficient bandwidth to decode and display CCIR601 resolution images at 60 frames per second. For less demanding applications such as MPEG1 SIF resolution decode or H.261 QCIF codec, the bus can operate in a 16-bit mode. In this mode a single 256k x 16 DRAM chip can be used; the most significant and least significant 16-bits of the DBUS[31:0] should be connected (i.e. bit 31 to bit 15, bit 30 to bit 14, etc.).

The DRAM interface is programmable to enable support of DRAMs with a variety of page mode cycle times, RAS to CAS delay times and RAS precharge times. Table 4 and figures 10 and 11 show the

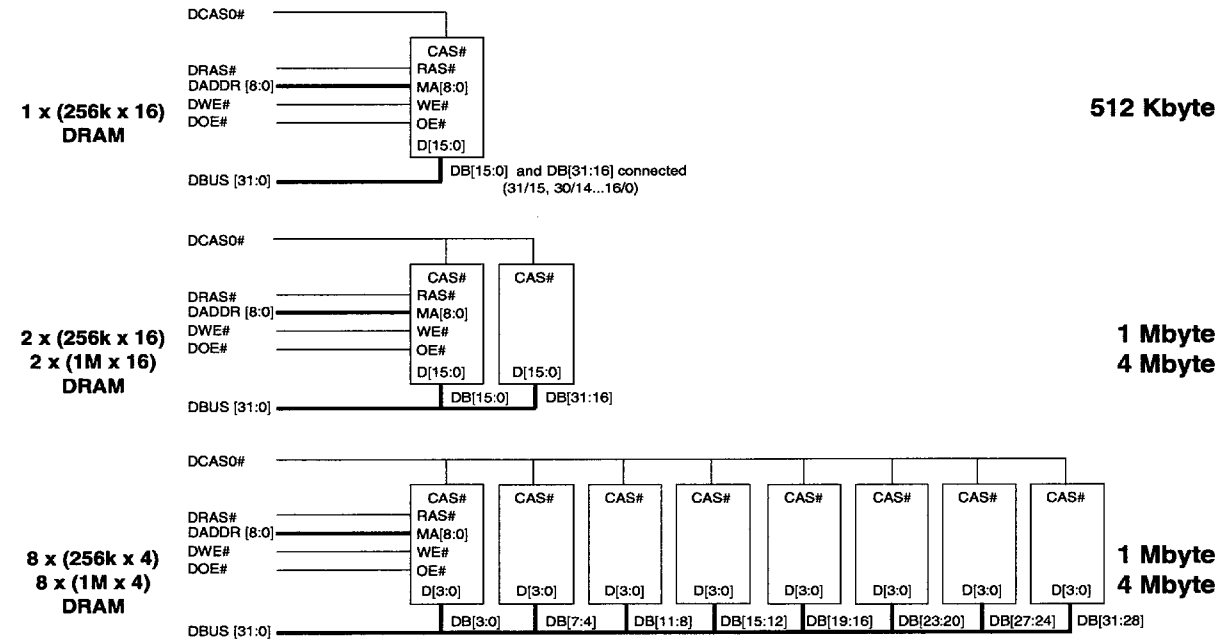

Figure 9. DRAM Configurations

DRAM output signal timing in terms of T states. The output signals may also be skewed in relation to each other and this should be taken into account when choosing DRAM for any application. The DRAM output signal skews are listed in table 5.

The MPPex DRAM controller uses page mode accesses whenever possible and takes care of DRAM refresh. The MPPex uses RAS only refresh mode, the refresh period is programmable.

The page mode cycle time of DRAMs varies from one manufacturer to another. A typical 70ns DRAM has a page mode cycle time of 40ns. For a MPPex with a 33MHz CPUCLK a 3T cycle takes 45ns which will meet the specifications of the 70ns DRAM.

When operating with 2T page mode cycle times with a 33MHz MPPex, the burst transfer rate of the DRAM interface is 128 Mbytes/sec.

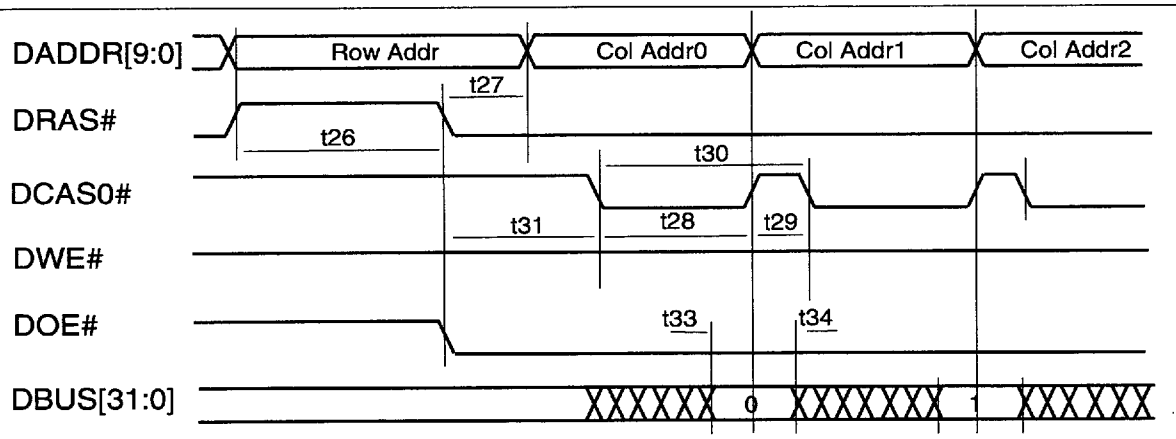

Figure 10. DRAM Read Timing

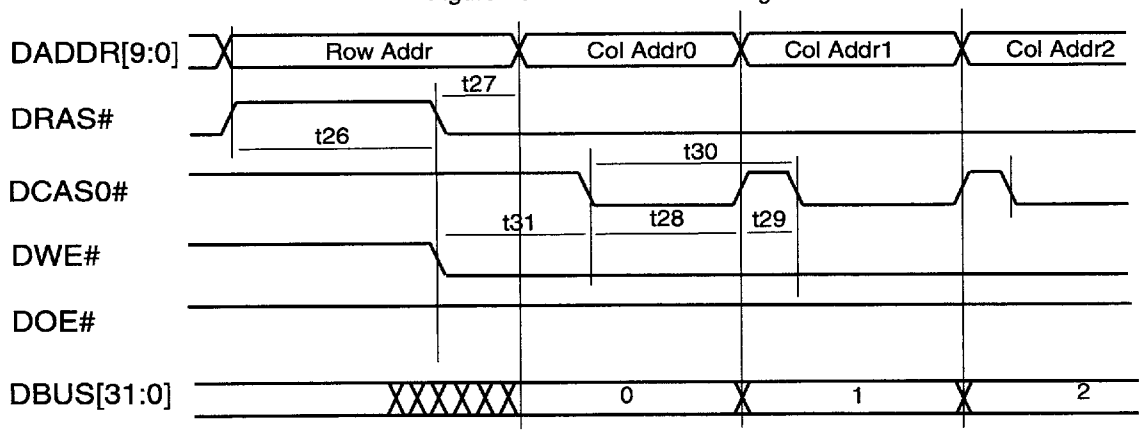

Figure 11. DRAM Write Timing

Symbol	Description	Programmable	
		Min	Max
t26	RAS precharge time	3T	5T
t27	Row address hold time	1T	3T
t28	CAS pulse width low	1T	2T
t29	CAS pulse width high	1T	2T
t30	Fast Page Mode access time	2T	4T
t31	RAS to CAS delay time	2T	4T
	* 1T = Internal PLL clock cycle		

Table 5. DRAM Interface Signal Logical Timing

Symbol	Description	30MHz		33MHz		40MHz	
		Min	Max	Min	Max	Min	Max
t32	DRAM port output signal skew	0	3ns	0	3ns	0	3ns
t33	Read cycle data setup time to CAS rising edge	5ns	-	3ns	-	3ns	-
t34	Read cycle data hold time to CAS rising edge	0	-	0	-	0	-

Table 4. DRAM Interface Signal Skew Timing

SRAM INTERFACE

The SRAM interface controls access to external SRAM which is used for RISC code, stack and data as well as buffer storage for the TDM, Audio, and Host sections. The SRAM bus supports four independent address spaces, each having programmable bus width and wait-states. The interface can thus support not only SRAM but also EPROM and memory mapped I/O ports for stand-alone applications.

A new feature available in MPPex is the RISCiit-Stall mechanism. This allows external logic to stop the RISCiit by forcing the AUX7 input line to a low value. The RISCiit will stall on the cycle following the rising edge of CPUCLK while AUX7 is low and will start again once AUX7 is taken high.

The timing of SRAM accesses is shown in Figures 12 and 13. From 0 to 32 wait states can be inserted into each cycle, each wait state being one MPPex CLOCK cycle long. All accesses by the SRAM DMA controller which services the TDM, Audio, and Host sections will have a minimum of one wait state inserted by the Interface. RISC accesses can be zero wait state. The SRAMs used with the MPPex running at 0 wait state, 33MHz, must support a write pulse width less than or equal to 15ns.

It is possible, when switching from a low speed bank to a high speed bank, for the turn off delay of the low speed bank to overlap the first access of the high speed bank. To prevent data corruption t39 (Bank Select Delay Time) is programmable for each bank from 0 to 3T states. See table 7 for details.

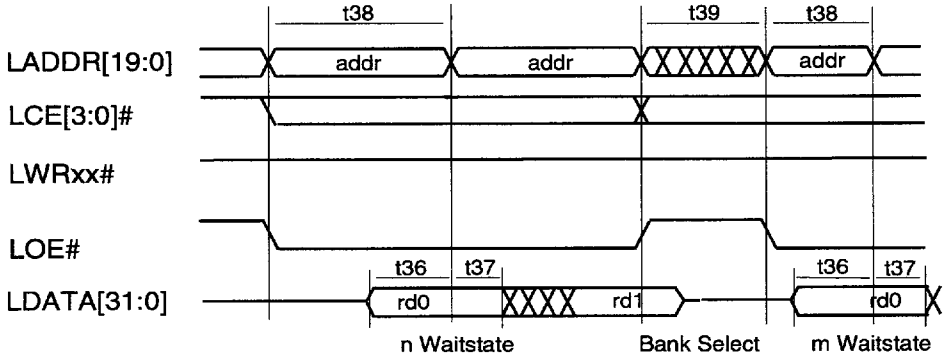

Figure 12. SRAM Read Timing

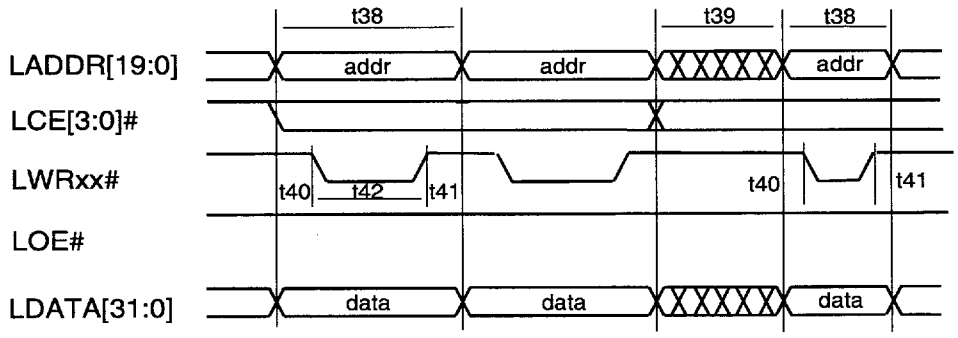

Figure 13. SRAM Write Timing

The signals for the SRAM bus are generated from the internal RISC clock and are timed in integer multiples of CPUCLK cycles, except for the write strobe, which is delayed by one quarter cycle from the address setup and advanced one quarter cycle from the start of the next access cycle.

The SRAM port signal skew may vary with MPPex speed grade, see table 6 for details.

Symbol	Description	Programmable	
		Min	Max
t38	SRAM access time	1T	33T
t39	Bank Select delay time	0T	3T
t40	Address setup time to write strobe	0.25T	0.25T
t41	Address hold time to write strobe	0.25T	0.25T
t42	Write strobe pulse width low	0.5T	32.5T
* 1T = CPUCLK pin cycle, Each Wait-state = 1T			

Table 7. SRAM Port Output Signal Logical Timing

Symbol	Description	30MHz		33MHz		40MHz	
		Min	Max	Min	Max	Min	Max
t35	SRAM port output signal skew	0	3ns	0	3ns	0	2ns
t36	Read cycle data setup time to data latch	6ns	-	6ns	-	4ns	-
t37	Read cycle data hold time to data latch	2ns	-	2ns	-	2ns	-

Table 6. SRAM Port Output Signal Skew Timing

TDM BUS

The TDM port implements a five-wire serial bus which provides an easy connection between the MPPex and available communications chips. The TDM bus is a Time Division Multiplexed bus which multiplexes data on up to 64 channels. Each channel is allocated a different time slot on the bus, and the MPPex can be set to send and/receive data on any combination of different time slots. Data is assumed to be ordered by time slot (i.e. if time slots 6, 8 and 17 are used, the first byte DMA'ed to memory is the byte in time slot 6, followed by 8 and 17 in order. Re-ordering must be done in software).

The interface consists of a Frame Sync (TDMFS), data transmit and receive signals (TDMDX, TDMDR), external buffer enable (TDMTSC#) and a clock (TDMCLK). The Frame sync and Clock signals are inputs to the MPPex, so the timing of the data transfer is externally controlled. The TDM port can support a number of different timings on the TDM bus. These possibilities are described in Table 8. A timing diagram for a particular configuration is shown in Figure 14.

The TDM bus can transfer data at a maximum rate of 16 Mbits/s. A more typical configuration would support up to 4.096Mbits/s with a TDMFS fre-

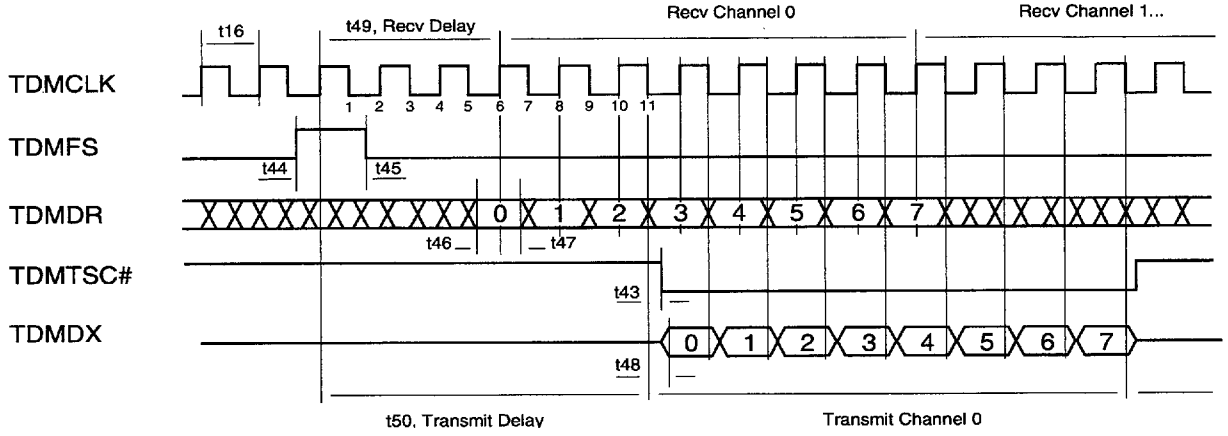

Figure 14. TDM Bus Timing

Symbol	Description
TDMCTL.sel2x	Serial clock 2x or 1x select
TDMCTL.clkphase	2x Serial clock phase to rising edge of TDMFS
TDMCTL.fe	Selects edge of serial clock to use when sampling TDMFS
TDMCTL.rce	Selects edge of serial clock to use when sampling TDMDR
TDMCTL.xce	Selects edge of serial clock to use when driving TDMDX
TDMCTL.xmitEndian	Selects little or big endian data type transmit
TDMCTL.rcvEndian	Selects little or big endian data type receive

Table 8. TDM Bus Programmability

quency of 8KHz. The TDM port hardware is flexible enough to interface to a wide range of communications chips for ISDN, PABX, LAN and WAN connectivity. In particular it will interface directly to chips which support the Concentration Highway Interface (CHI), ISDN Oriented Modular Revision 2 (IOM-2) interface and Multi-Vendor Integration Protocol (MVIP).

The TDM bus programmability includes independent receive, transmit and frame sync clock edge selection and independent receive and transmit data offsets. This is illustrated in table 10.

Symbol	Description	Programmable	
		Min	Max
t49	TDM Receive delay to TDMFS	0	8T
t50	TDM transmit delay to TDMFS	0	8T
		* 1T = TDMCLK cycle	

Table 10. TDM Delay Timing

Symbol	Description	30MHz		33MHz		40MHz	
		Min	Max	Min	Max	Min	Max
t16	TDMCLK period	62.5ns	-	62.5ns	-	62.5ns	-
t43	TDMTSC# control output delay to TDMCLK	0	2	0	2	0	2
t44	TDMFS setup time to TDMCLK	4	-	4	-	4	-
t45	TDMFS hold time to TDMCLK	2	-	2	-	2	-
t46	TDMDR data setup time to TDMCLK	4	-	4	-	4	-
t47	TDMDR data hold time to TDMCLK	2	-	2	-	2	-
t48	TDMDX data output delay to TDMCLK	0	2	0	2	0	2

Table 9. TDM Bus AC Timing

AUDIO PORT

The MPPex Audio Port has two modes of operation. The original mode allows the MPPex to be pin compatible with the original MPP chip. Decoder mode is selectable in software and converts the port to interface directly with low cost audio DACs.

ORIGINAL MODE

In original mode, the Audio port is a bidirectional serial port which carries audio data to and from the MPPex. It interfaces directly to the serial ports on Analog Devices 2101 DSPs and other DSPs with compatible ports. The port consists of a five-wire interface which can transfer data at rates of up to 16 Mbits/s. It is a single-channel serial bus with a fixed word length of 16 bits. It supports independent transmit and receive frame syncs with a fixed delay of one clock cycle between the frame sync and the transmission or receipt of data. It uses "normal" framing, so data is transmitted or received on the cycle after the Frame Sync is active. Data is transferred at the same rate as the ACLK. Figure 15 and table 11 show the timing of transfers on the Audio port.

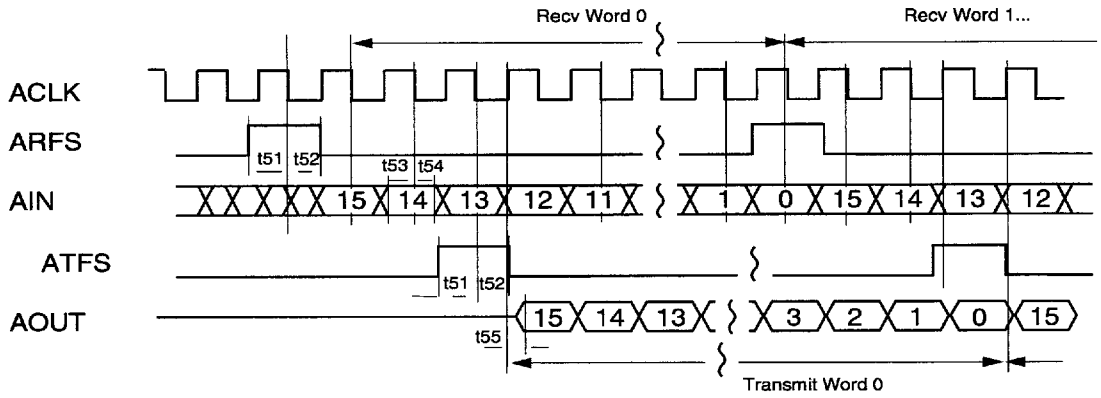

Figure 15. Audio Bus Timing

Symbol	Description	30Mhz		33MHz		40MHz	
		Min	Max	Min	Max	Min	Max
t11	ACLK period	62.5ns	-	62.5ns	-	62.5ns	-
t51	ATFS/ARFS setup time to ACLK	4	-	4	-	4	-
t52	ATFS/ARFS hold time to ACLK	2	-	2	-	2	-
t53	AIN setup time to ACLK	4	-	4	-	4	-
t54	AIN hold time to ACLK	2	-	2	-	2	-
t55	AOUT output delay time	0	2	0	2	0	2

Table 11. Audio Bus Timing

Depending on the application, the Audio port can be interfaced directly to a DSP or to an audio Analog-to-Digital & Digital-to-Analog codec, in which case the MPPex is responsible for any audio decompression.

DECODER MODE

In Decoder Mode the audio port is dedicated to decode functions only and the audio input function is disabled. In this mode the audio input clock should be 256xFs, where Fs is usually 32KHz, 44.1KHz or 48KHz. Two clock pins are available, ACLK1 and ACLK2, and can be selected by the MPPex software.

ADCLK is the audio DAC clock and is an output from the MPPex. The audio data out, AOUT, and left/right (ALR) pins are driven after the falling edge of the ADCLK. Figure xx and table xx show the signal timing in Decoder Mode.

The decoder mode can directly drive both popular DAC types, left justified and right justified. The justification mode select is done by MPPex software.

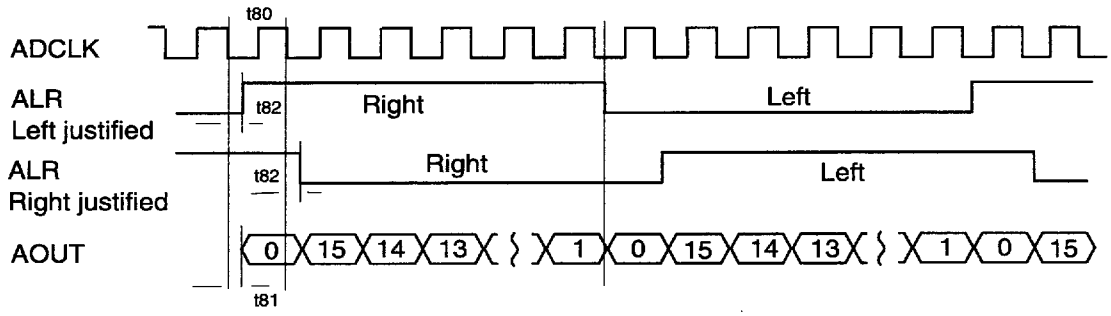

Figure 16. Decoder Mode Audio Port Timing

Symbol	Description	30MHz		33MHz		40MHz	
		Min	Max	Min	Max	Min	Max
t80	ADCLK period	62.5ns	-	62.5ns	-	62.5ns	-
t81	ALR output delay to ADCLK	0	4	0	4	0	4
t82	AOUT output delay to ADCLK	0	4	0	4	0	4

Table 12. Decoder Mode Audio Port Timing

HOST PORT

The Host Port is used by an external Host to control the MPPex and may also be used to transfer high- or low-speed user data, audio and bitstream information. The Host port is a generic 16-bit parallel bus which accesses six registers in the MPPex. The registers and their functions are detailed in the Register Description section. There are three ports in the Host Interface, a DMA port, a VCXI port and a Debug port. Figure 16 illustrates the timing relationships of the Host port.

The DMA port typically transfers user data (graphics, program executables etc.) that have been demultiplexed from the MPEG System compliant bitstream. In addition, the audio, video or system multiplexed bitstream can be carried over this interface.

The Host port uses the HRDREQ# and HWRREQ# pins to indicate its readiness to send and receive data. The HIRQ line is used by the MPPex to indicate that the HOSTIRQSTAT register should be interrogated.

The VCXI port transfers commands and status information between the MPPex and an external Host. In some systems, the MPPex will act as the System Controller and so there will be no external Host. However in computer based systems there will be another microprocessor responsible for controlling the system. It controls the MPPex through the VCXI port, using the VCXI's "shared variable" mechanism. This gives the Host read/write access to global control variables in the MPPex RISC's 'C' program and provides a simple and effective control mechanism.

The Debug port provides an additional path to the MPPex RISC for debugging purposes. This allows

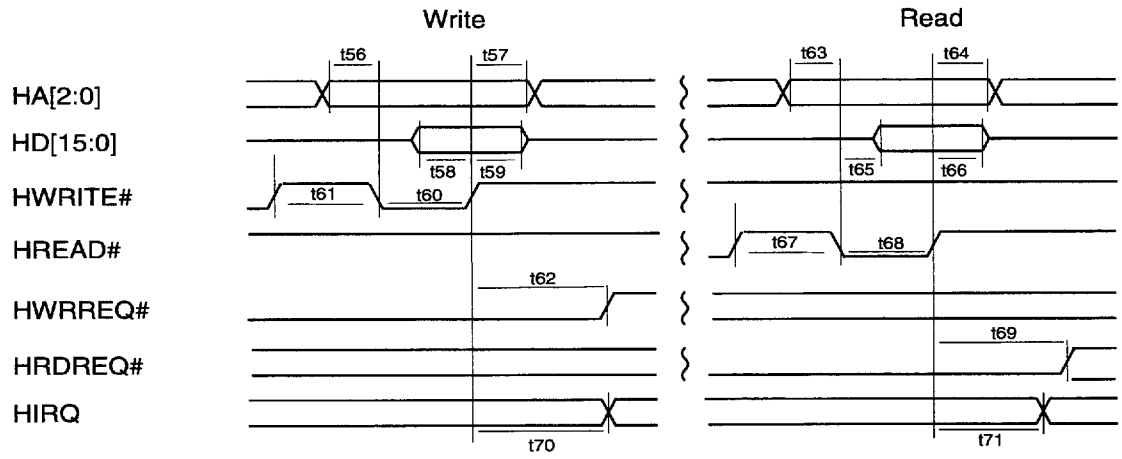

Figure 17. Host Bus Timing

software debuggers access to the state of the MPPex hardware and software without the disturbing the VCXI or DMA ports.

The Host port is implemented with a 16-bit data bus, a 3-bit address bus, read and write strobes and read and write request lines. The request lines indicate when there is data waiting for the Host to read or when the Host should write the data word. The lines can be programmed to indicate this for any combination of the DMA, VCXI or Debug ports.

Table 12 shows the timing of the Host port signals.

Symbol	Description	30MHz		33MHz		40MHz	
		Min	Max	Min	Max	Min	Max
t56	HA to HWRITE# setup time	4	-	4	-	4	-
t57	HA to HWRITE# hold time	2	-	2	-	2	-
t58	HD to HWRITE# setup time	4	-	4	-	4	-
t59	HD to HWRITE# hold time	2	-	2	-	2	-
t60	HWRITE# pulse width low	30	-	30	-	30	-
t61	HWRITE# pulse width high	30	-	30	-	30	-
t62	HWRREQ# to HWRITE# output delay	0	8	0	8	0	8
t63	HA to HREAD# setup time	4	-	4	-	4	-
t64	HA to HREAD# hold time	2	-	2	-	2	-
t65	HD to HREAD# output delay	0	4	0	4	0	4
t66	HD to HREAD# hold time	2	-	2	-	2	-
t67	HREAD# pulse width high	30	-	30	-	30	-
t68	HREAD# pulse width low	30	-	30	-	30	-
t69	HRDREQ# to HREAD# output delay	0	8	0	8	0	8
t70	HIRQ to HWRITE# output delay	0	8	0	8	0	8
t71	HIRQ to HREAD# output delay	0	8	0	8	0	8

Table 13. Host Port Timing

CLOCK GENERATORS

Figure 17 shows the clock distribution to the various sections of the MPPex. CPUCLK is the main system input clock to the MPPex and is used to derive the T-CLK for DRAM bus timing and the VPCLK. The pixel clock (PCLK2XSCN), the audio clock (ACLK) and TDM port clock (TDMCLK) are asynchronous and must be less than half the frequency of the clock of the section to which they are interfacing or less than the absolute maximum for that clock, whichever is lower.

The RISC processor uses the CPUCLK, and executes one instruction per cycle. This clock is also used by the Huffman decoder section, the SRAM DMA controller and the I/O resources served by the SRAM DMA controller.

The 2x T-Clock is used to time the memory accesses of the DRAM in addition to the timing of the various processing resources and the video filters. The T-CLK must be at least 4 times faster than the PCLK2XSCN to enable full 7 tap filtering (i.e. 2xCPUCLK > 4xPCLK). In situations where reduced filtering capacity is needed, the clock relationship can be relaxed.

The clock to the VPe is generated on board the MPPex and is selectable from 1x, 4/3x to 2x the CPUCLK. The MPPex is speed graded for both CPUCLK and VPCLK maximum speeds, the maximum speed of each clock is marked on the package.

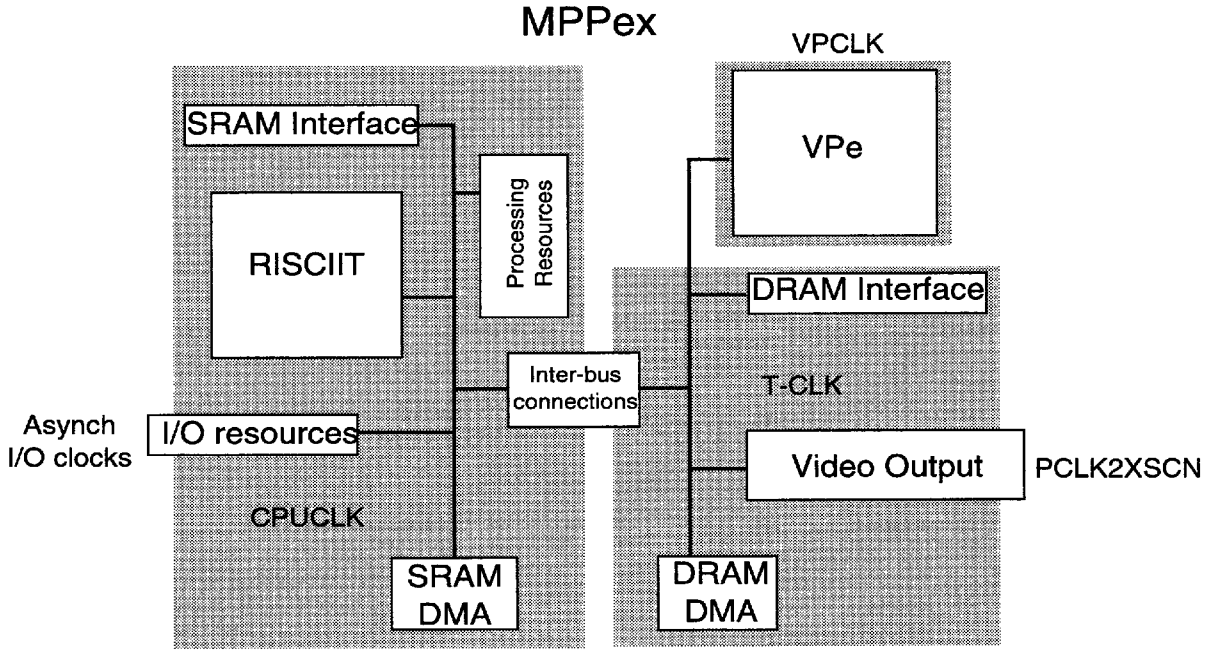

Figure 18. The MPPex Clock Distribution

SIGNAL DESCRIPTION

Name	I/O	Definition
LOE#	O	RISC Port output enable
LCE#[3:0]	O	RISC Port chip enables. RISC boots from internal ROM or LCE# = 0x03 depending on the value of ROMDIS.
LWRLL#	O	RISC port write enable byte 0
LWRLH#	O	RISC port write enable byte 1
LWRHL#	O	RISC port write enable byte 2
LWRHH#	O	RISC port write enable byte 3
LD[31:0]	I/O	RISC port data bus
LA[19:0]	O	RISC port address bus
RESET#	I	System reset (active low)
CPUCLK	I	RISC and System clock input
DEBUGIRQ	I	System debug interrupt
ROMDIS	I	Disable the internal boot ROM and boot from external ROM located at LCE# = 0x03
TEST2	O	Test output (phase45)
AUX[7:0]	I/O	Auxiliary Control Lines
HIRQ	O	Host Interrupt Request. Indicates an interrupt from the VC to the host.
HWRREQ#	O	Host DMA channel Write Request
HRDREQ#	O	Host DMA channel Read Request
HD[15:0]	I/O	Host Data Bus. Compressed data is passed to and from the VC across this bus. It is also used to pass commands and parameters from the host to the VC.
HA[2:0]	I	Host Address Bus. This bus is used by the host to address one of eight registers in the host interface.
HREAD#	I	Host Read. Enables data from the host interface onto the HDATA[15:0] bus.
HWRITE#	I	Host Write. Latches data from the HDATA[15:0] bus into the host interface registers.

Name	I/O	Definition
VSYNCSCN	I/O	Vertical Sync for Screen Video port Programmable for rising or falling edge
HSYNCSCN	I/O	Horizontal Sync for Screen Video port Programmable for rising or falling edge
BLANKSCN	O	Blanking for Screen Video port
PCLK2XSCN	I	Pixel Clock; two times the actual pixel clock for Screen Video port
PCLKQSCN	I	Pixel Clock qualifier in for Screen Video port
YSCN[7:0]	O	Y Luminance data bus for Screen Video port
UVSCN[7:0]	O	UV Chrominance data bus for Screen Video port
BLU[7:0]	O	Blue output image data when in 24 bit RGB mode
RAS#	O	Reference DRAM Row Address Strobe
CAS0#	O	Reference DRAM Column Address Strobe bank 0
DA[9:0]	O	Reference DRAM Multiplexed Address
DWE#	O	Reference DRAM Write Enable
DOE#	O	Reference DRAM Output Enable
DBUS[31:0]	I/O	Reference DRAM Data Bus
ACLK1	I	Audio Port Serial Clock
AIN	I	Audio Port Serial Data In
AOUT	O	Audio Port Serial Data Out
ARFS	I	Audio Port Receive Frame Sync
ATFS	I	Audio Port Transmit Frame Sync
ADCLK	O	Audio DAC output clock. Can be either 1x or 8x datarate.
ACLK2	I	Alternative, internally selectable audio input clock.
ALR	O	Audio left-right ouput signal. High for left, low for right.
TDMCLK	I	TDM Bus Serial Clock
TDMDR	I	TDM Bus Serial Data Receive
TDMDX	O	TDM Bus Serial Data Transmit
TDMFS	I	TDM Bus Frame Sync
TDMTSC#	O	TDM Bus Tristate Control; used to enable external driver for TDMDX
RSEL[1:0]	I	RAM bank 3 boot width select. 3 = 8 bits, 2 = 16 bits, 0 = 32 bits wide

REGISTER DESCRIPTION

The Host Interface allows communication between the VCP RISC and an external Host (if any). There are three access ports in the Host Interface for VCXI, DMA and Debug data transfer. All Host Interface registers are aligned on 16-bit boundaries and so the HADDR pins are 16-bit word addresses.

hostdmaport

0x0 (R/W)

hostdmaport

31	...	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	...	x	D15 - D0															

15-0: Host Data
DMA data transferred between the MPPex RISC processor and the Host. Typically this port is used for high-speed speed data transfer such as program or bit-stream. In RGB-24 bit display mode, DMA[15:8] are given over to BLUE[7:0] and the DMA port is disabled.

hostvcxport

0x1 (R/W)

hostvcxport

31	...	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	...	x	x	x	x	x	x	x	x	x	D7 - D0							

7-0: VCXI Data
VCXI data transferred between the MPPex RISC processor and the Host. Typically this port is used for VCXI commands and data.

hostdbgport

0x2 (R/W)

hostdbgport

31	...	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	...	x	x	x	x	x	x	x	x	x	D7 - D0							

7-0: Debug Data
Debug data transferred between the MPPex RISC processor and the Host. Typically this port is used for debugging only.

hostctl

0x3 (R/W)

hostctl

31	...	8	7	6	5	4	3	2	1	0
x	...	x	H2R Irq	Input select 2-0			Output select 2-0			Clr R2H

7: Host-to-RISC Interrupt Request
When the Host writes a '1' to this bit a Host-to-RISC interrupt is generated to the RISC.

6-4: Input select 2-0
Determines which of the DMA, VCXI and Debug ports contribute to the HWRREQ pin. The logic for this pin is

```
HWRREQ =  (DMATRE & Isel0) |
          (VCXTRE & Isel1) |
          (DBGTRE & Isel2)
```

3-1: Output select 2-0
Determines which of the DMA, VCXI and Debug ports contribute to the HRDREQ pin. The logic for this pin is

```
HRDREQ =  (DMADW & Osel0) |
          (VCXDW & Osel1) |
          (DBGDW & Osel2)
```

0: Clear RISC-to-Host interrupt
When the Host writes a '1' to this bit it clears the RISC-to-Host interrupt.

hostmask

0x4 (R/W)

hostmask

31	...	8	7	6	5	4	3	2	1	0
x	...	x	End ian Sel	Dbug TRE En	Dbug DW En	DMA TRE En	DMA DW En	VCX TRE En	VCXI DW En	R2H Irq En

The bits in this register determine if a condition causes a Host interrupt on the HIRQ pin. If not, the interrupt status is still set in the *hostirqstat* register.

7: Data Endian Select
When this bit is set to '1', the Host port expects little endian data. Otherwise data is big endian.

6: Debug Port TRE Interrupt Enable
When this bit is set to '1', the Host is interrupted when the Debug port is waiting for data to be written by the Host.

5: Debug Port DW Interrupt Enable
When this bit is set to '1', the Host is interrupted when the Debug port contains data which the Host should read.

4: DMA Port TRE Interrupt Enable
When this bit is set to '1', the Host is interrupted when the DMA port is waiting for data to be written by the Host.

3: DMA Port DW Interrupt Enable
When this bit is set to '1', the Host is interrupted when the DMA port contains data which the Host should read.

2: VCXI Port TRE Interrupt Enable
When this bit is set to '1', the Host is interrupted when the VCXI port is waiting for data to be written by the Host.

1: VCXI Port DW Interrupt Enable
When this bit is set to '1', the Host is interrupted when the VCXI port contains data which the Host should read.

0: RISC-to-Host Interrupt Enable
When this bit is set to '1', the RISC-to-Host interrupt will cause an interrupt to the Host.

hostirqstat

0x5 (RD)

hostirqstat

31	...	8	7	6	5	4	3	2	1	0
x	...	x	x	Dbug TRE	Dbug DW	DMA TRE	DMA DW	VCX TRE	VCXI DW	R2H Irq

6: **Debug Port TRE Interrupt Status**
When this bit is set to '1', the Debug port is waiting for data to be written by the Host.

5: **Debug Port DW Interrupt Status**
When this bit is set to '1', the Debug port contains data which the Host should read.

4: **DMA Port TRE Interrupt Status**
When this bit is set to '1', the DMA port is waiting for data to be written by the Host.

3: **DMA Port DW Interrupt Status**
When this bit is set to '1', the DMA port contains data which the Host should read.

2: **VCXI Port TRE Interrupt Status**
When this bit is set to '1', the VCXI port is waiting for data to be written by the Host.

1: **VCXI Port DW Interrupt Status**
When this bit is set to '1', the VCXI port contains data which the Host should read.

0: **RISC-to-Host Interrupt Status**
When this bit is set to '1', the RISC-to-Host interrupt has occurred.

PINOUT 208 QUAD FLAT PACK

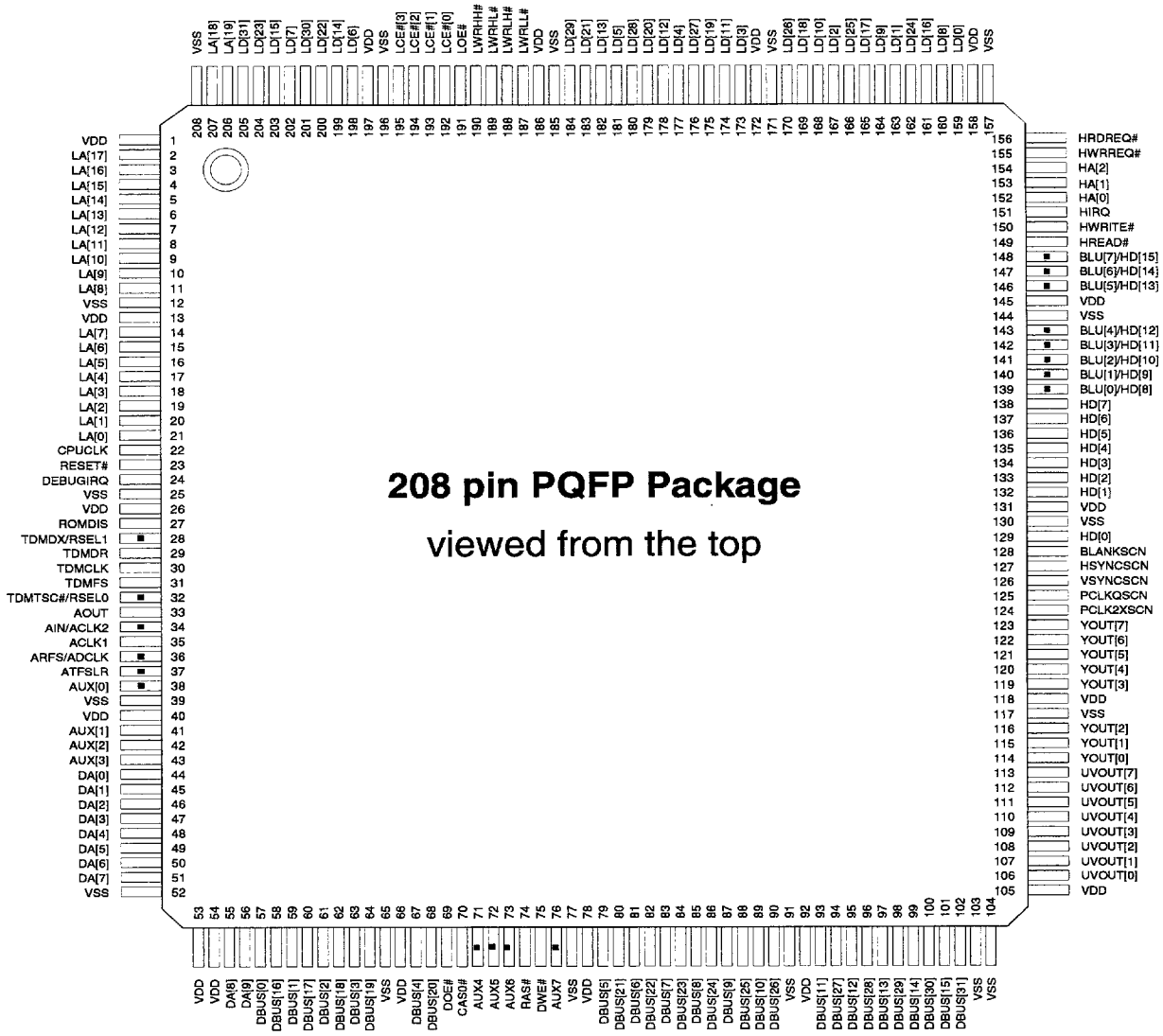

Figure 18. 208 QFP MPP Pinout

Note:
The black mark indicates a change from previous versions of the MPP chip.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	-65°C to 110°C
Voltage Range on any Pin	-0.5V to (Vcc + 0.5V)
Power Dissipation	2.1 Watts @ 33MHz

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range	0°C to 70°C
Supply Voltage Vcc	4.75V to 5.25V

DC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

Symbol	Parameter	Min	Max	Unit	Notes
Vih	High Level Input Voltage	2.0	Vcc+0.25	V	All inputs TTL levels except CLK
Vil	Low Level Input Voltage	-0.3	0.8	V	All inputs TTL levels except CLK
Vch	CLK High Level Input	2.0	Vcc+0.25	V	TTL level input
Vcl	CLK Low Level Input	-0.3	0.8	V	TTL level input
Voh	High Level Ouptput Voltage	3.0	-	V	IOH = 1mA
Vol	Low Level Output Voltage	-	0.45	V	IOL = 4mA
Ili	Input Leakage Current	-	±15	µA	
Ilo	Output Leakage Current	-	±15	µA	
Cin	Input Capacitance	-	10	pF	fc = 1 MHz
Co	Input/Output Capacitance	-	12	pF	fc = 1 MHz
Cclk	CLK Capacitance	-	20	pF	fc = 1 MHz

Table 14. DC Electrical Characteristics

AC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

All timings are in nanoseconds (ns).

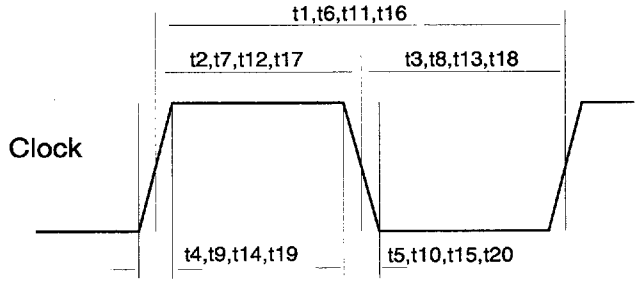

Figure 20. Clock Timing Diagram

Symbol	Description	30MHz		33MHz		40MHz	
		Min	Max	Min	Max	Min	Max
t1	Clock Period	33.3	100ns	30.3ns	100ns	25ns	100ns
t2	Clock low time	27ns	-	24ns	-	21ns	-
t3	Clock high time	27ns	-	24ns	-	21ns	-
t4	Clock rise time	-	6	-	3	-	3
t5	Clock fall time	-	6	-	3	-	3

Table 15. CPUCLK Timing

Symbol	Description	30MHz		33MHz		40MHz	
		Min	Max	Min	Max	Min	Max
t6	Pixel Clock Period	33ns	-	30ns	-	30ns	-
t7	Pixel Clock low time	15ns	-	15ns	-	15ns	-
t8	Pixel Clock high time	15ns	-	15ns	-	15ns	-
t9	Pixel Clock rise time	-	4ns	-	4ns	-	4ns
t10	Pixel Clock fall time	-	4ns	-	4ns	-	4ns

Table 16. PCLK2XSCN Timing

Symbol	Description	30MHz		33MHz		40MHz	
		Min	Max	Min	Max	Min	Max
t11	Audio Clock Period	62.5n	-	62.5ns	-	62.5ns	-
t12	Audio Clock low time	25ns	-	25ns	-	25ns	-
t13	Audio Clock high time	25ns	-	25ns	-	25ns	-
t14	Audio Clock rise time	-	6	-	3	-	3
t15	Audio Clock fall time	-	6	-	3	-	3

Table 17. ACLK Timing

Symbol	Description	30MHz		33MHz		40MHz	
		Min	Max	Min	Max	Min	Max
t16	TDM Clock Period	62.5n	-	62.5ns	-	62.5ns	-
t17	TDM Clock low time	25ns	-	25ns	-	25ns	-
t18	TDM Clock high time	25ns	-	25ns	-	25ns	-
t19	TDM Clock rise time	-	6	-	3	-	3
t20	TDM Clock fall time	-	6	-	3	-	3

Table 18. TDMCLK Timing

MECHANICAL

208-LEAD QUAD FLAT PACK

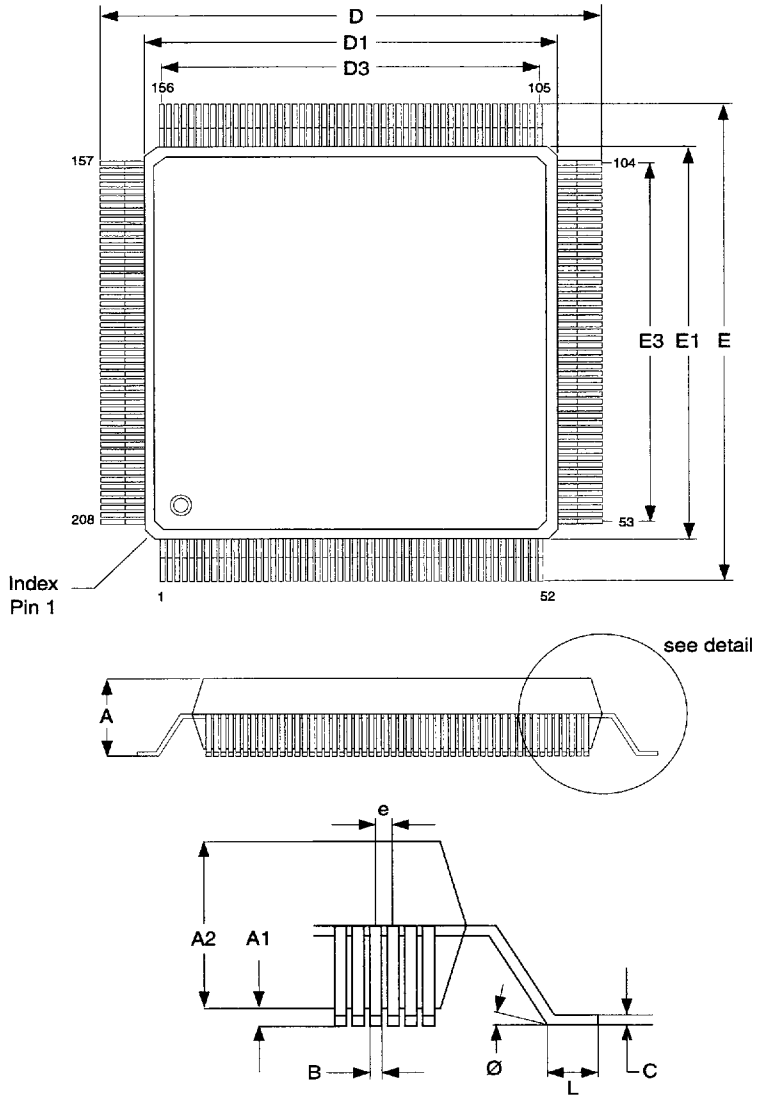

Figure 19. PQFP Mechanical

Note:
1.All dimensions are in inches (millimeters)
2. Actual package used has millimeter native dimensions - take care with rounding from metric to imperial.

Symbol	Min	Nom	Max
A	-	-	0.165 (4.20)
A1	0.010 (0.25)	-	-
A2	0.130 (3.30)	0.134 (3.40)	0.138 (3.50)
B	0.007 (0.18)	0.009 (0.23)	0.011 (0.28)
C	0.005 (0.12)	0.006 (0.16)	0.008 (0.20)
D	1.195 (30.35)	1.205 (30.60)	1.215 (30.85)
D1	1.098 (27.90)	1.102 (28.00)	1.106 (28.10)
D3	1.004 (25.50) REF		
e	0.0197 (0.50) BASIC		
E	1.195 (30.35)	1.205 (30.60)	1.215 (30.85)
E1	1.098 (27.90)	1.102 (28.00)	1.106 (28.10)
E3	1.004 (25.50) REF		
L	0.016 (0.40)	0.020 (0.50)	0.024 (0.60)
¿	0¡	2.5¡	5.0¡

Table 19. PQFP Mechanical