

## CMOS 4-BIT MICROCONTROLLER

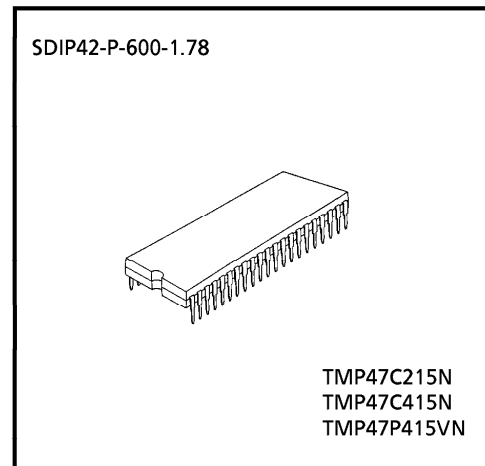
**TMP47C215N**  
**TMP47C415N**

The 47C215/415 is a high speed and high performance 4-bit single chip microcomputer, integrating high current output port and the 4 bit A/D conversion input based on the TLCS-470 series.

PART No.	ROM	RAM	PACKAGE	OTP
TMP47C215N	2048 × 8-bit	128 × 4-bit	SDIP42-P-600-1.78	TMP47P415VN
TMP47C415N	4096 × 8-bit	256 × 4-bit		

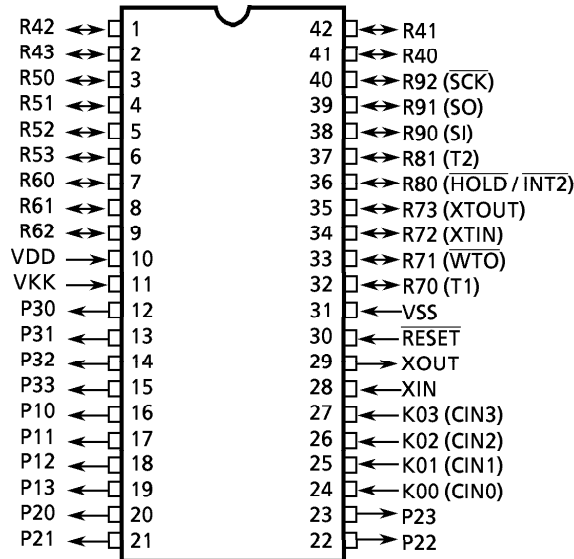
**FEATURES**

- ◆ 4-bit single chip microcomputer
- ◆ Instruction execution time: 1.0  $\mu$ s (at 8 MHz),  
244  $\mu$ s (at 32.8 kHz)
- ◆ 90 basic instructions
  - Table look-up instructions
  - 5-bit to 8-bit data conversion instruction
- ◆ Subroutine nesting: 15 levels max.
- ◆ 5 interrupt sources (External: 1, Internal : 4)  
All sources have independent latches each, and multiple interrupt control is available.
- ◆ I/O port (36 pins)
  - Input 1 ports 4 pins
  - Output 3 ports 12 pins
  - I/O 6 ports 20 pins
- ◆ Interval Timer
- ◆ Two 12-bit Timer / Counters  
Timer, event counter, and pulse width measurement mode
- ◆ Watchdog Timer
- ◆ Serial Interface with an 8-bit buffer
  - Simultaneous transmission and reception capability
  - External / internal clock, leading / trailing edge shift, and 4/8-bit mode
- ◆ 4-bit A/D conversion input 4 channels
- ◆ High break down voltage outputs  
VFT direct drive capability (23 bit)
- ◆ High current outputs  
LED direct drive capability (typ. 15 mA × 1 bits).
- ◆ Dual-clock operation  
High-speed / Low-power-consumption operating mode
- ◆ Hold function  
Battery/Capacitor back-up
- ◆ Real Time Emulator : BM47C415N0A

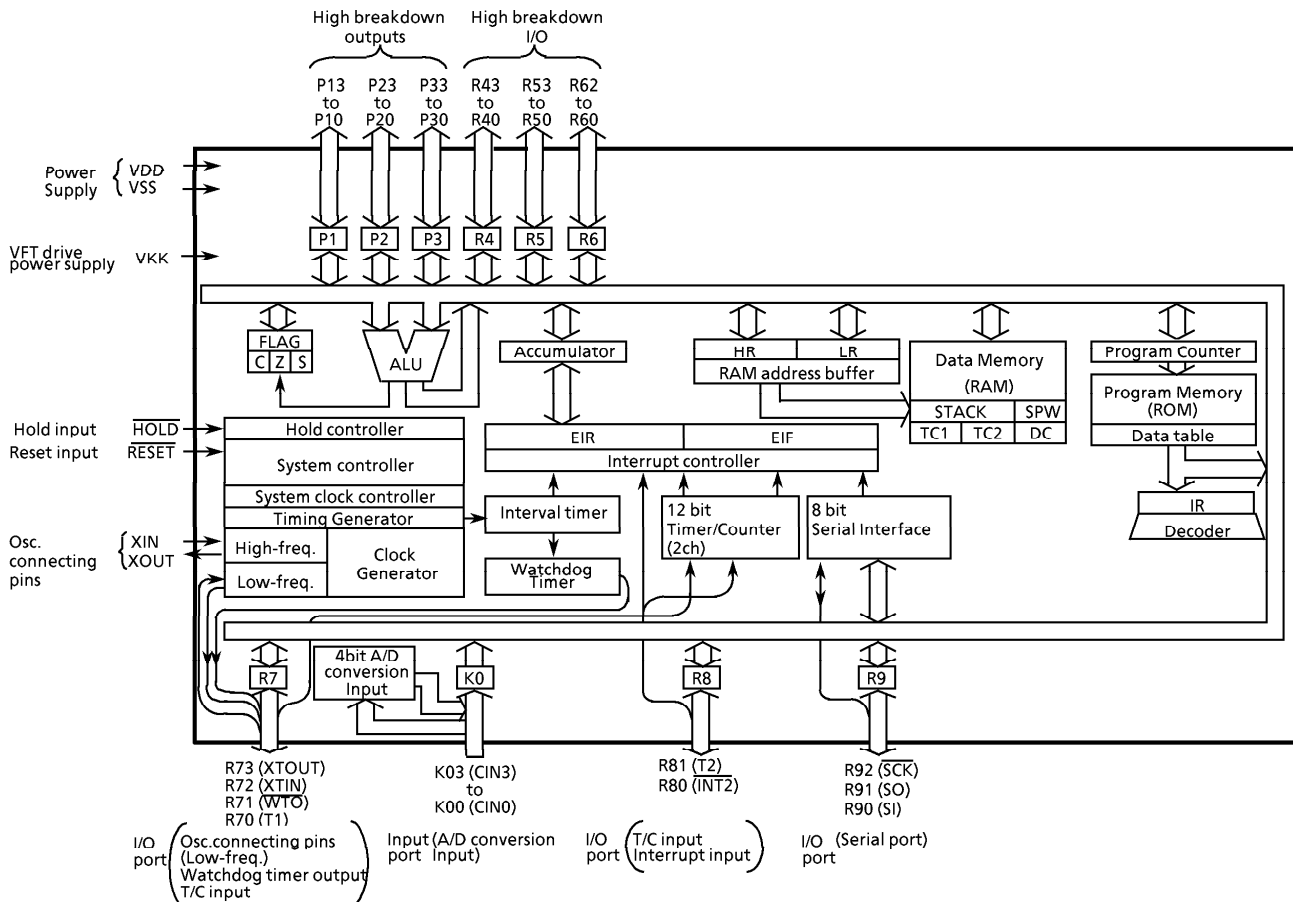


PIN ASSIGNMENTS (TOP VIEW)

SDIP42-P-600-1.78



BLOCK DIAGRAM



## PIN FUNCTION

PIN NAME	Input / Output	FUNCTION	
K03 (CIN3) to K00 (CIN0)	Input (Input)	4-bit input port	A/D Conversion (comparator) Input
P13 to P10	Output	4-bit high breakdown voltage output port with latch 8-bit data are output by the 5-bit to 8-bit data conversion instruction [OUTB @ HL.]	
P23 to P20			
P33 to P30	Output	4-bit high breakdown voltage output port with latch	
R43 to R40	I/O	4-bit high breakdown voltage I/O port with latch	
R53 to R50			
R62 to R60		3-bit high breakdown voltage I/O port with latch	
R73 (XTOUT)	I/O (Output)	4-bit I/O port with latch. When using as the input port or watchdog timer output, the latch must be set to "1". Set to Dual-clock operating mode, when R73, R72 pin use as clock generator.	Resonator connecting pin (Low-freq.) For inputting external clock, XTIN is used and XTOUT is opened.
R72 (XTIN)	I/O (Input)		Watchdog timer output
R71 ( $\overline{\text{WTO}}$ )	I/O (Output)		
R70 (T1)	I/O (Input)		Timer / Counter 1 external input
R81 (T2)	I/O (Input)	2-bit I/O port with latch. When used as the input port, external interrupt input pin, or timer / counter external input pin, the latch must be set to "1".	Timer / Counter 2 external input
R80 (INT2) / $\overline{\text{HOLD}}$	I/O (Input)		External interrupt 2 or hold request / release signal input
R92 ( $\overline{\text{SCK}}$ )	I/O (I/O)	3-bit I/O port with latch. When used as the input port or serial port, the latch must be set to "1".	Serial clock I/O
R91 (SO)	I/O (Output)		Serial data output
R90 (SI)	I/O (Input)		Serial data input
XIN	Input	Resonator connecting pin (High-frequency).	
XOUT	Output	For inputting external clock, XIN is used and XOUT is opened.	
$\overline{\text{RESET}}$	Input	Reset signal input	
VDD	Power Supply	+ 5 V	
VSS		0 V (GND)	
VKK		VFT drive power supply	

**OPERATIONAL DESCRIPTION**

Concerning the 47C215/415 the configuration and functions of hardware are described. As the description has been provided with priority on those parts differing from the 47C660/860, the technical data sheets for the 47C660/860 shall also be referred to.

**1. SYSTEM CONFIGURATION**

◆INTERNAL CPU FUNCTION

They are the same as those of the 47C660/860 except program memory (ROM), data memory (RAM) system clock controller and interrupt function.

◆PERIPHERAL HARDWARE FUNCTION

- ① Input / Output Ports
- ② Interval Timer
- ③ Timer / Counters (TC1, TC2)
- ④ Watchdog Timer
- ⑤ A/D Conversion (Comparator) input
- ⑥ Serial Interface

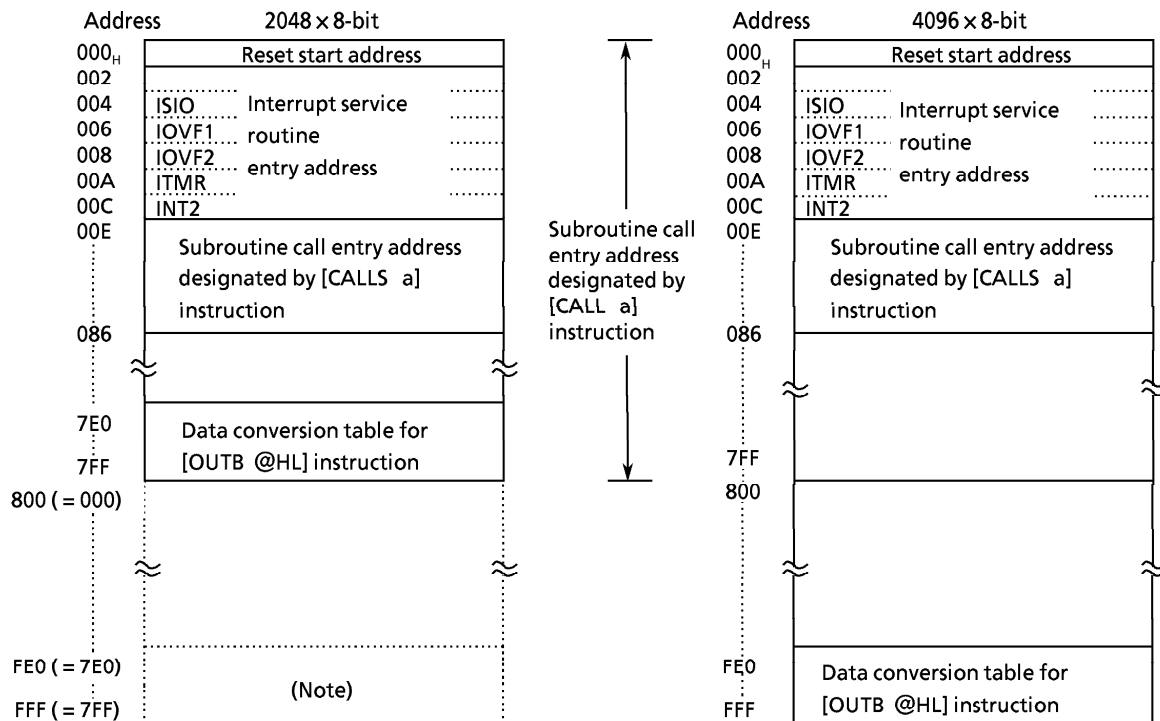
The description has been provide with priority on functions (① and ⑤) added to and changed form 47C660/860.

**2. INTERNAL CPU FUNCTION**

**2.1 Program Memory (ROM)**

The 47C215 has 2048 × 8 bits (addresses 000<sub>H</sub> through 7FF<sub>H</sub>) of program memory (mask ROM), the 47C415 has 4096 × 8 bits (addresses 000<sub>H</sub> through FFF<sub>H</sub>).

Figure 2-1 shows the program memory map. Address 000<sub>H</sub> to 086<sub>H</sub> and FE0<sub>H</sub> to FFF<sub>H</sub> (000<sub>H</sub> to 086<sub>H</sub> and 7E0<sub>H</sub> to 7FF<sub>H</sub> for the 47C215) of the program memory are also used for special purposes.



Note. When the 47P415 is used, the address from FE0<sub>H</sub> to FFF<sub>H</sub> are used as the data conversion table area.

(a) 47C215

(b) 47C415

Figure 2-1. Program Memory Map

On the 47C215, no physical program memory exists in the address range 800<sub>H</sub> through FFF<sub>H</sub>. However, if this space is accessed by program, the most significant bit of each address is always regarded as "0" and the contents of the program memory corresponding to the address 000<sub>H</sub> through 7FF<sub>H</sub> are read. For example, when outputting the data at address FF3<sub>H</sub> are read to ports by the [OUTB @HL] instruction, the data at address 7F3<sub>H</sub> is actually read. That is, on the 47C215, the conversion table is located in the address space 7E0<sub>H</sub> through 7FF<sub>H</sub>. When evaluating the 47C215 by using the 47P415. However, the conversion table must be allocated in the memory location addressed FE0<sub>H</sub> through FFF<sub>H</sub> also.

## 2.2 Data Memory (RAM)

The 47C415 has 256 × 4 bits (addresses 00<sub>H</sub> through FF<sub>H</sub>) of the data memory (RAM), and the 47C215 has 128 × 4 bits (addresses 00<sub>H</sub> through 0F<sub>H</sub>, and 90<sub>H</sub> through FF<sub>H</sub>).

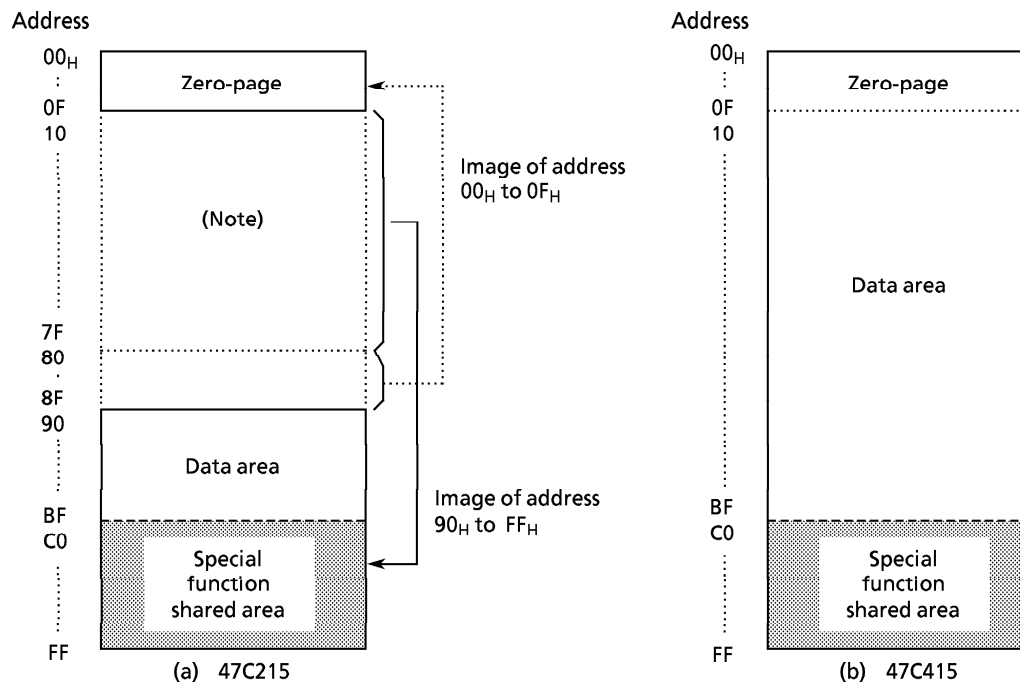


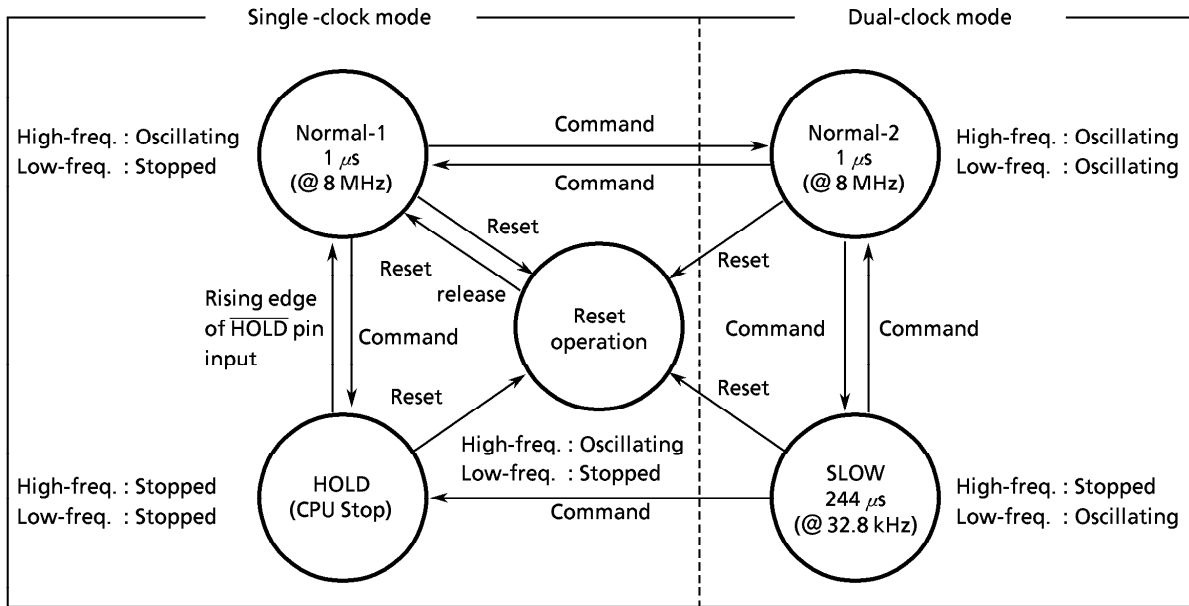
Figure 2-2. Data Memory Capacity and Address Assignment

*Note: With the 47C215, the most significant bit of the RAM address is always regarded as "0", so that addresses 90<sub>H</sub> to FF<sub>H</sub> may be accessed as addresses 10<sub>H</sub> to 7F<sub>H</sub>. However, programming should be performed assuming that the RAM is assigned to addresses 00<sub>H</sub> to 0F<sub>H</sub> and 90<sub>H</sub> to FF<sub>H</sub> as shown in Figure 2-2 by considering the application software evaluation with development tools.*

### 2.3 System Clock Controller

The system clock controller starts or stops the high-frequency and low-frequency clock oscillator and switches between the basic clocks. The operating mode is generally divided into the single-clock mode and the dual-clock mode, which are controlled by command. The 47C215/415 can swithc from SLOW operation mode to HOLD operation mode.

After HOLD operation mode was released, Normal-1 operation mode is set.



Note . Normal-1 and Normal-2 operating modes are sometimes referred to as the Normal operating mode collectively.

Figure 2-3. Operating Mode Transition Diagram

Note . Returning from SLOW operation to Normal-2 operation

When returning from SLOW operation to Normal-2 operation, the warming up timer is used to change the operation frequency after getting stabilized oscillation of the low-frequency clock.

The watchdog timer counter is used to count the warming up time.

To count cerainly the warming up time, it is necessary to initialize the counter. When returning from SLOW operation to Normal-2 operation, the watchdog timer must be cleared just before setting of the system clock control command register.

Example. Returning from SLOW operation to Normal-2 operation

```
LD      A, #0000B
OUT     A, %OP15
LD      A, #1100B
OUT     A, %OP16
```

2.4 INTERRUPT FUNCTION

(1) Interrupt Controller

There are 5 interrupt sources (1 external and 4 internal).

The prioritized multiple interrupt capability is supported.

The interrupt latches (IL<sub>4</sub> through IL<sub>0</sub>) to hold interrupt requests are provided for the interrupt sources. Each interrupt latch is set to "1" when an interrupt request is made, asking the CPU to accept the interrupt. The acceptance of interrupt can be permitted or prohibited by program through the interrupt enable master flip-flop (EIF) and interrupt enable register (EIR). When two or more interrupts occur simultaneously, the one with the highest priority determined by hardware is serviced first.

Sources		Priority	Interrupt latch	Permit conditions by program	Entry address
Internal	Serial interface interrupt (ISIO)	(High rank) 1	IL <sub>4</sub>	EIF = 1, EIR <sub>3</sub> = 1	0004 <sub>H</sub>
	Timer / Counter 1 overflow interrupt (IOVF1)	2	IL <sub>3</sub>	EIF = 1, EIR <sub>2</sub> = 1	0006 <sub>H</sub>
	Timer / Counter 2 overflow interrupt (IOVF2)	3	IL <sub>2</sub>		0008 <sub>H</sub>
	Interval timer interrupt (ITMR)	4	IL <sub>1</sub>	EIF = 1, EIR <sub>1</sub> = 1	000A <sub>H</sub>
External	External interrupt 2 (INT2)	(Low rank) 5	IL <sub>0</sub>		000C <sub>H</sub>

Table 2-2. Interrupt Sources

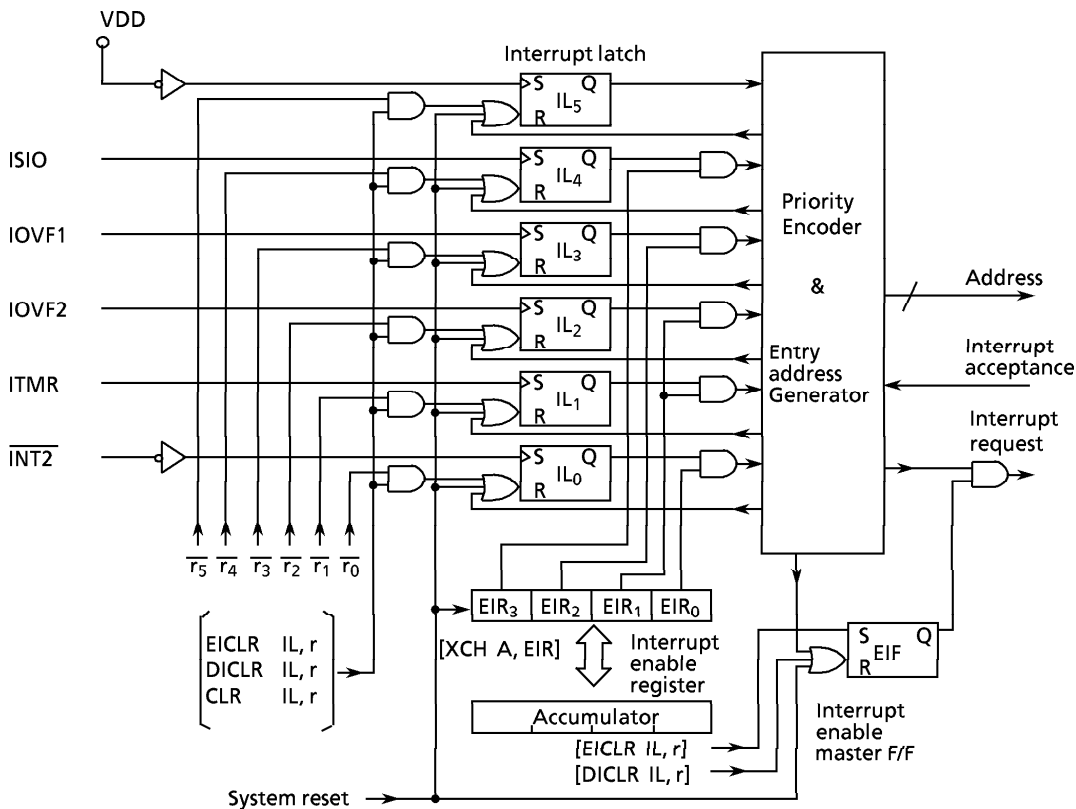


Figure 2-24. Interrupt Controller Block Diagram

a. Interrupt enable master flip-flop (EIF)

The EIF controls the enable / disable of all interrupts. When this flip-flop is cleared to "0", all interrupts are disabled; when it is set to "1", the interrupts are enabled.

When an interrupt is accepted, the EIF is cleared to "0", temporarily disabling the acceptance of subsequent interrupts.

When the interrupt service program has been executed, the EIF is set to "1" by the execution of the interrupt return instruction [RETI], being put in the enabled state again.

Set or clear of the EIF in program is performed by instructions [EICLR IL,r] and [DICLR IL,r], respectively. The EIF is initialized to "0" during reset.

b. Interrupt enable register (EIR)

The EIR is a 4-bit register specifies the enable or disable of each interrupt except INT1. An interrupt is enabled when the corresponding bit of the EIR is "1", and an interrupt is disabled when the corresponding bit of the EIR is "0". Bit 1 (EIR<sub>1</sub>) of the EIR is shared by both IOVF2 and ITMR interrupts.

Read/write on the EIR is performed by executing [XCH A,EIR] instruction. The EIR is initialized to "0" during reset.

c. Interrupt latches (IL)

An interrupt latch is provided for each interrupt source. It is set to "1" when an interrupt request is made to ask the CPU for accepting the interrupt. Each latch is cleared to "0" upon acceptance of the interrupt. It is initialized to "0" during the reset.

The interrupt latches can be cleared independently by interrupt latch operation instructions ([EICLR IL,r], [DICLR IL,r], and [CLR IL,r]) to make them cancel interrupt requests or initialize by program. When the value of instruction field(r) is "0", the interrupt latch is cleared; when the value is "1", the IL is held. Note that the interrupt latches cannot be set by instruction.

Example 1 : To enable IOVF1 and INT2

```
LD      A, #0101B    ; EIR←0101B
XCH     A,  EIR
EICLR   IL, 111111B  ; EIF←1
```

Example 2 : To set the EIF to "1" and to clear the interrupt latches except ISIO to "0".

```
EICLR   IL, 010000B  ; EIF←1, IL5←0, IL3-IL0←0
```

(2) Interrupt Processing

An interrupt request is held until the interrupt is accepted or the IL is cleared by reset or the interrupt latch operation instruction. The interrupt acknowledge processing is performed in 2 instruction cycles after the end of the current instruction execution (or after the timer/counter processing if any). The interrupt service program terminates upon execution of the interrupt return instruction [RETI]. The interrupt acknowledge processing consists of the following sequence:

- ① The contents of the program counter and the flags are saved on the stack.
- ② The interrupt entry address corresponding to the interrupt source is set to the program counter.
- ③ The status flag is set to "1".
- ④ The EIF is cleared to "0", temporarily disabling the acceptance of subsequent interrupts.
- ⑤ The IL for the accepted interrupt source is cleared to "0".
- ⑥ The instruction stored at the interrupt entry address is executed. (Generally, in the program memory space at the interrupt entry address, the branch instruction to each interrupt processing program is stored. Note that the interrupt entry address is assigned every 2-byte, so that the long branch instruction can not be stored in the program normally. The interrupt service program is assigned to the memory locations 0000<sub>H</sub> through 0FFF<sub>H</sub>.)

To perform the multi-interrupt, EIF is set to "1" in the interrupt service program, and the acceptable interrupt source is selected by the EIR.



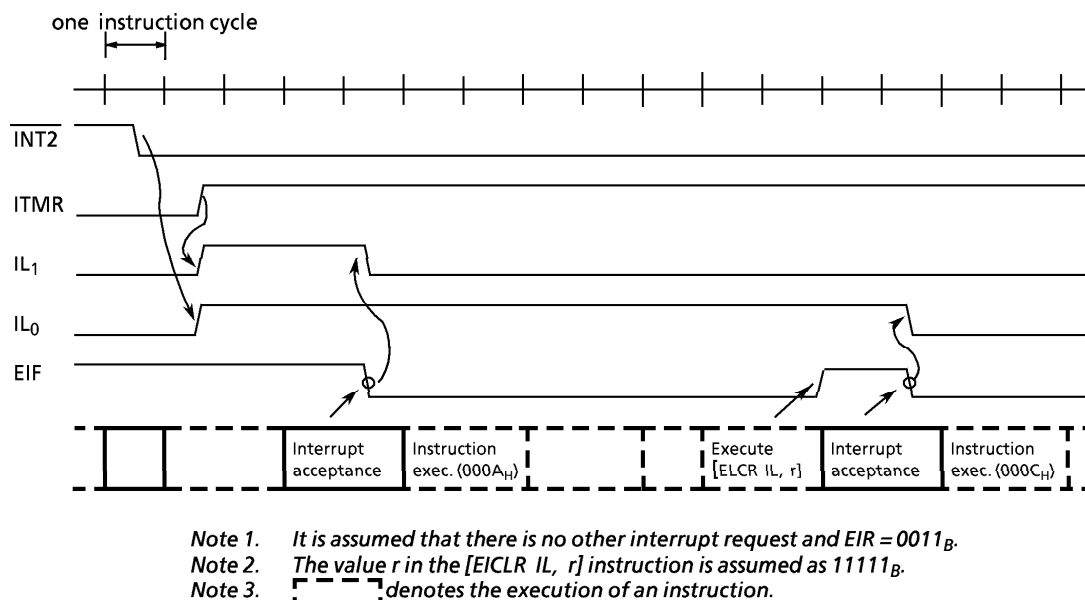


Figure 2-25. Interrupt Timing Chart (Example)

The interrupt return instruction [RETI] performs the following operations:

- ① Restores the contents of the program counter and the flags from the stack.
- ② Sets the EIF to "1" to provide the interrupt enable state again.

Note. When the time required for the interrupt service is longer than that for the interrupt request, only the interrupt service program is executed without executing the main program.

In the interrupt processing, the program counter and flags are automatically saved or restored but the accumulator and other registers (H or L register, DMB, DC, etc.) are not. If it is necessary to save or restore them, it must be performed by program as shown in the following example. To perform the multi-interrupt, the saving RAM area never be overlapped.

Example 1 : To save/restore accumulator and HL register pair.

XCH HL, GSAV1 ; RAM[GSAV1] ↔ HL

XCH A, GSAV1 + 2 ; RAM[GSAV1 + 2] ↔ Acc

Note. The lower 2 bits of GSAV1 should be "0's".

### (3) External Interrupt

When an external interrupt (INT2) occurs, the interrupt latch is set at the falling edge of the corresponding pin input (INT2).

The INT2 interrupt can be enabled / disabled by the EIR.

Therefore, the INT2 interrupt occurs at the falling edge of the pin input when R80 (INT2) pin is used for the I/O port.

But bit 0 of the EIR is only kept at "0" not accepting the interrupt request.

Because the external interrupt input is the hysteresis type, each of high and low level operation requires 2 or more instruction cycles for a correct interrupt operation.

### 3. PERIPHERAL HARDWARE FUNCTION

#### 3.1 Input / Output Ports

The 47C215/415 has 10 I/O ports (36 pins) each as follows:

- ① K0 ; 4-bit input (shared with comparator inputs)
- ② P1, P2, P3 ; 4-bit output (shared with segment outputs)
- ③ R4, R5 ; 4-bit input / output (shared with digit outputs)
- ④ R6 ; 3-bit input / output (shared with digit outputs)
- ⑤ R7 ; 4-bit input / output (shared with the low-frequency resonator connecting pins, the watchdog timer output and timer/counter input)
- ⑥ R8 ; 2-bit input / output (shared with external interrupt request input and timer / counter input)
- ⑦ R9 ; 3-bit input / output (shared with serial port)

Each output port contains a latch, which holds the output data. The input ports have no latch; therefore, it is desired hold data externally until it is read or to read twice or more before processing it.

Port Address (**)	Port		Input/Output instruction							
	Input (IP**)	Output (OP**)	IN %p, A	OUT A, %p	OUT #, %p	OUTB @HL	SET %p, b	TEST %p, b	SET @L	
00H	K0 input port	P0 output port	○	○	○	-	-	○	-	
01	(A/D conversion input)	(Note 2)	○	○	○	○ (Note 3)	○	○	-	
02	P1 output latch	P1 output port	○	○	○	○	○	○	-	
03	P2 output latch	P2 output port	○	○	○	○	○	○	-	
04	P3 output latch	P3 output port	○	○	○	○	○	○	-	
05	R4 input port	R4 output port	○	○	○	○	○	○	○	
06	R5 input port	R5 output port	○	○	○	○	○	○	○	
07	R6 input port	R6 output port	○	○	○	○	○	○	○	
08	R7 input port	R7 output port	○	○	○	○	○	○	○	
09	R8 input port	R8 output port	○	○	○	○	○	○	○	
0A	R9 input port	R9 output port	○	○	○	○	○	○	○	
0B	—	—	-	-	-	-	-	-	-	
0C	—	—	-	-	-	-	-	-	-	
0D	—	—	-	-	-	-	-	-	-	
0E	Status input (Note 4)	Serial transmit buffer	○	○	○	-	-	○	-	
0F	Serial receive buffer	Serial transmit buffer	○	○	○	-	-	-	-	
10H	Undefined	Hold operating mode control	-	○	-	-	-	-	-	
11	Undefined	—	-	-	-	-	-	-	-	
12	Undefined	A/D conversion input control	-	-	-	-	-	-	-	
13	SK0 status	K0 port input selector	○	○	-	-	-	-	-	
14	Undefined	—	-	-	-	-	-	-	-	
15	Undefined	Watchdog timer control	-	○	-	-	-	-	-	
16	Undefined	System clock control	-	○	-	-	-	-	-	
17	Undefined	—	-	-	-	-	-	-	-	
18	Undefined	Interval timer interrupt control	-	○	-	-	-	-	-	
19	Undefined	—	-	-	-	-	-	-	-	
1A	Undefined	—	-	-	-	-	-	-	-	
1B	Undefined	—	-	-	-	-	-	-	-	
1C	Undefined	Timer/counter 1 control	-	○	-	-	-	-	-	
1D	Undefined	Timer/counter 2 control	-	○	-	-	-	-	-	
1E	Undefined	Serial interface control 1	-	○	-	-	-	-	-	
1F	Undefined	Serial interface control 2	-	○	-	-	-	-	-	

Note 1 "—" means the reserved state. Unavailable for the user programs.

Note 2 As concerns the port address "00". In and TEST instructions operate port K0, and out instruction operates port P0.

Note 3 The 5-bit to 8-bit data conversion instruction [OUTB @HL], automatic access to ports P1 and P2.

Note 4 The status input of serial interface, clock generator, and HOLD (KE0) pin.

Table 3-1. Port Address Assignments and Available I/O Instructions

3.1.1 I/O port

(1) K0 (K03 to K00) PORT

The 4-bit input port. Port K0 is shared with the A/D converter (comparator) input. The K0 port input selector (OP13) determines whether this port is to be used for digital or comparator input. The most significant bit of the K0 port input selector is set to "1" for digital input and to "0" for comparator input. The K0 port input selector is initialized to "0" during reset.

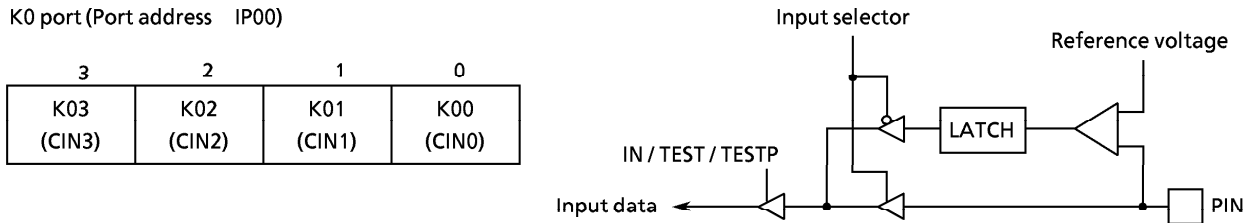


Figure 3-1. K0 port

(2) P1 (P13 to P10), P2 (P23 to P20), P3 (P33 to P30) port

The 4-bit high breakdown voltage output ports with latch, which can directly drive Vacuum Fluorescent Tubes (VFT). The latch data can be read by input instruction. The latch is initialized to "0" during reset.

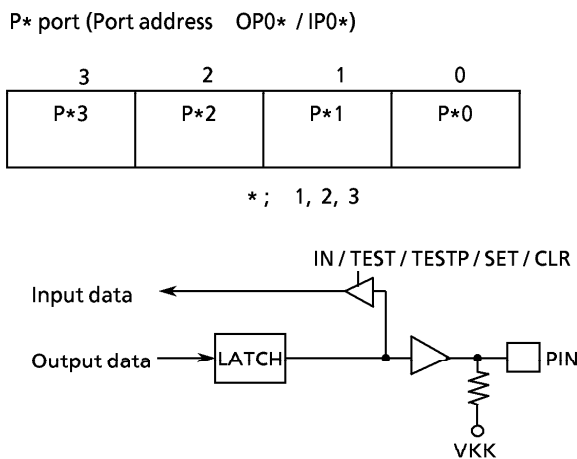


Figure 3-2. Ports P1, P2, P3

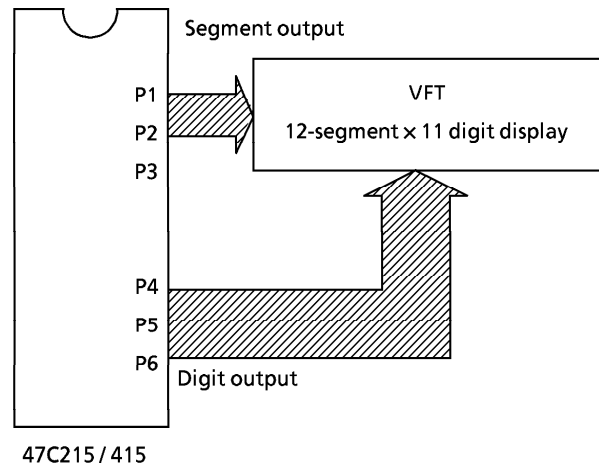


Figure 3-3. Example of driving a VFT

(3) Ports R4 (R43 to R40), R5 (R53 to R50), R6 (R62 to R60), R7 (R73 to R70)

These ports are 4-bit I/O ports with a latch. When used as an input port, the latch (R4, R5 and R6) must be set to "0" and the latch (R7) must be set to "1". The latch (R4, R5 and R6) is initialized to "0" during reset. The R7 latch is initialized to "1" during Reset. These 4 ports (16 pins) can be set, cleared, and tested for each bit as specified by L register indirect addressing bit manipulation instructions [SET @L], [CLR @L], and [TEST @L]. Table 3-2 lists the pins (I/O ports) that correspond to the L register contents.

Example: To clear R43 pin as specified by the L register indirect addressing bit manipulation instruction.

```
LD    L, #0011B ; Set R43 pin address to L register
CLR  @L         ; R43←0
```

L register				Pin
3	2	1	0	
0	0	0	0	R40
0	0	0	1	R41
0	0	1	0	R42
0	0	1	1	R43

L register				Pin
3	2	1	0	
0	1	0	0	R50
0	1	0	1	R51
0	1	1	0	R52
0	1	1	1	R53

L register				Pin
3	2	1	0	
1	0	0	0	R60
1	0	0	1	R61
1	0	1	0	R62
1	0	1	1	-

L register				Pin
3	2	1	0	
1	1	0	0	R70
1	1	0	1	R71
1	1	1	0	R72
1	1	1	1	R73

Table 3-2. Relationship between L register contents and I/O port bits

a. R4 (R43 to R40), R5 (R53 to R50), R6 (R62 to R60) port

The 4-bit high breakdown voltage I/O ports with latch, which can directly drive Vacuum Fluorescent Tubes (VFT). The latch should be cleared to "0" when used as an input port. The is initialized to "0" during reset.

R\* port (Port address OP0\* / IP0\*)

3	2	1	0
R*3	R*2	R*1	R*0

\*; 4, 5, 6

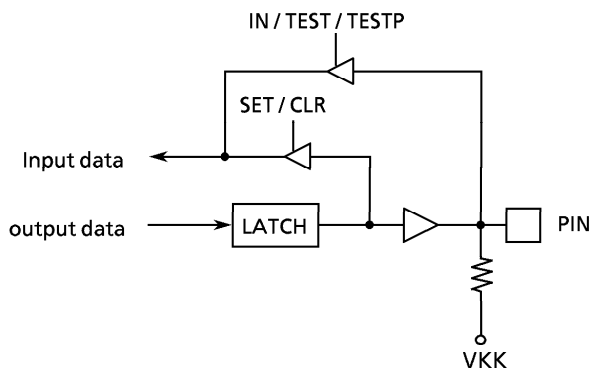


Figure 3-4. R4, R5, R6 port

※ VFT drive power supply (VKK)

The 23 pins of the P1, P2, P3, R4, R5, R6 ports are P-channel open drain construction with pulldown resistor. Each pin is connected to a VKK pin via a pulldown resistor (TYP. 80 kΩ). Thus, Vacuum Fluorescent Tubes (VFT) can be driven by applying a negative (-) voltage to the VKK pin, without using external resistor.

b. Port R7 is shared by the low-frequency resonator connection pins (XTIN, XTOUT), the timer / counter1 input pin and the watchdog timer output pin ( $\overline{WTO}$ ). For the dual-clock mode operation, the low-frequency resonator(32.768 kHz) is connected to R72 (XTIN) and R73 (XTOUT) pins. For the single-clock mode operation, R72 and R73 pins are used for the ordinary I/O ports. When the watchdog timer is used, R71 ( $\overline{WTO}$ ) becomes the watchdog timer output pin. The watchdog timer output is the logical AND output with the port R71 output latch. To use the R71 pin for an ordinary I/O port, the watchdog timer must be disabled (with the watchdog timer output set to "1"). When used as a timer / counter1, R70 latch must be set to "1". To use it for an ordinary I/O port, the event counter / pulse width measurement modes of the timer / counter1 must be disabled.

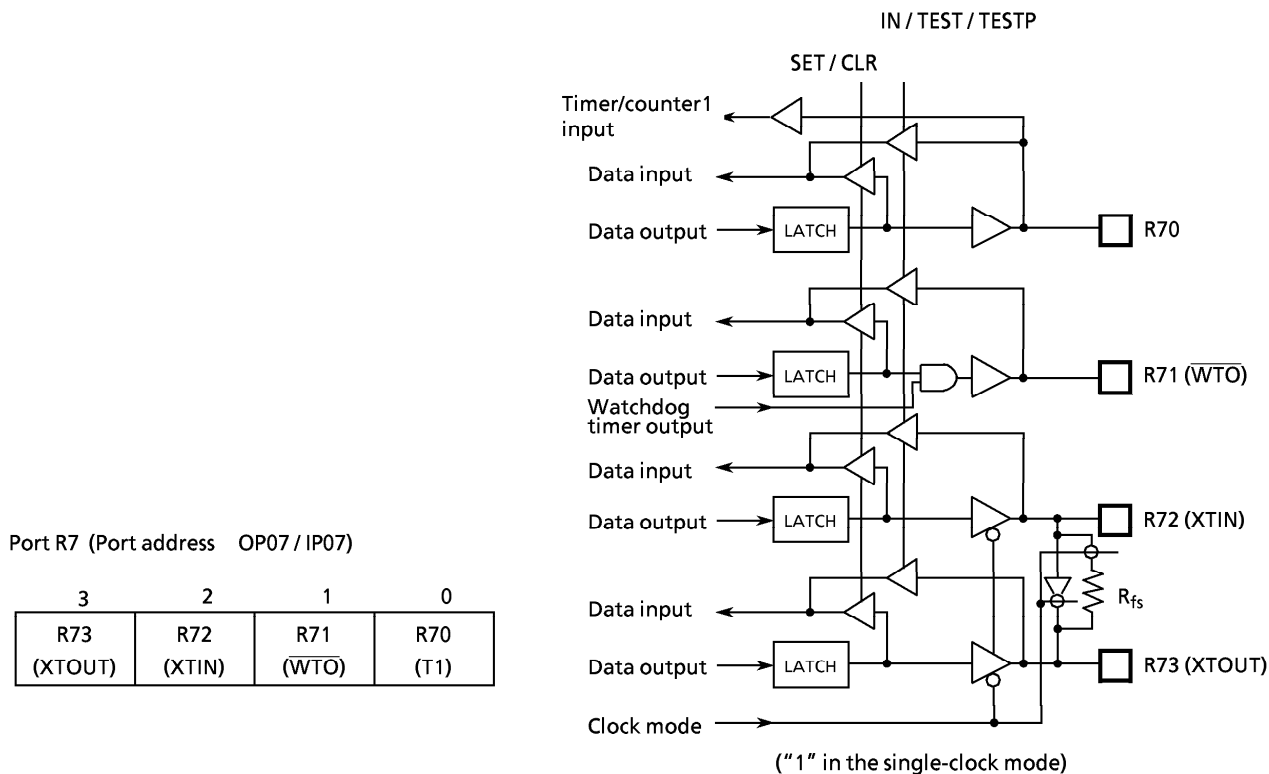


Figure 3-5. Port R7

(4) PORT R8 (R80 to R81) and  $\overline{\text{HOLD}} / (\overline{\text{INT2}})$  pin

a. R80 ( $\overline{\text{INT2}} / \overline{\text{HOLD}}$  (KE0))

Port KE (KE0) is a 1bit sense input port shared with the hold request/release signal input pin ( $\overline{\text{HOLD}}$ ), the external interrupt 2 input pin and the R80 I/O pin. This input port (KE0) is assigned to the least significant bit of port address IP0E and is processed as the data with inverted polarity. For example, if an input instruction is executed with the pin on the high level, "0" is read. The bit1 through bit3 of port KE, an uncertain value is read when an input instruction is executed.

b. R81

Port R81 is a I/O port with a latch. When used as input port, the latch must be set to "1". The latch is initializes to "1" during reset. Port R81 is shared with the timer / counter2 input pin. To use this port for the timer / counter2 input pin, the latch should be set to "1". To use it for an ordinary I/O port, the event countre / pulse width measurement modes of the timer/counter should be disabled.

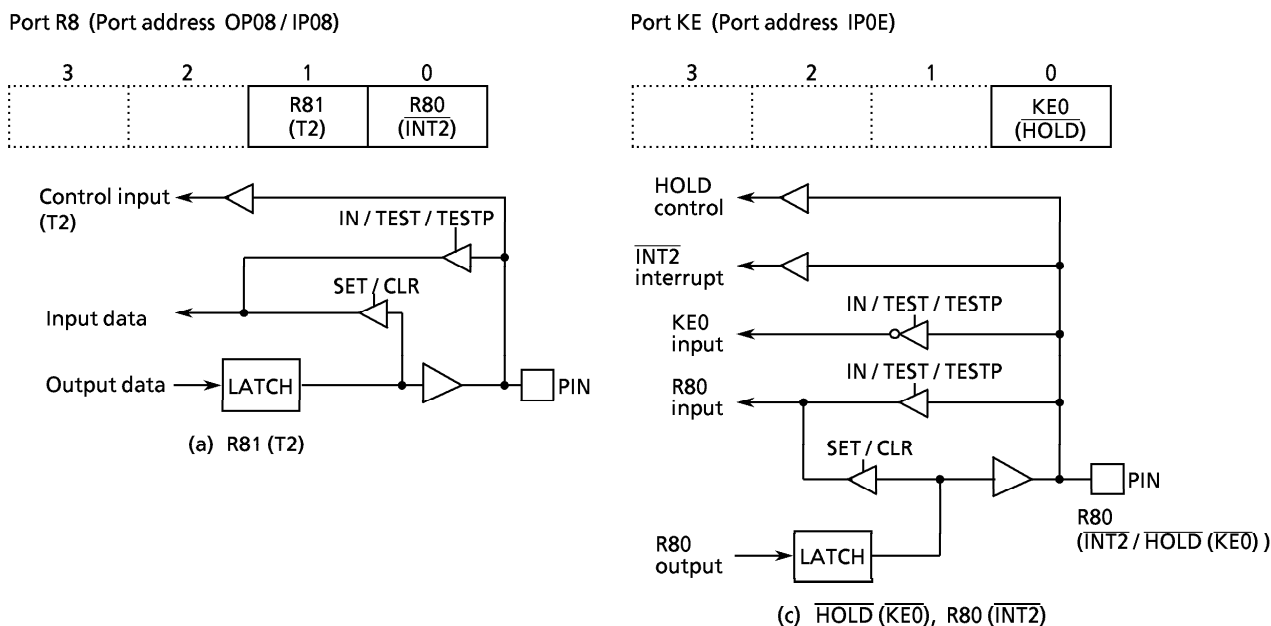


Figure 3-6. Port R8 and port KE

*Note: When  $\overline{\text{HOLD}} (\overline{\text{INT2}})$  pin is used for an I/O port, external interrupt 2 occurs upon detection of the falling edge of pin input therefore a bit 0 of the interrupt enable resister (EIR0) should be clear to "0".*





### 3.2 4bit A/D Conversion (Comparator) Input

The comparator input is analog input to discriminate key input or AFC (Auto Frequency Control) signal. It's composed of 4-bit D/A converter, comparator and control circuit. Analog input level (CIN0 to CIN3) can be detected as 16-stage by setting reference voltage.

The comparator input can also be used as K0 port (digital input). To use as K0 port, set the most significant bit of the port address OP13 to "1". Which port is selected digital (K0) or comparator (CIN) input can be monitored by accessing the port address IP13.

#### 3.2.1 Circuit Configuration of Comparator Input

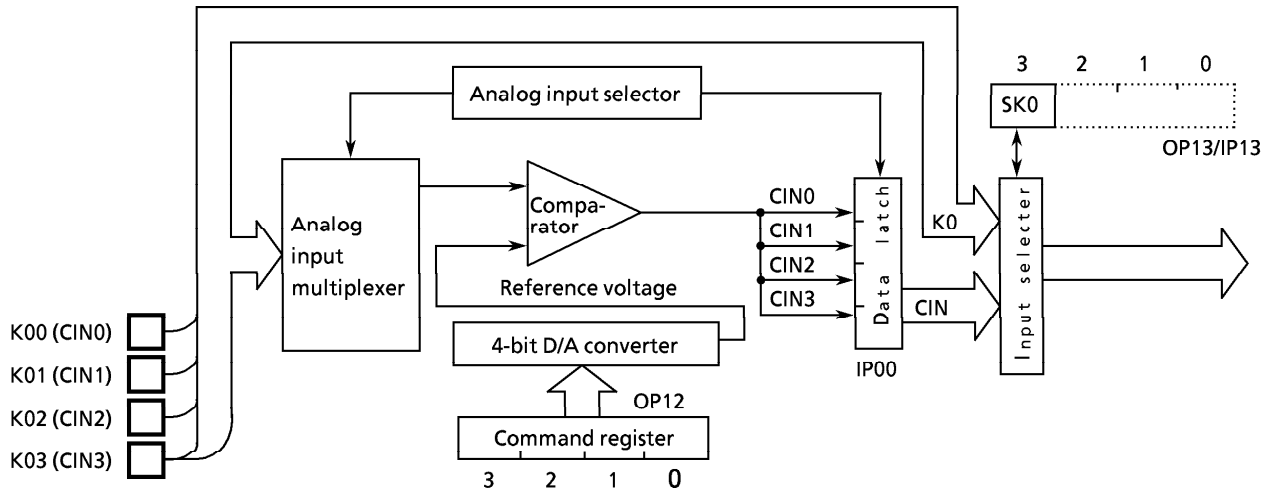


Figure 3-8. Circuit of Comparator Input

### 3.2.2 Control of Comparator Input

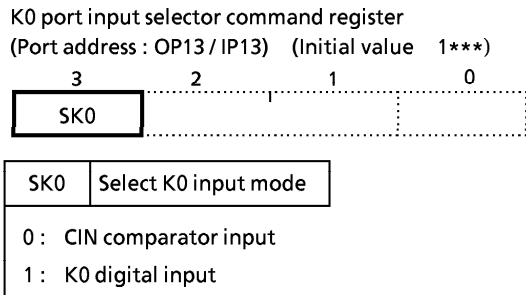


Figure 3-9. Command Register, Status Register

Reference voltage (Vref) is set by command register (port address OP12), and it is determined by the following form.

$$V_{REF} = V_{DD} \times (n + 1) / 16 [V] \quad (n = 0 \text{ to } 15)$$

After initialization sequence, 4-channel comparator inputs continue comparison operation successively.

Since 2-instruction cycles are required to complete comparison of 1-channel, it is necessary to wait for 8-instruction cycles after setting a reference voltage to read data from the comparator. When analog input voltage is higher than reference voltage, comparator data latch is set to "1". At the initialization sequence, OP12 is set to "0". There is not latch when used to port K0.

OP12				Vref. [V]
3	2	1	0	
0	0	0	0	0.31
0	0	0	1	0.62
0	0	1	0	0.94
0	0	1	1	1.25
0	1	0	0	1.56
0	1	0	1	1.87
0	1	1	0	2.19
0	1	1	1	2.50
1	0	0	0	2.81
1	0	0	1	3.12
1	0	1	0	3.44
1	0	1	1	3.75
1	1	0	0	4.06
1	1	0	1	4.37
1	1	1	0	4.69
1	1	1	1	5.00

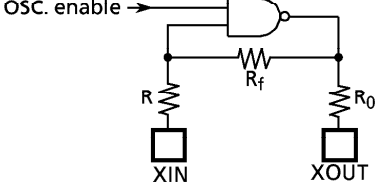
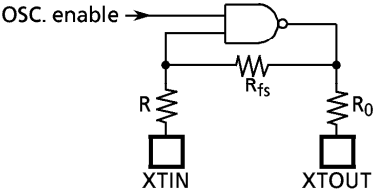
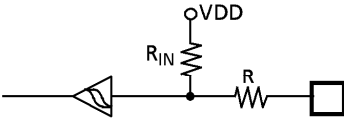
Table 3-3. Reference Voltage

*Note. When the comparator input is selected, the comparator consumes typically 700 μA current at VDD = 5 V. To reduce the power consumption, K0 port should be set to digital input mode. In the HOLD mode, the comparator current is automatically cut off by hardware. Further, during the slow operating mode, A/D conversion input is automatically disabled by hardware to reduce the power consumption.*

INPUT/OUTPUT CIRCUITRY

(1) Control pins

The input / output circuitries of the 47C215/415 control pins are shown below.

CONTROL PIN	I/O	CIRCUITRY	REMARKS
XIN XOUT	Input Output		Resonator connecting pins $R = 1\text{ k}\Omega$ (typ.) $R_f = 1.5\text{ M}\Omega$ (typ.) $R_0 = 2\text{ k}\Omega$ (typ.)
XTIN XTOUT	Input Output		Resonator connecting pins $R = 1\text{ k}\Omega$ (typ.) $R_{fs} = 6\text{ M}\Omega$ (typ.) $R_0 = 220\text{ k}\Omega$ (typ.)
RESET	Input		Hysteresis input Pull-up resistor $R_{IN} = 220\text{ k}\Omega$ (typ.) $R = 1\text{ k}\Omega$ (typ.)

(2) I/O ports

The input / output circuitries of the 47C215/415 I/O ports are shown below, any one of the circuitries can be chosen by a code (MA - MC) as a mask option.

PORT	I/O	Input / Output Circuitry (Code)			REMARKS
		MA	MB	MC	
K0	Input				Pull-up / Pull-down resistor $R_{IN} = 70\text{ k}\Omega$ (typ.) $R = 1\text{ k}\Omega$ (typ.)
P1 P2 P3	Output				Source open drain output Initial "Hi-Z" High-breakdown voltage $R_K = 80\text{ k}\Omega$ (typ.)
R4 R5 R6	I/O				Source open drain output Initial "Hi-Z" High-breakdown voltage $R_K = 80\text{ k}\Omega$ (typ.) $R = 1\text{ k}\Omega$ (typ.)
R7	I/O	R70 	R71, R72, R73 	Sink open drain output Initial "Hi-Z" Hysteresis input (R70) $R = 1\text{ k}\Omega$ (typ.) High current (R70) $I_{OL} = 15\text{ mA}$ (typ.)	
R8 R9	I/O	Initial "Hi-Z" 			Sink open drain output Initial "Hi-Z" Hysteresis input $R = 1\text{ k}\Omega$ (typ.)

## ELECTRICAL CHARACTERISTICS

## ABSOLUTE MAXIMUM RATINGS

 $(V_{SS} = 0\text{ V})$ 

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	$V_{DD}$		- 0.3 to 6.5	V
Input Voltage	$V_{IN}$		- 0.3 to $V_{DD} + 0.3$	V
Output Voltage	$V_{OUT1}$	R7, R8, R9, XOUT	- 0.3 to $V_{DD} + 0.3$	V
	$V_{OUT3}$	P1, P2, P3, R4, R5, R6	$V_{DD} - 40$ to $V_{DD} + 0.3$	
Output Current (per 1 pin)	$I_{OUT1}$	R70	30	mA
	$I_{OUT2}$	R71 to R73, R80, R81, R9	3.2	
	$I_{OUT3}$	P1, P2, P3	- 12	
	$I_{OUT4}$	R4, R5, R6	- 25	
Output Current (Total)	$\Sigma I_{OUT3}$	P1, P2, P3	- 80	mA
	$\Sigma I_{OUT4}$	R4, R5, R6	- 100	
Power Dissipation [ $T_{opr} = 70^\circ\text{C}$ ]	PD		600	mW
Soldering Temperature (time)	Tsld		260 (10 s)	$^\circ\text{C}$
Storage Temperature	Tstg		- 55 to 125	$^\circ\text{C}$
Operating Temperature	Topr		- 30 to 70	$^\circ\text{C}$

Note. Output voltage  $V_{OUT3}$  : The  $V_{OUT3}$  of OTP (TMP47P415VN) is from  $V_{DD} - 38$  (V) to  $V_{DD} + 0.3$  (V).

## RECOMMENDED OPERATING CONDITIONS

 $(V_{SS} = 0\text{ V}, T_{opr} = - 30\text{ to }70^\circ\text{C})$ 

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	$V_{DD}$		In the Normal mode	4.5	5.5	V
			In the SLOW mode	2.7		
			In the HOLD mode	2.0		
Input - High Voltage	$V_{IH1}$	Except Hysteresis Input	$V_{DD} \geq 4.5\text{V}$	$V_{DD} \times 0.7$	$V_{DD}$	V
	$V_{IH2}$	Hysteresis Input		$V_{DD} \times 0.75$		
	$V_{IH3}$		$V_{DD} < 4.5\text{V}$	$V_{DD} \times 0.9$		
Input - Low Voltage	$V_{IL1}$	Except Hysteresis Input	$V_{DD} \geq 4.5\text{V}$	0	$V_{DD} \times 0.3$	V
	$V_{IL2}$	Hysteresis Input			$V_{DD} \times 0.25$	
	$V_{IL3}$		$V_{DD} < 4.5\text{V}$		$V_{DD} \times 0.1$	
Clock Frequency	fc	XIN, XOUT		0.4	8.0	MHz
	fs	XTIN, XTOUT		30.0	34.0	kHz

Note. Input voltage  $V_{IH3}$ ,  $V_{IL3}$  : in the SLOW or HOLD mode

## D.C. CHARACTERISTICS

(V<sub>SS</sub> = 0 V, T<sub>opr</sub> = -30 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V <sub>HS</sub>	Hysteresis Input		-	0.7	-	V
Input Current	I <sub>IN1</sub>	K0, $\overline{\text{RESET}}$	V <sub>DD</sub> = 5.5 V,	-	-	± 2	μA
	I <sub>IN2</sub>	R ports (open drain)	V <sub>IN</sub> = 5.5 V / 0 V				
Input Resistance	R <sub>IN1</sub>	KO port with pull-up/pull-down		30	70	150	kΩ
	R <sub>IN2</sub>	$\overline{\text{RESET}}$		100	220	450	
Pull-down resistance	R <sub>K</sub>	source open drain	V <sub>DD</sub> = 5.5 V, V <sub>KK</sub> = -30 V	-	80	-	
Output Leakage Current	I <sub>LO1</sub>	sink open drain	V <sub>DD</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V	-	-	2	μA
	I <sub>LO2</sub>	source open drain	V <sub>DD</sub> = 5.5 V, V <sub>OUT</sub> = -30 V	-	-	-2	
Output Level High Voltage	V <sub>OH</sub>	P1, P2, P3	V <sub>DD</sub> = 4.5 V, I <sub>OH</sub> = -5 mA	2.4	-	-	V
Output Level Low Voltage	V <sub>OL</sub>	R71 to R73, R80, R81, R9	V <sub>DD</sub> = 4.5 V, I <sub>OL</sub> = 1.6 mA	-	-	0.4	V
Output Level High Current	I <sub>OH</sub>	R4, R5, R6	V <sub>DD</sub> = 4.5 V, V <sub>OL</sub> = 2.4 V	-	-15	-	mA
Output Level Low Current	I <sub>OL</sub>	R70	V <sub>DD</sub> = 4.5 V, V <sub>OL</sub> = 1.0 V	-	15	-	mA
Supply Current (in the Normal mode)	I <sub>DD</sub>		V <sub>DD</sub> = 5.5 V, f <sub>c</sub> = 4 MHz	-	3	6	mA
Supply Current (in the SLOW mode)	I <sub>DDS</sub>		V <sub>DD</sub> = 3.0 V, f <sub>s</sub> = 32.768 kHz	-	30	60	μA
Supply Current (in the HOLD mode)	I <sub>DDH</sub>		V <sub>DD</sub> = 5.5 V	-	0.5	10	μA

Note 1. Typ. values show those when T<sub>opr</sub> = 25 °C, V<sub>DD</sub> = 5 V

Note 2. Input Current I<sub>IN1</sub> ; The current through resistor is not included, when the input resistor (pull-up / pull-down) is contained.

Note 3. Supply Current I<sub>DD</sub>, I<sub>DDH</sub> ; V<sub>IN</sub> = 5.3 V / 0.2 V  
The K0 port is open when the input resistor is contained. The voltage applied to the R port is within the valid range.

I<sub>DDS</sub> ; V<sub>IN</sub> = 2.8 V / 0.2 V, low frequency clock is only oscillated (connecting XTIN, XTOUT).  
at comparator input is disabled.

## A/D conversion characteristics

(V<sub>SS</sub> = 0 V, V<sub>DD</sub> = 4.5 to 5.5 V, T<sub>opr</sub> = -30 to 70 °C)

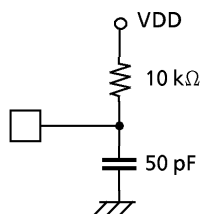
PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Input Voltage	V <sub>AIN</sub>	CIN3 to CIN0		V <sub>SS</sub>	-	V <sub>DD</sub>	V
A/D conversion error				-	-	± 1/2	LSB

A.C. CHARACTERISTICS

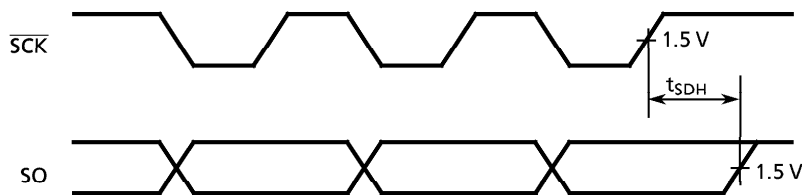
( $V_{SS} = 0\text{ V}$ ,  $V_{DD} = 4.5\text{ to }5.5\text{ V}$ ,  $T_{opr} = -30\text{ to }70\text{ }^\circ\text{C}$ )

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	$t_{cy}$	In the Normal mode	1.0	—	20	$\mu\text{s}$
		In the SLOW mode	235	—	267	
High level clock pulse width	$t_{WCH}$	External clock mode	80	—	—	ns
Low level clock pulse width	$t_{WCL}$					
Shift Data Hold Time	$t_{SDH}$		$0.5 t_{cy} - 300$	—	—	ns

Note. External circuit for  $\overline{\text{SCK}}$  Pin and SO pin



Serial port (completion of Transmission)



RECOMMENDED OSCILLATING CONDITIONS

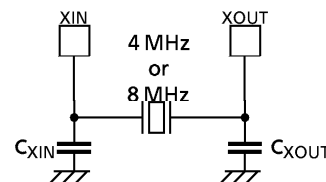
( $V_{SS} = 0\text{ V}$ ,  $V_{DD} = 4.5\text{ to }6.0\text{ V}$ ,  $T_{opr} = -30\text{ to }70\text{ }^\circ\text{C}$ )

(1) 8 MHz

Ceramic Resonator

CSA8.00MT (MURATA)  $C_{XIN} = C_{XOUT} = 30\text{ pF}$

KBR8.00M (KYOCERA)  $C_{XIN} = C_{XOUT} = 30\text{ pF}$



(2) 4 MHz

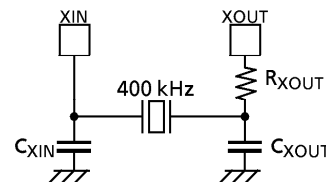
Ceramic Resonator

CSA4.00MG (MURATA)  $C_{XIN} = C_{XOUT} = 30\text{ pF}$

KBR-4.00MS (KYOCERA)  $C_{XIN} = C_{XOUT} = 30\text{ pF}$

Crystal Oscillator

204B-6F 4.0000 (TOYOCOM)  $C_{XIN} = C_{XOUT} = 20\text{ pF}$

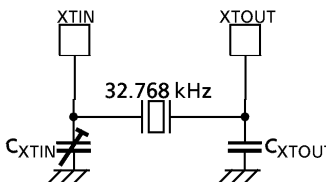


(3) 400 kHz

Ceramic Resonator

CSB400B (MURATA)  $C_{XIN} = C_{XOUT} = 220\text{ pF}$ ,  $R_{XOUT} = 6.8\text{ k}\Omega$

KBR-400B (KYOCERA)  $C_{XIN} = C_{XOUT} = 100\text{ pF}$ ,  $R_{XOUT} = 10\text{ k}\Omega$



(4) 32.768 kHz ( $V_{SS} = 0\text{ V}$ ,  $V_{DD} = 2.7\text{ to }6.0\text{ V}$ ,  $T_{opr} = -30\text{ to }70\text{ }^\circ\text{C}$ )

Crystal Oscillator

$C_{XTIN}$ ,  $C_{XTOUT}$ ; 10 to 33 pF

Note: In order to get the accurate oscillation frequency, the adjustment of capacitors must be required.

TYPICAL CHARACTERISTICS

