MOTOROLA

4-Bit D Flip-Flop

Military 100E531

Product Preview

ELECTRICALLY TESTED PER:
100E531

The 100E531 is a quad master-slave D-type flip-flop with differential outputs. Each flip-flop may be clocked separately by holding Common Clock (C_C) LOW and using the Clock Enable ($\overline{CE}$) inputs for clocking. Common clocking is achieved by holding the $\overline{CE}$ inputs LOW and using C_C to clock all four flip-flops. In this case, the $\overline{CE}$ inputs perform the function of controlling the common clock, to each flip-flop.

Individual asynchronous resets are provided (R). Asynchronous set controls (S) are ganged together in pairs, with the pairing chosen to reflect physical chip symmetry.

Data enters the master when both C_C and $\overline{CE}$ are LOW, and transfers to the slave when either C_C or $\overline{CE}$ (or both) go HIGH.

- 1100 MHz Min. Toggle Frequency
- Differential Outputs
- Individual and Common Clocks
- Individual Resets (asynchronous)
- Paired Sets (asynchronous)
- Extended 100E V_{EE} Range of - 4.2 V to - 5.46 V
- 75 kΩ Input Pulldown Resistors

AVAILABLE AS

1) JAN: N/A
2) SMD: N/A
3) 883: Planned
X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: X

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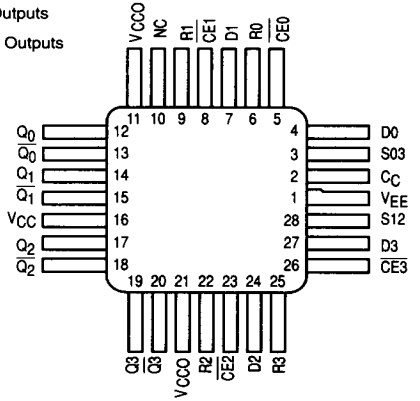
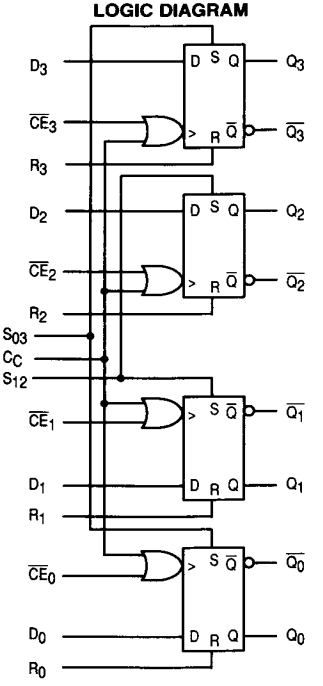
PIN NAME

Pin	Function
D_0 - D_3	Data Inputs
$\overline{CE_0}$ - $\overline{CE_3}$	Clock Enables (Individual)
R_0 - R_3	Resets
C_C	Common Clock
S_{03}, S_{12}	Sets (Paired)
Q_0 - Q_3	True Outputs
$\overline{Q_0}$ - $\overline{Q_3}$	Inverting Outputs



LOGIC DIAGRAM



This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

100E Series DC CHARACTERISTICS: V_{EE} = -4.2 V to - 5.46 V, $V_{CC} = V_{CCO}$ = GND; -55°C to + 125°C

Symbol	Parameter	Min	Max	Units	TEST CONDITION APPLIED:	
V_{OH}	Output HIGH Voltage	-1025	-880	mV	$V_{IN} = V_{IH(max)}$	Loading with
V_{OL}	Output LOW Voltage	-1810	-1620	mV	or $V_{IN} = V_{IL(min)}$	50Ω to -2.0 V
V_{OHA}	Output HIGH Voltage	-1035		mV	$V_{IN} = V_{IH(min)}$	Loading with
V_{OLA}	Output LOW Voltage		-1610	mV	or $V_{IN} = V_{IL(max)}$	50Ω to -2.0 V
V_{IH}	Input HIGH Voltage	-1165	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		µA	$V_{IN} = V_{IL(min)}$	

DC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		− 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current							µA	
	C_C		350		350		350		
	S		450		450		450		
	R		300		300		300		
	$\overline{CE}$		300		300		300		
	D		150		150		150		
I_{EE}	Power Supply Current		70		81		70	mA	

AC CHARACTERISTICS: $V_{EE} = V_{EE(min)}$ to $V_{EE(max)}$, $V_{CC} = V_{CCO}$ = GND

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
	Functional Parameters:	+ 25° C		+ 125° C		− 55° C			
		Min	Max	Min	Max	Min	Max		
f_{MAX}	Max. Toggle Frequency	1100		1100		1100		MHz	
t_{PLH} t_{PHL}	Propagation Delay to Output								
	$\overline{CE}$	360	700	360	700	360	700	ps	
	C_C	325	675	325	675	325	675	ps	
	R	350	725	350	725	350	725	ps	
	S	350	725	350	725	350	725	ps	
t_S	Setup Time								
	D	150		150		150		ps	(Note 2)
t_H	Hold Time								
	D	175		175		175		ps	(Note 2)
t_{RR}	Reset Recovery Time	400		400		400		ps	
t_{Skew}	Within-device Skew	60		60		60		ps	(Note 1)
t_{PW}	Minimum Pulse Width								
	Clk, S, R	400		400		400		ps	
t_r t_f	Rise/Fall Times 20 - 80%	300	675	300	675	300	675	ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.
2. Setup/hold time guaranteed for both C_C & $\overline{CE}$.

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