Alcatel 1964 TRX
SDH / SONET integrated modules
SERDES Transceiver (Transponder) STM-64 / OC-192

Description

These SERDES Transceivers are intended to be used at 10 Gbit/s optical SDH and SONET bit rate and provide electrical accesses at lower 622 Mbit/s bit rate. The modules are housed in a space-saving 300-pin package, providing the same electrical access for overall applications. The transmitter side contains an in-house cooled EA-ILM laser with a laser driver and temperature control loop. The transmit path starts with 16 : 1 serializer Asic. The receiver contains an in-house III-V PIN detector with preamplifier in a front-end module, a main amplifier Asic, a clock and data recovery function with accurate decision circuit. The receive path ends with 1 : 16 deserializer Asic. The Alcatel 1964 TRX family is a range of SERDES transceivers modules, providing convenient and flexible optical interfaces for SDH / SONET systems operating at 9.95 Gbit/s or 10.709 Gbit/s and exceed the applicable ITU-T G.691, Telcordia GR-253-ed.3 and Optical Interworking Forum OIF99.102 standards.

Features

- New International Standard
- Multisource Optical Interfaces
- Upward compatibility with the different features
- Applications:
  Short-Reach or Intra-Office (25 km) and Intermediate-Reach or Short-Haul (40 km)
- Optical 9.95 Gbit/s rate or 10.709 Gbit/s rate (FEC)
- Electrical 622 Mbit/s rate or 669 Mbit/s rate (FEC)
- Operating at 1.5 µm wavelength
- Full performance in operating case temperature from - 5 to + 65 °C
- Space-saving package : 3.5 inch x 4 inch (8.9 cm x 10.16 cm)
- Alcatel Reliability and Qualification Program for built in quality

Transmitter:
- EA-ILM 1.5µ cooled laser
- Up to +2 dBm optical output
- 16x2 input data 622 Mbit/s LVDS
- 1x2 ref. clock 155 or 622 MHz PECL compatible
- Shut down command
- Analog monitoring
- Digital alarms
- Power supplies: +5 V, - 5 V & + 3.3 V
- Power consumption: 4.2 W typical

Receiver:
- InGaAs PIN-preamp detector
- High typical sensitivity - 15 dBm
- 16x2 output data 622 Mbit/s LVDS
- 1x2 ref. clock 155 MHz PECL compatible
- Analog monitoring
- Digital alarms
- Power supplies: +5 V, - 5 V & + 3.3 V
- Power consumption: 2.8 W typical

Applications

Used in transmission systems from high-speed for intermediate-reach to long-reach applications, the Alcatel 1900 TRX family operates at SONET OC-192 rates as well as at ITU-T SDH STM-64 rates. Covering all types of SDH / SONET optical interfaces (tributaries and aggregates) the Alcatel 1900 TRX modules are suitable for line systems, Add Drop Multiplexers and digital cross-connects as well as ATM or IP switches and routers.

As part of the global Alcatel 1900 TRX family, the Alcatel 1964 TRX Short-Haul module is the first version for all types of STM-64 (Intra-office, Short-Haul and Long-Haul) and OC-192 (Short-Reach, Intermediate-Reach and Long-Reach) optical interfaces. These modules ensure ease of use and offer new flexibility to get 10 Gbit/s optical links to system designers.

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Optical characteristics

	Condition	Symb	Min	Typ	Max	Min	Typ	Max	Unit
			I-64.2 / SR-2			S-64.2b / IR-2			
Target distance	Note 1			25			40		Km
Optical budget	Note 1		0		7	3		11	dB
Dispersion	Note 1				500			800	ps/nm
Path penalty					2			2	dB
Transmitter									
Center wavelength		λc	1530	1550	1565	1530	1550	1565	nm
Optical output power	Note 3	S_{NOM}	- 5		- 1	- 1		+ 2	dBm
Spectral width	Note 4	$\Delta\lambda$			1			1	nm
SMSR			30			30			dB
Extinction ratio	Note 5	Er	8.2			8.2			dB
Shutdown optical power		S_{IDLE}		-50	-40		-50	-40	dBm
Generated jitter	Note 2				0.1			0.1	Ulpp
Return loss					24			24	dB
Receiver									
Receiver sensitivity	Note 6	R_{NOM}	- 14	- 15		- 14	- 15		dBm
Receiver overload	Note 6	R_{NOM}	- 1			- 1			dBm
Generated jitter	Note 2				0.1			0.1	Ulpp
Reflectance					- 27			- 27	dB

Note 1: Optical budgets are defined based on Telcordia GR-253-ed.3 & ITU-T G.691.
Note 2: From 50 kHz to 80 MHz bandwidth and no jitter on TxREFCLK.
Note 3: Measured at connector interface.
Note 4: The maximum full width of the central wavelength peak; measured 20 dB down from the maximum amplitude under modulation condition NRZ at 9.95328 Gbit/s and PRBS 2^{23}-1.
Note 5: Measured at connector interface under modulation conditions NRZ at 9.95328 Gbit/s and PRBS 2^{23}-1.
Note 6: Measured at BER 10^{-12} and under modulation conditions NRZ at 9.95328 Gbit/s and PRBS 2^{23}-1
All parameters are specified End-of-Life within the overall relevant operating temperature range.
The typical values are referenced to + 25 °C, nominal power supply, beginning of life.

Electrical characteristics

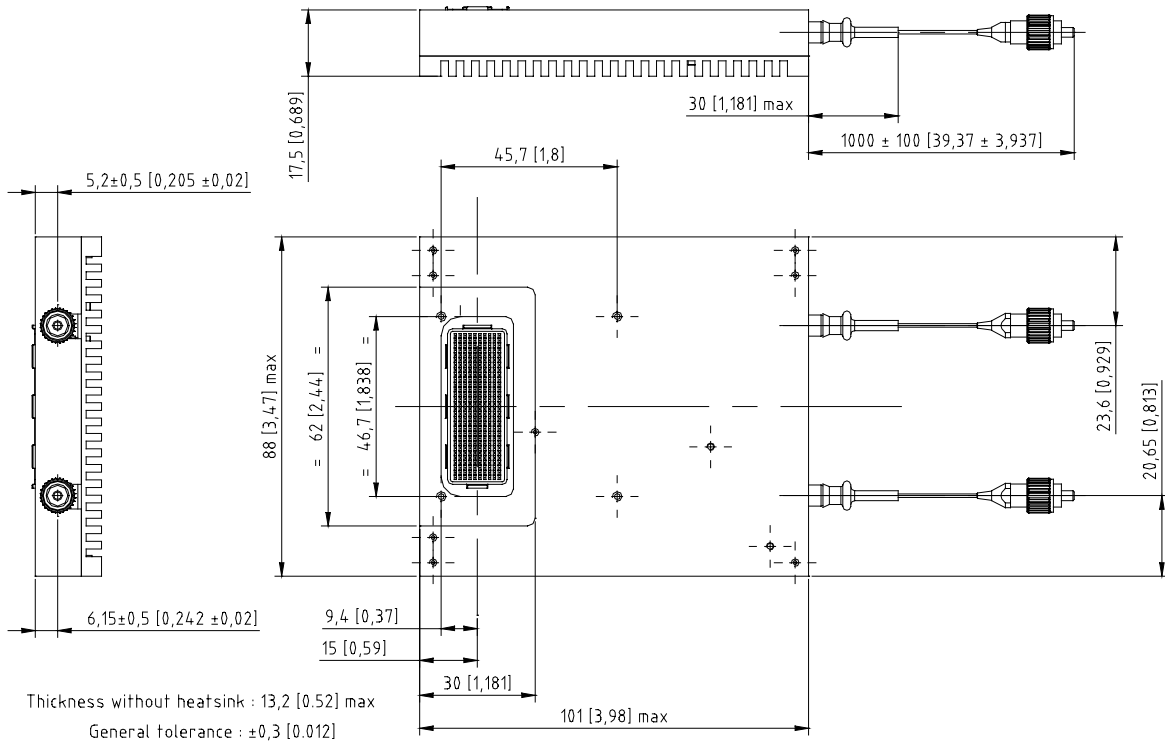| Parameter	Condition	Symbol	Min	Typical	Max	Unit
Negative supply voltage		V_{EE}	- 4.94	- 5.2	- 5.45	V
Negative supply current		I_{EE}		900	1300	mA
1st Positive supply voltage		V_{DD}	3.13	3.3	3.47	V
1st Positive supply current		I_{DD}		760	2000	mA
2nd Positive supply voltage		V_{CC}	4.75	5.0	5.25	V
2nd Positive supply current		I_{CC}		130	200	mA
Power dissipation	Total			7.0	14	W
Common mode LVDS input voltage		$LVDS_{VI}$	800		1700	mV
Differential LVDS input swing		$LVDS_{VIDTH}$	100		1000	mV
LVDS output differential voltage	Note 7	$LVDS_{VOD}$	250		600	mVpp
LVDS differential input impedance		$LVDS_{RIN}$	80		120	Ω
LVTTL input low voltage		$LVTTL_{VIL}$	0		0.8	V
LVTTL input high voltage		$LVTTL_{VIH}$	2.0		3.3	V
LVTTL input low current	$V_{IN} = 0.5$ V	$LVTTL_{IIL}$	-500			µA
LVTTL input high current	$V_{IN} = 2.4$ V	$LVTTL_{IIH}$			50	µA
LVTTL output low voltage	$I_{OL} = 4$ mA	$LVTTL_{VOL}$			0.4	V
LVTTL output high voltage	$I_{OH} = -100$ µA	$LVTTL_{VOH}$	2.4			V
LVPECL differential input voltage swing	Note 8	$LVPECL_{VDIF}$	300		930	mV

Note 7: Peak to peak single ended voltage.
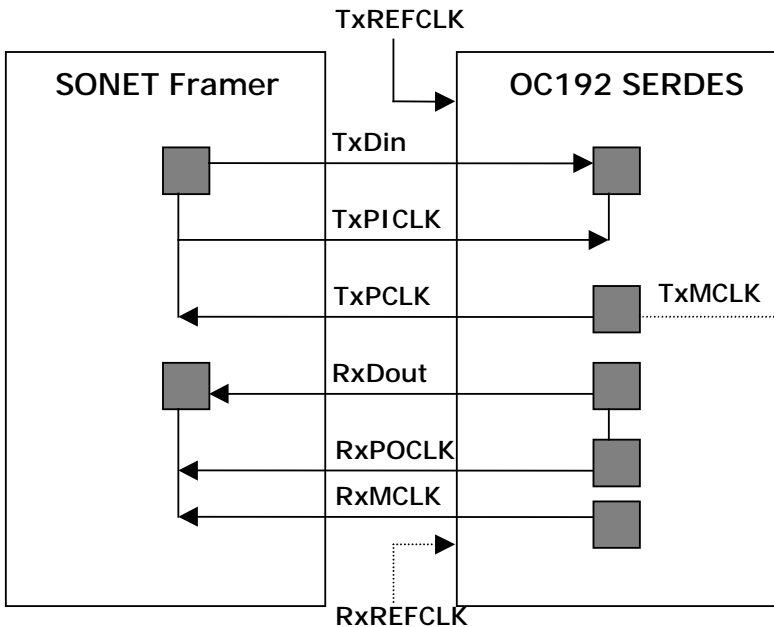Note 8: Internally AC coupled
All parameters are specified End-of-Life within the overall relevant operating temperature range. The typical values are referenced to + 25 °C, nominal power supply, beginning of life.

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Outline drawing

30 [1,181] max

1000 ± 100 [39,37 ± 3,937]

17,5 [0,689]

45,7 [1,8]

5,2±0,5 [0,205 ±0,02]

88 [3,47] max

62 [2,44]

46,7 [1,838]

23,6 [0,929]

20,65 [0,813]

6,15±0,5 [0,242 ±0,02]

9,4 [0,37]

15 [0,59]

30 [1,181]

101 [3,98] max

Thickness without heatsink : 13,2 [0.52] max

General tolerance : ±0,3 [0.012]

Framer to Transceiver clocking

TxREFCLK

SONET Framer

OC192 SERDES

TxDin

TxPICLK

TxPCLK — TxMCLK

RxDout

RxPOCLK

RxMCLK

RxREFCLK

Clocking definition

TxREFCLK	Transmitter Reference Clock Input: Differential clock PECL compatible input, internally AC coupled with 50 Ω terminated.
TxDin	Transmitter Parallel Data Input: Differential 622 Mbit/s LVDS input, internally 100 Ω differential terminated.
TxPICLK	Transmitter Reference Parallel Clock Input: Differential clock LVDS input, internally 100 Ω differential terminated.
TxPCLK	Transmitter Reference Parallel Clock Output: Differential clock LVDS output.
TxMCLK	Transmitter Monitor Clock: LVDS clock output signal. This signal represents the synthesized frequency of the serializer.
RxDout	Receiver Parallel Data Output: Differential 622 Mbit/s LVDS output.
RxPOCLK	Receiver Reference Parallel Clock Output: Differential clock LVDS output.
RxMCLK	Receiver Monitor Clock: Differential LVDS output signal. This signal represents the PLL VC0 clock.
RxREFCLK	Receiver Reference Clock Input: Differential clock PECL compatible input.

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Pin out from customer line card

	K	J	H	G	F	E	D	C	B	A	
1	Rx+5VA	FFU	FGND	RxDout12P	FFU	RxDout8P	RxDigGND	RxDout4P	RxDigGND	RxDout0P	Receiver
2	Rx+5VA	FFU	FGND	RxDout12N	FFU	RxDout8N	RxDigGND	RxDout4N	RxDigGND	RxDout0N	
3	RxRATESEL	FFU	FFU	RxDigGND	RxPOWMON	RxDigGND	FFU	RxDigGND	FFU	RxDigGND	
4	Rx3.3VA	NUC	FGND	RxDout13P	Rx3.3VD	RxDout9P	RxDigGND	RxDout5P	RxDigGND	RxDout1P	
5	Rx3.3VA	NUC	FGND	RxDout13N	Rx3.3VD	RxDout9N	RxDigGND	RxDout5N	RxDigGND	RxDout1N	
6	RxRESET	NUC	FFU	RxDigGND	RxPOWALM	RxDigGND	FFU	RxDigGND	FFU	RxDigGND	
7	FFU	FFU	RxAGND	RxDout14P	Rx3.3VD	RxDout10P	RxDigGND	RxDout6P	RxDigGND	RxDout2P	
8	FFU	FFU	RxAGND	RxDout14N	Rx3.3VD	RxDout10N	RxDigGND	RxDout6N	RxDigGND	RxDout2N	
9	FFU	NUC	FFU	RxDigGND	FFU	RxDigGND	FFU	RxDigGND	RxLCKREF	RxDigGND	
10	Rx-5.2VA	FFU	RxAGND	RxDout15P	Rx-5.2VD	RxDout11P	RxDigGND	RxDout7P	RxDigGND	RxDout3P	
11	Rx-5.2VA	FFU	RxAGND	RxDout15N	Rx-5.2VD	RxDout11N	RxDigGND	RxDout7N	RxDigGND	RxDout3N	
12	FFU	NUC	FFU	RxDigGND	FFU	RxDigGND	FFU	RxDigGND	FFU	RxDigGND	
13	Rx-5.2VA	FFU	RxAGND	FFU	Rx-5.2VD	RxPOCLKP	RxDigGND	RxMCLKP	RxDigGND	RxREFCLKP	
14	Rx-5.2VA	FFU	RxAGND	FFU	Rx-5.2VD	RxPOCLKN	RxDigGND	RxMCLKN	RxDigGND	RxREFCLKN	
15	FFU	NUC	TBD	RxDigGND	FFU	RxDigGND	FFU	RxDigGND	RxLOCKERR	RxDigGND	
16	Tx+5VA	FFU	TxAGND	TxDin12P	FFU	TxDin8P	TxDigGND	TxDin4P	TxDigGND	TxDin0P	Transmitter
17	Tx+5VA	FFU	TxAGND	TxDin12N	FFU	TxDin8N	TxDigGND	TxDin4N	TxDigGND	TxDin0N	
18	FFU	NUC	FFU	TxDigGND	LsBIASMON	TxDigGND	LsPOWMON	TxDigGND	TxSKEWSEL0	TxDigGND	
19	Tx3.3VA	FFU	TxAGND	TxDin13P	Tx3.3VD	TxDin9P	TxDigGND	TxDin5P	TxDigGND	TxDin1P	
20	Tx3.3VA	FFU	TxAGND	TxDin13N	Tx3.3VD	TxDin9N	TxDigGND	TxDin5N	TxDigGND	TxDin1N	
21	TxRATESEL	FFU	FFU	TxDigGND	LsENABLE	TxDigGND	LsTEMPMON	TxDigGND	TxSKEWSEL1	TxDigGND	
22	Tx3.3VA	FFU	TxAGND	TxDin14P	Tx3.3VD	TxDin10P	TxDigGND	TxDin6P	TxDigGND	TxDin2P	
23	Tx3.3VA	FFU	TxAGND	TxDin14N	Tx3.3VD	TxDin10N	TxDigGND	TxDin6N	TxDigGND	TxDin2N	
24	TxRESET	NUC	FFU	TxDigGND	LsBIASALM	TxDigGND	FFU	TxDigGND	FFU	TxDigGND	
25	Tx-5.2VA	NUC	FGND	TxDin15P	Tx-5.2VD	TxDin11P	TxDigGND	TxDin7P	TxDigGND	TxDin3P	
26	Tx-5.2VA	NUC	FGND	TxDin15N	Tx-5.2VD	TxDin11N	TxDigGND	TxDin7N	TxDigGND	TxDin3N	
27	FFU	NUC	FFU	TxDigGND	LsTEMPALM	TxDigGND	FFU	TxDigGND	TxPICLKSEL	TxDigGND	
28	Tx-5.2VA	FFU	FGND	TxPICLKP	Tx-5.2VD	TxPCLKP	TxDigGND A	Tx155MCKP	TxDigGND	TxREFCLKP	
29	Tx-5.2VA	FFU	FGND	TxPICLKN	Tx-5.2VD	TxPCLKN	TxDigGND	Tx155MCKN	TxDigGND	TxREFCLKN	
30	FFU	NUC	FFU	TxDigGND	TxREFSEL	TxDigGND	FFU	TxDigGND	TxLOCKERR	TxDigGND	

Receiver power & GND supplies	Transmitter power & GND supplies	NUC — No User Connection
Receiver d.c. signals	Transmitter d.c. signals	FFU — Reserve For Future Use
622 differential signals	622 differential signals	

Receiver pin description

RxDout##P Receiver NRZ Data Output Positive: 622 Mbit/s LVDS output signal. Data are synchronized at the output of the module with the output clock RxPOCLK signal. RxDout15 is the most significant bit and first bit received.

RxDout##N Receiver NRZ Data Output Negative: 622 Mbit/s LVDS output signal. Data are synchronized at the output of the module with the output clock RxPOCLK signal. RxDout15 is the most significant bit and first bit received.

RxPOCLKP Receiver Parallel Output Clock Positive: 622 MHz LVDS output. Regenerated clock synchronized to the data. The falling edge of RxPOCLKP is in the middle of the data pattern.

RxPOCLKN Receiver Parallel Output Clock Negative: 622 MHz output signal. Regenerated clock synchronized to the data. The rising edge of RxPOCLKN is in the middle of the data pattern.

RxREFCLKP Receiver Reference Clock Positive: 155 MHz PECL, compatible, internally AC coupled 50 Ω terminated.

RxREFCLKN Receiver Reference Clock Negative: 155 MHz PECL, compatible, internally AC coupled 50 Ω terminated.

RxMCLKP Receiver Monitor Clock Positive: 622 MHz LVDS output signal. This signal represents the PLL VC0 clock.

RxMCLKN Receiver Monitor Output Clock Negative: 622 MHz LVDS output signal. This signal represents the PLL VC0 clock.

RxLCKREF Receiver Lock Clock Reference: LVTTL input command. Selects the reference frequency mode of RxPOCLK. When is at logic low, the RxPOCLK is forced to lock to the RxREFCLK. When at logic high, the RxPOCLK is locked to the CDR reference clock.

RxRESET Receiver deserializer RESET: LVTTL input command. When at logic low, the deserializer function is reinitialized.

RxPOWMON Receiver Power Monitoring: analog output monitor. This voltage is proportional to the mean optical input power. Typical slope is 1 V / mW from –1 to–17dBm.

RxPOWALM Receiver Power Alarm: LVTTL output alarm. Set to logic low when the incoming optical power is less than –17dBm+/-2dB.

RxLOCKERR Receiver Loss of Clock Error: LVTTL output alarm. Set to logic low when the clock recovery is not locked onto the optical data stream. Set to logic high in normal operation.

RxRATESEL Receiver rate Selection : LVTTL input command. Selects the bit rate. When is at logic high, the standard 9.95328Gbits/s bit rate is selected, if it's logic low the FEC bit rate 10.709Gbit/s is selected. Note that in this case the RxREFCLK frequency has to be 167.328MHz.

FFU Reserve For Future Use.

NUC No User Connection.

Transmitter pin description

TxDin##P — Transmitter NRZ Data Input Positive: 622 Mbit/s LVDS input signal. Data are retimed at the input of the module by the input clock TxPICLK signal. TxDin15 is the most significant and the first bit transmitted

TxDin##N — Transmitter NRZ Data Input Negative: 622 Mbit/s LVDS input signal. Data are retimed at the input of the module by the input clock TxPICLK signal. TxDin15 is the most significant and the first bit transmitted.

TxPICLKP — Transmitter Parallel Input Clock Positive: 622 MHz or 311 MHz LVDS input signal. When TxPICLKSEL is at logic low, the frequency has to be 622 MHz and the rising edge of TxPICLKN is in the middle of the data pattern. When TxPICLKSEL is at logic high, the frequency has to be 311 MHz and the rising/falling edges of TxPICLKN are in the middle of the data crossing point.

TxPICLKN — Transmitter Parallel Input Clock Negative: 622 MHz or 311 MHz LVDS input signal. When TxPICLKSEL is at logic low, the frequency has to be 622 MHz and the falling edge of TxPICLKN is in the middle of the data pattern. When TxPICLKSEL is at logic high, the frequency has to be 311 MHz and the falling edge of TxPICLKN is in the middle of the data crossing point.

TxPCLKP — Transmitter Parallel Clock output Positive: 622 MHz LVDS output signal. Reference clock generated from the TxREFCLK signal. Usable to synchronize the output data stage of the framer ASIC.

TxPCLKN — Transmitter Parallel Clock output Negative: 622 MHz LVDS output signal. Reference clock generated from the TxREFCLK signal. Usable to synchronize the output data stage of the framer ASIC.

TxREFCLKP — Transmitter Reference Clock Positive: 622 MHz or 155 MHz PECL compatible input signal. When TxREFSEL0 is at logic low, the frequency is 155 MHz. When RxREFSEL0 is at logic high, the frequency is 622 MHz.

TxREFCLKN — Transmitter Reference Clock Negative: 622 MHz or 155 MHz PECL compatible input signal. When TxREFSEL0 is at logic low, the frequency is 155 MHz. When RxREFSEL0 is at logic high, the frequency is 622 MHz.

TxMCLKP — Transmitter Monitor Clock Positive: 155 MHz LVDS clock output signal. This signal represents the synthesized frequency of the serializer.

TxMCLKN — Transmitter Monitor Clock Negative: 155 MHz LVDS clock output signal. This signal represents the synthesized frequency of the serializer.

TxPICLKSEL — Transmitter Parallel Clock Select: LVTTL input command. Selects the reference frequency mode of TxPICLK. When at logic low, the frequency has to be 622 MHz. When at logic high, the frequency has to be 311 MHz.

TxREFSEL — Transmitter Reference clock Select : LVTTL input command. Selects the reference frequency mode of TxREFCLK. When at logic low, the frequency is 155 MHz. When at logic high, the frequency is 622 MHz.

TxSKEWSEL0 — Transmitter Adjusts Skew of TxPICLK Select: LVTTL input command. This LSB digital logic input allows delaying internally the TxPICLK in the 311 MHz mode.

TxSKEWSEL1 — Transmitter Adjusts Skew of TxPICLK Select: LVTTL input command. This MSB digital logic input allows delaying internally the TxPICLK in the 311 MHz mode.

TxRATESEL — Transmitter Rate Selection: LVTTL input command. Selects the bit rate. When is at logic high, the standard 9.95328Gbits/s bit rate is selected, if it's logic low the FEC bit rate 10.709Gbit/s is selected. Note that in this case the TxREFCLK frequency has to be 167.328MHz or 669.312MHz.

TxRESET — Transmitter serializer RESET: LVTTL input command. When at logic low, the serializer function is reinitialized.

LsENABLE — Laser Enable: LVTTL input command. When at logic high, the laser is disabled. When at logic low, the laser is enabled.

TxLOCKERR — Transmitter Lock Error: LVTTL output alarm. When at logic low, it indicates that the serializer is not locked on the TxREFCLK. When at logic high, the serializer is in normal operating.

LsBIASALM — Laser Bias Alarm: LVTTL output alarm. When at logic low, the laser has reached its end of life condition. When at logic high, the laser is in normal operating.

LsTEMPALM — Laser Temperature Alarm: LVTTL output alarm. When at logic low, the laser temperature is approximately 3°C above or below the normal operating. When at logic high, the laser is in normal operating.

LsBIASMon — Laser Bias Monitoring: analog output monitor. This voltage is proportional to the laser current. The typical slope is 20 mV / mA.

LsPOWMon — Laser Power Monitoring: analog output monitor. This voltage is proportional to the laser output power. Normalized at 0.5V over lifetime, the 50 % drift in output power correlates with a 50 % variation in output voltage.

LsTEMPMon — Laser temperature Monitoring: analog output monitor. This voltage represents the laser temperature deviation. Normalized at 2.5V over lifetime.

FFU — Reserved for further additional features.

NUC — No User Connection. This pin has to be left open.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Maximum optical input power			+ 2	dBm
Negative supply voltage	V_{EE}	- 6	0	V
1st Positive supply voltage	V_{DD}	0	+ 3.6	V
2nd Positive supply voltage	V_{CC}	0	+ 6	V
Control input voltage		0	V_{DD}	V
Digital output voltage		0	V_{DD}	V
Analog output voltage		0	V_{DD}	V
Alarm output voltage		0	V_{DD}	V
Storage temperature	T_{STG}	- 20	+ 70	°C
Storage 72h max		- 40	+ 85	°C
Operating case temperature	T_{OP}	- 5	+ 65	°C

Ordering information

Alcatel 1964 TRX

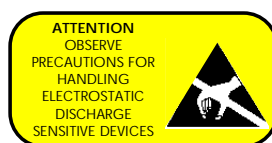|	Dispersion (ps/nm)	Span (km)	Part Number
I-64.2 / SR-2	400	25	3CN 00576 xx
I-64.2 / SR-2 FEC	400	25	3CN 00578 xx
S-64.2b / IR-2	800	40	3CN 00532 xx
S-64.2b / IR-2 FEC	800	40	3CN 00577 xx

Options

3CN xxxxx   xA → FC/PC   Ax → With heat sink
             xB → SC/PC   Bx → Without heat sink

Standards

Compliant with ITU-T G.691
Telcordia GR-253-ed.3
Optical Interworking Forum
OIF99.102
Optical fiber according to ITU-T G.652
Environment according to IEC 68-2 and
MIL STD 883
Telcordia TR-EOP-000063

**LASER RADIATION
AVOID EXPOSURE TO BEAM
Class 3A laser product**

ATTENTION
OBSERVE
PRECAUTIONS FOR
HANDLING
ELECTROSTATIC
DISCHARGE
SENSITIVE DEVICES

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