

Octal D-type transparent latch (3-State)

54ABT373

FEATURES

- 8-bit transparent latch
- 3-State output buffers
- Output capability: +48mA/-24mA
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 54ABT373 high-performance BiCMOS device combines low static and dynamic

power dissipation with high speed and high output drive.

The 54ABT373 device is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

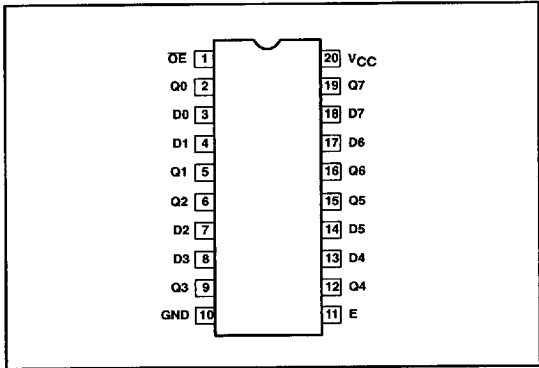
When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

ORDERING INFORMATION

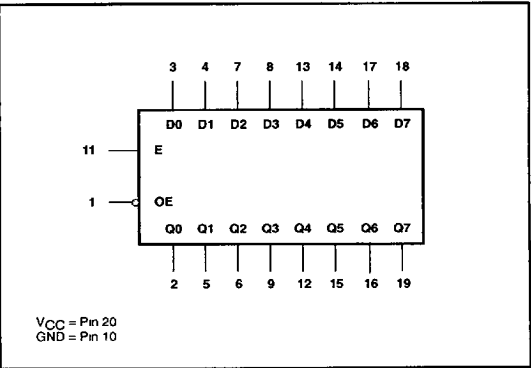
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
20-Pin Ceramic DIP	54ABT373/BRA	GDIP1-T20
20-Pin Ceramic LLCC	54ABT373/B2A	CQCC2-N20

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

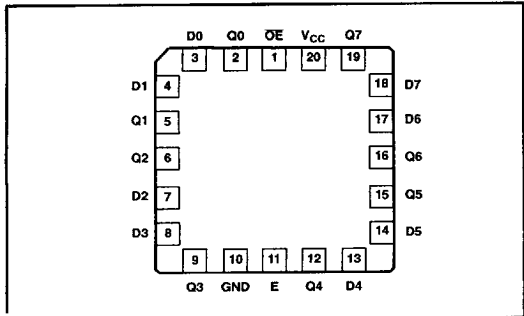
PIN CONFIGURATION



LOGIC SYMBOL



LLCC LEAD CONFIGURATION



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PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output enable input (active Low)
3, 4, 7, 8, 13, 14, 17, 18	D0 - D7	Data inputs
2, 5, 6, 9, 12, 15, 16, 19	Q0 - Q7	3-State outputs
11	E	Enable input (active High)
10	GND	Ground (0V)
20	V _{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS Q0 - Q7	OPERATING MODE
$\overline{OE}$	E	D _n			
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	D _n	D _n	Z	

H = High voltage level

h = High voltage level one setup time prior to the High-to-Low E transition

L = Low voltage level

l = Low voltage level one setup time prior to the High-to-Low E transition

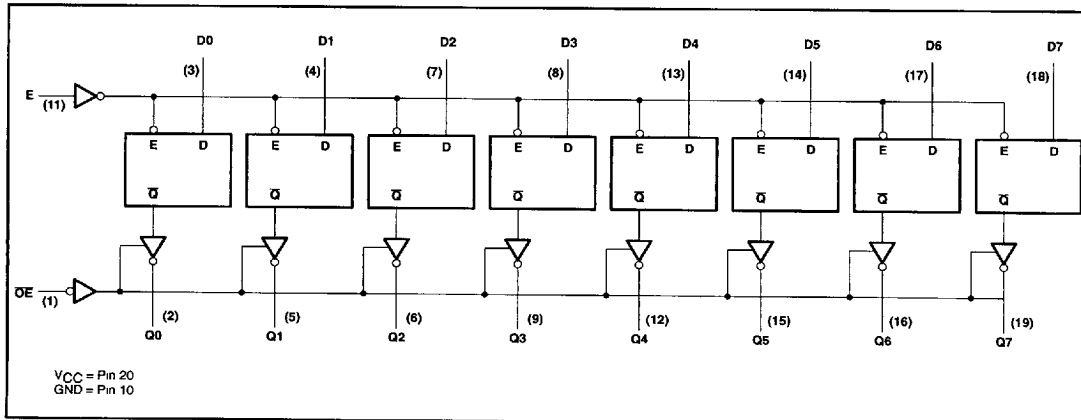
NC = No change

X = Don't care

Z = High impedance "off" state

↓ = High-to-Low E transition

LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage range		-0.5 to +7.0	V
I _{IK}	DC input diode current	V _I < 0	-18	mA
V _I	DC input voltage range ²		-1.2 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _O	DC output voltage range ²	Output in Off or High state	-0.5 to +5.5	V
I _O	DC output current	Output in Low state	96	mA
T _{STG}	Storage temperature range		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V _{CC}	DC supply voltage	4.5	5.5	V
V _I	Input voltage	0	V _{CC}	V
V _{IH}	High-level input voltage	2.0		V
V _{IL}	Low-level input voltage		0.8	V
I _{OH}	High-level output current		-24	mA
I _{OL}	Low-level output current		48	mA
Δt/Δv	Input transition rise or fall rate	0	5	ns/V
T _{amb}	Operating free-air temperature range	-55	+125	°C

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DC ELECTRICAL CHARACTERISTICS

 $V_{CC} = \text{MAX}$, $V_I = V_{IL}$ or V_{IH} unless otherwise noted.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T _{amb} = +25°C			T _{amb} = -55 to +125°C		
			MIN	TYP ²	MAX	MIN	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 4.5V; I _{IK} = -18mA			-1.2		-1.2	V
V _{OH}	High-level output to voltage	V _{CC} = 4.5V; I _{OH} = -3mA	2.5			2.5		V
		V _{CC} = 5.0V; I _{OH} = -3mA	3.0			3.0		V
		V _{CC} = 4.5V; I _{OH} = -24mA	2.0	2.4		2.0		V
V _{OL}	Low-level output voltage	V _{CC} = 4.5V; I _{OL} = 48mA		0.42	0.55		0.55	V
I _I	Input leakage current	V _I = GND or 5.5V		±0.01	±1.0		±1.0	μA
I _{OZH} ⁶	3-State output High current	V _O = 2.7V, V _I = V _{IL} or 3.0V		0.1	10		10	μA
I _{OZL} ⁶	3-State output Low current	V _O = 0.5V, V _I = V _{IL} or 3.0V		-0.1	-10		-10	μA
I _O	Short-circuit output current ⁴	V _O = 2.5V, V _I = GND or V _{CC}	-50	-100	-180	-50	-180	mA
I _{CCH}	Quiescent supply current	Outputs High, V _I = GND or V _{CC}		0.5	250		250	μA
I _{CCL}		Outputs Low, V _I = GND or V _{CC}		24	30		30	mA
I _{CCZ}		Outputs 3-State, V _I = GND or V _{CC}		0.5	250		250	μA
ΔI _{CC}	Additional supply current per input pin ⁵	One input at 3.4V, other inputs at V _{CC} or GND		0.5	1.5		1.5	mA
I _{OFF}	Power OFF leakage current	V _{CC} = 0V, V _I or V _O ≤ 4.5V	-100	1.0	100			μA
I _{CEX}	Output High leakage current	V _{CC} = 5.5V, V _I or V _O = 5.5V			50		50	μA

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AC ELECTRICAL CHARACTERISTICS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = -55°C to +125°C V _{CC} = +5.0V ± 10%		
			MIN	TYP	MAX	MIN	MAX	
t _{PLH} t _{PHL}	Propagation delay Dn to Qn	Waveform 4	1.9 2.2	3.9 4.2	5.4 5.7	1.3 2.0	6.8 7.0	ns ns
t _{PLH} t _{PHL}	Propagation delay E to Qn	Waveform 3	2.6 3.2	4.6 5.2	6.1 6.7	1.8 2.5	7.7 7.7	ns ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	Waveform 6 Waveform 7	1.2 2.0	3.2 4.7	5.5 6.2	1.0 1.5	6.2 7.2	ns ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	Waveform 6 Waveform 7	2.5 2.0	4.9 4.5	6.4 6.0	2.4 2.0	8.0 7.0	ns ns

AC SETUP REQUIREMENTS

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			T _{amb} = +25°C V _{CC} = +5.0V			T _{amb} = -55°C to +125°C V _{CC} = +5.0V ± 10%			
			MIN	TYP	MAX	MIN	MAX		
t _s (H) ⁷ t _s (L) ⁷	Setup time Dn to E	Waveform 5	2.2 2.2			2.5 2.5		ns ns	
t _h (H) ⁷ t _h (L) ⁷	Hold time Dn to E	Waveform 5	2.2 2.2			2.5 2.5		ns ns	
t _w (H) ⁸	E pulse width High or Low	Waveform 3	3.3			3.3		ns	

NOTES:

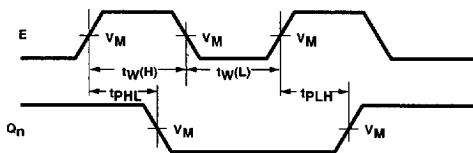
- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C .
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V .
- To accommodate ATE tester limitations, I_{OZ} tests are tested with $V_{\text{IH}} = 3.0\text{V}$, but 2.0V V_{IH} is guaranteed.
- t_{set} and t_{hold} limits that are less than 3.0ns are guaranteed, but are only tested to a 3.0ns limit due to tester limitations.
- t_w limits that are less than 6.0ns are guaranteed, but are only tested to a 6.0ns limit due to tester limitations.

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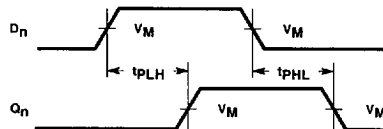
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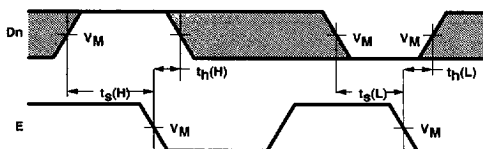
AC WAVEFORMS

 $V_M = 1.5V$, $V_{IN} = GND$ to $3.0V$ 

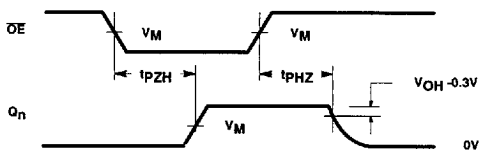
Waveform 3. Propagation Delay, Enable to Output, and Enable Pulse Width



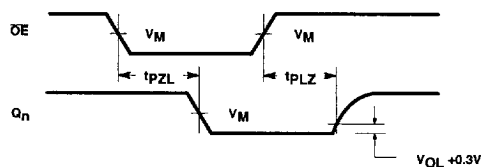
Waveform 4. Propagation Delay Data to Outputs



Waveform 5. Data Setup and Hold Times



Waveform 6. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 7. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

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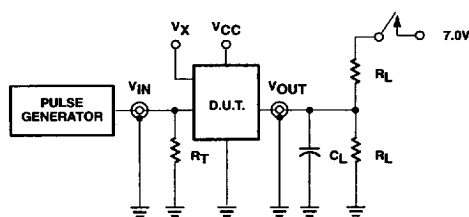
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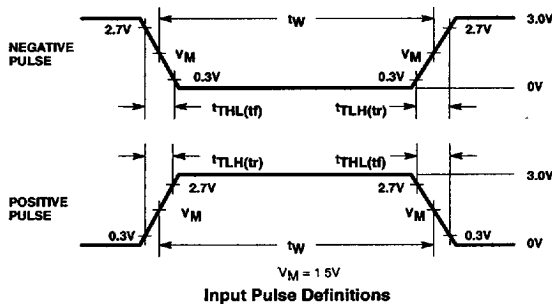
TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ} , t_{PZL}	closed
All other	closed open



INPUT PULSE REQUIREMENTS

Family	Amplitude	Rep. Rate	t_W	t_R	t_F
54ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

DEFINITIONS:

 R_L = Load Resistor; see AC Characteristics for value. C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value. R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.