

54LS273, 54S273 Flip-Flops

Military Logic Products

Octal D Flip-Flops

Product Specification

FEATURES

- Ideal buffer for MOS microprocessor or memory
- Eight edge-triggered D flip-flops
- High-speed Schottky version available
- Buffered common clock
- Buffered, asynchronous Master Reset
- Slim 20-pin plastic and ceramic DIP packages
- See '377 for Clock Enable version
- See '373 for transparent latch version
- See '374 for 3-State version

DESCRIPTION

The '273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset (MR) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the MR input. The device is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

ORDERING INFORMATION

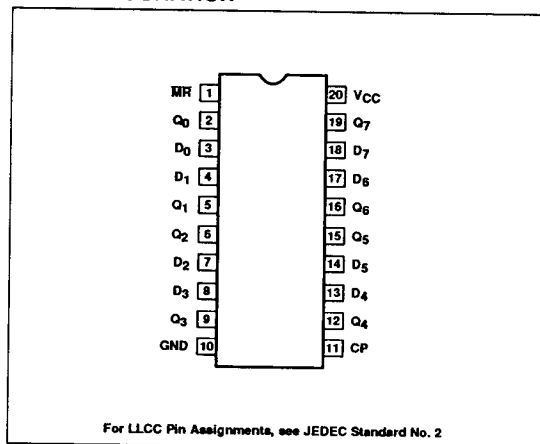
DESCRIPTION	ORDER CODE
20-Pin Ceramic DIP	54LS273/BRA 54S273/BRA
20-Pin Ceramic FlatPack	54LS273/BSA 54S273/BSA
20-Pin Ceramic LLCC	54LS273/B2A 54S273/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

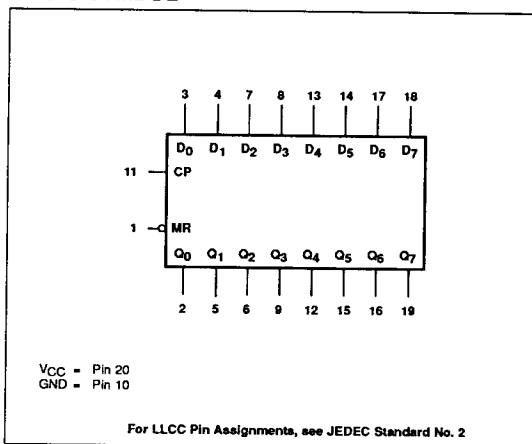
PINS	DESCRIPTION	54S	54LS
All	Inputs	1SUL	1LSUL
All	Outputs	10SUL	10LSUL

NOTE: A 54S Unit Load (SUL) is 50µA I_{IH} and -2.0mA I_{IL} and a 54LS Unit Load (LSUL) is 20µA I_{IH} and -0.4mA I_{IL} .

PIN CONFIGURATION



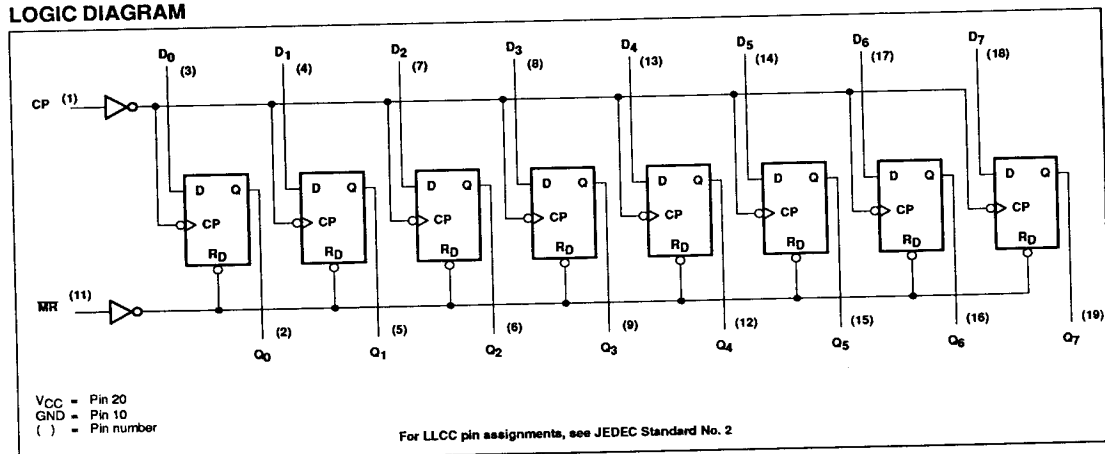
LOGIC SYMBOL



Flip-Flops

54LS273, 54S273

LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS
	MR	CP	D_n	Q_n
Reset (clear)	L	X	X	L
Load "1"	H	↑	h	H
Load "0"	H	↑	l	L

H = High voltage level steady state.

h = High voltage level one setup time prior to the Low-to-High Clock transition.

L = Low voltage level steady state.

l = Low voltage level one setup time prior to the Low-to-High Clock transition.

X = Don't Care.

↑ = Low-to-High clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54LS	54S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +7.0	-0.5 to +5.5	V
I_I	Input current range	-30 to +1	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	-65 to +150	°C

Flip-Flops

54LS273, 54S273

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54LS			54S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			2.0			V
V_{IL}	Low-level input voltage			+0.7			+0.8	V
I_{IK}	Input clamp current			+0.7			+0.7	V
I_{OH}	High-level output current			-18			-18	mA
I_{OL}	Low-level output current			-400			-1000	μ A
I_{OL}	Low-level output current			4			20	mA
T_A	Operating free-air temperature range	-55		+125	-55		+125	$^{\circ}$ C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS ¹	54LS273			54S273			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	
V_{OH}	High-level output voltage	$V_{CC} = \text{Min}, V_{IH} = \text{Min}, V_{IL} = \text{Max}, I_{OH} = \text{Max}$	2.5	3.4		2.5			V
V_O	Low-level output voltage	$V_{CC} = \text{Min}, V_{IH} = \text{Min}, V_{IL} = \text{Max}, I_{OL} = \text{Max}$		0.25	0.4			0.5	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{Min}, I_I = I_{IK}$			0.4			0.45	V
I_{IH2}	Input current at maximum input voltage	$V_{CC} = \text{Max}$ $V_I = 5.5\text{V}$						1.0	mA
I_{IH1}	High-level input current	$V_{CC} = \text{Max}, V_I = 2.7\text{V}$			0.1				mA
I_{IL}	Low-level input current	$V_{CC} = \text{Max}$ $V_I = 0.4\text{V}$			20			50	μ A
I_{IL}	Low-level input current	$V_{CC} = \text{Max}$ $V_I = 0.5\text{V}$			-0.4				mA
I_{OS}	Short-circuit output current ³	$V_{CC} = \text{Max}$	-20			-40		-2.0	mA
I_{CC}	Supply current ⁴ (total)	$V_{CC} = \text{Max}$		17	27		109	150	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}\text{C}, V_{CC} = 5.0\text{V}^5$

74VHC00: 74VHC00, 74VHC02, 74VHC04, 74VHC08, 74VHC14, 74VHC15, 74VHC24, 74VHC25, 74VHC26, 74VHC27, 74VHC30, 74VHC32, 74VHC36, 74VHC37, 74VHC40, 74VHC45, 74VHC47, 74VHC50, 74VHC54, 74VHC59, 74VHC60, 74VHC62, 74VHC66, 74VHC67, 74VHC68, 74VHC70, 74VHC74, 74VHC76, 74VHC86, 74VHC87, 74VHC90, 74VHC93, 74VHC95, 74VHC96, 74VHC97, 74VHC98, 74VHC99							
TYPICAL CHARACTERISTICS: TA = 25 °C, VCC = 5.0V							
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			CL = 15pF		CL = 15pF		
			Min	Max	Min	Max	
tMAX	Maximum clock frequency	Waveform 1	30		75		MHz
tPLH	Propagation delay	Waveform 1		27		15	ns
tPHL	Clock to output			27		15	ns
tPHL	Propagation delay, MR to output	Waveform 2		27		15	ns

Flip-Flops

54LS273, 54S273

AC SETUP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			Min	Max	Min	Max	
$t_{W(L)}$	Clock pulse width (Low)	Waveform 1	20		7.0		ns
t_W	Master Reset pulse width	Waveform 2	20		10		ns
$t_s(H)$	Setup time, High data to CP	Waveform 3	20		5.0		ns
$t_h(H)$	Hold time, High data to CP	Waveform 3	5.0		3.0		ns
$t_s(L)$	Setup time, Low data to CP	Waveform 3	20		5.0		ns
$t_h(L)$	Hold time, Low data to CP	Waveform 3	5.0		3.0		ns
t_{rec}	Recovery time, MR to CP	Waveform 2	25		5.0		ns

AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

AC ELECTRICAL CHARACTERISTICS $T_A = 25^{\circ}\text{C}$, $V_{CC} = 5.0\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			$C_L = 50\text{pF}$		$C_L = 50\text{pF}$		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		75		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		32 32		17.5 17.5	ns ns
t_{PHL}	Propagation delay, MR to output	Waveform 2		32		17.5	ns

AC ELECTRICAL CHARACTERISTICS $T_A = -55^\circ\text{C}$ and $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V}^5$

AC ELECTRICAL CHARACTERISTICS $T_A = -55^{\circ}\text{C}$ and $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V}$							
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			$C_L = 50\text{pF}$		$C_L = 50\text{pF}$		
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	30		75		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Waveform 1		42 42		23 23	ns ns
t_{PLH}	Propagation delay MR to output	Waveform 2		42		23	ns

AC SETUP REQUIREMENTS $T_A = -55^\circ\text{C}$ and $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V}^5$

SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			Min	Max	Min	Max	
$t_{W(L)}$	Clock pulse width (Low)	Waveform 1	20		7.0		ns
t_W	Master Reset pulse width	Waveform 2	20		10		ns
$t_s(H)$	Setup time, High data to CP	Waveform 3	20		5.0		ns
$t_h(H)$	Hold time, High data to CP	Waveform 3	5.0		3.0		ns
$t_s(L)$	Setup time, Low data to CP	Waveform 3	20		5.0		ns
$t_h(L)$	Hold time, Low data to CP	Waveform 3	5.0		3.0		ns
t_{rec}	Recovery time, MR to CP	Waveform 2	25		5.0		ns

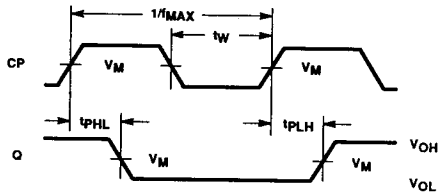
NOTES:

- For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} after a momentary ground, then $\geq 4.0\text{V}$ is applied to clock with all outputs open and $\geq 4.0\text{V}$ applied to all Data inputs and the Master Reset input.
- These parameters are guaranteed, but not tested.

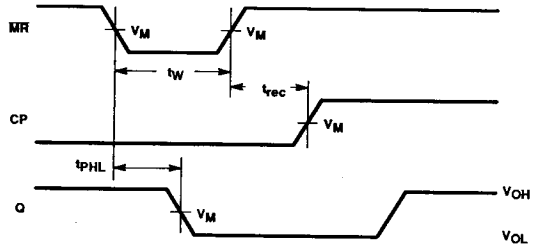
Flip-Flops

54LS273, 54S273

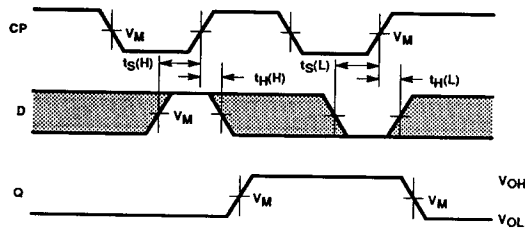
AC WAVEFORMS



Waveform 1. Clock to Output Delays and Clock Pulse Width



Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



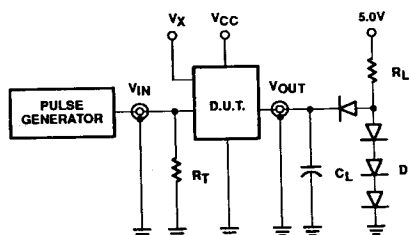
Waveform 3. Data Setup and Hold Times

NOTE: $V_M = 1.5V$ for 54S; $V_M = 1.3V$ for 54LS
The shaded areas indicate when the input is permitted to change for predictable output performance.

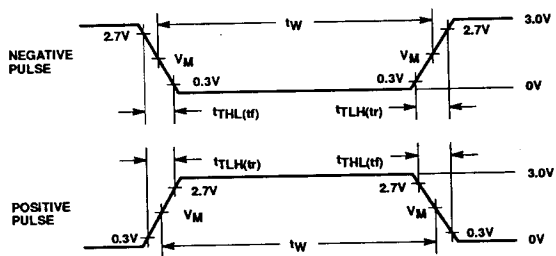
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54LS273, 54S273

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0k Ω	1.3V	1MHz	500ns	≤ 15 ns	≤ 6 ns
54SXXX	280 Ω	1.5V	1MHz	500ns	≤ 2.5 ns	≤ 2.5 ns

DEFINITIONS:

C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

V_X = Unlocked pins must be held at $\leq 0.8V$, $\geq 2.7V$ or open per Function Table.