2.5 V/3.3 V, 2:1 Multiplexer/ Demultiplexer Bus Switch

ADG3248

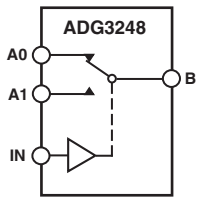
FEATURES

225 ps Propagation Delay through the Switch
4.5 Ω Switch Connection between Ports
Data Rate 1.244 Gbps
2.5 V/3.3 V Supply Operation
Level Translation
3.3 V to 2.5 V
2.5 V to 1.8 V
Small Signal Bandwidth 610 MHz
6-Lead SC70 Package

APPLICATIONS

3.3 V to 2.5 V Voltage Translation
2.5 V to 1.8 V Voltage Translation
Bus Switching
Docking Stations
Memory Switching
Analog Switch Applications

FUNCTIONAL BLOCK DIAGRAM



SWITCHES SHOWN FOR A LOGIC 0 INPUT

GENERAL DESCRIPTION

The ADG3248 is a 2.5 V or 3.3 V, high performance 2:1 multiplexer/demultiplexer. It is designed on a low voltage CMOS process, which provides low power dissipation yet gives high switching speed and very low on resistance. This allows the input to be connected to the output without additional propagation delay or generating additional ground bounce noise.

Each switch of the ADG3248 conducts equally well in both directions when on. The ADG3248 exhibits break-before-make switching action, preventing momentary shorting when switching channels.

The ADG3248 is available in a tiny 6-lead SC70 package.

PRODUCT HIGHLIGHTS

1. 3.3 V or 2.5 V supply operation.
2. Extremely low propagation delay through switch.
3. 4.5 Ω switches connect inputs to outputs.
4. Tiny SC70 package.

REV. 0

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ADG3248–SPECIFICATIONS[1] (V_{CC} = 2.3 V to 3.6 V, GND = 0 V, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Symbol	Conditions	B Version Min	B Version Typ[2]	B Version Max	Unit
DC ELECTRICAL CHARACTERISTICS						
Input High Voltage	V_{INH}	V_{CC} = 2.7 V to 3.6 V	2.0			V
	V_{INH}	V_{CC} = 2.3 V to 2.7 V	1.7			V
Input Low Voltage	V_{INL}	V_{CC} = 2.7 V to 3.6 V			0.8	V
	V_{INL}	V_{CC} = 2.3 V to 2.7 V			0.7	V
Input Leakage Current	I_I			±0.01	±1	µA
OFF State Leakage Current	I_{OZ}	0 ≤ A, B ≤ V_{CC}		±0.01	±1	µA
ON State Leakage Current		0 ≤ A, B ≤ V_{CC}		±0.01	±1	µA
Maximum Pass Voltage	V_P	V_A/V_B = V_{CC} = 3.3 V, I_O = –5 µA	2.0	2.5	2.9	V
		V_A/V_B = V_{CC} = 2.5 V, I_O= –5 µA	1.5	1.8	2.1	V
CAPACITANCE[3]						
A Port Off Capacitance	C_A OFF	f = 1 MHz		3.5		pF
B Port Off Capacitance	C_B OFF	f = 1 MHz		4.5		pF
A, B Port On Capacitance	C_A, C_B ON	f = 1 MHz		8.5		pF
Control Input Capacitance	C_{IN}	f = 1 MHz		4		pF
SWITCHING CHARACTERISTICS[3]						
Propagation Delay A to B or B to A, t_{PD}[4]	t_{PHL}, t_{PLH}	C_L = 50 pF, V_{CC} = 3 V			0.225	ns
Propagation Delay Matching[5]					5	ps
Transition Time	t_{TRANS}	R_L = 510 Ω, C_L = 50 pF		16	29	ns
Break-before-Make Time	t_{BBM}	R_L = 510 Ω, C_L = 50 pF	5	10		ns
Maximum Data Rate		V_{CC} = 3.3 V; V_A/V_B = 2 V		1.244		Gbps
Channel Jitter		V_{CC} = 3.3 V; V_A/V_B = 2 V		45		ps p-p
DIGITAL SWITCH						
On Resistance	R_{ON}	V_{CC} = 3 V, V_A = 0 V, I_{BA} = 8 mA		4.5	8	Ω
		V_{CC} = 3 V, V_A = 1.7 V, I_{BA} = 8 mA		12	28	Ω
		V_{CC} = 2.3 V, V_A = 0 V, I_{BA} = 8 mA		5	9	Ω
		V_{CC} = 2.3 V, V_A = 1 V, I_{BA} = 8 mA		9	18	Ω
On Resistance Matching	ΔR_{ON}	V_{CC} = 3 V, V_A = 0 V, I_A = 8 mA		0.1	0.5	Ω
POWER REQUIREMENTS						
V_{CC}			2.3		3.6	V
Quiescent Power Supply Current	I_{CC}	Digital Inputs = 0 V or V_{CC}		0.01	1	µA

NOTES

[1]Temperature range is as follows: B Version: –40°C to +85°C.

[2]Typical values are at 25°C, unless otherwise stated.

[3]Guaranteed by design, not subject to production test.

[4]The digital switch contributes no propagation delay other than the RC delay of the typical R_{ON} of the switch and the load capacitance when driven by an ideal voltage source. Since the time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the digital switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

[5]Propagation delay matching between channels is calculated from the on resistance matching and load capacitance of 50 pF.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C, unless otherwise noted.)

V_{CC} to GND . . . . . –0.5 V to +4.6 V
Digital Inputs to GND . . . . . –0.5 V to +4.6 V
DC Input Voltage . . . . . –0.5 V to +4.6 V
DC Output Current . . . . . 25 mA per Channel
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
θ_{JA} Thermal Impedance . . . . . 332°C/W
Lead Temperature, Soldering (10 sec) . . . . . 300°C
IR Reflow, Peak Temperature (<20 sec) . . . . . 235°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

PIN CONFIGURATION
6-Lead SC70

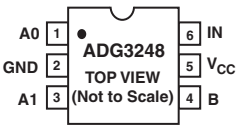


Table I. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	A0	Port A0, Input or Output
2	GND	Ground Reference
3	A1	Port A1, Input or Output
4	B	Port B, Input or Output
5	V_{CC}	Positive Power Supply Voltage
6	IN	Channel Select

Table II. Truth Table

IN	Function
L	B = A0
H	B = A1

ORDERING GUIDE

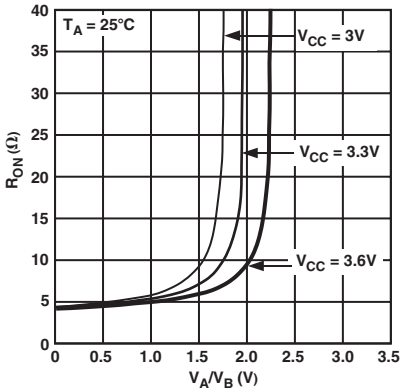
Model	Temperature Range	Package Description	Package	Branding
ADG3248BKS-R2	–40°C to +85°C	SC70 (Thin Shrink Small Outline Transistor Package)	KS-6	SMA
ADG3248BKS-REEL	–40°C to +85°C	SC70 (Thin Shrink Small Outline Transistor Package)	KS-6	SMA
ADG3248BKS-REEL7	–40°C to +85°C	SC70 (Thin Shrink Small Outline Transistor Package)	KS-6	SMA

CAUTION

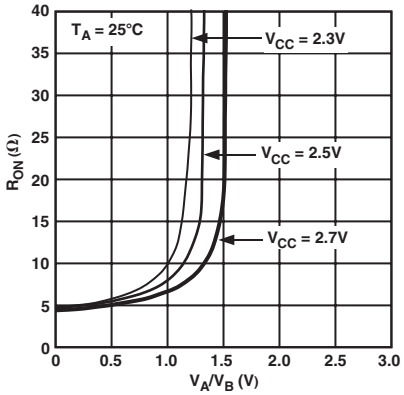
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG3248 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

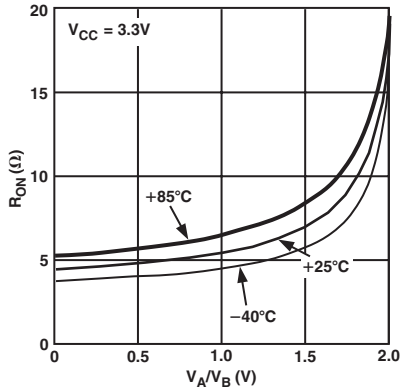
V_{CC}	Positive Power Supply Voltage.
GND	Ground (0 V) Reference.
V_{INH}	Minimum Input Voltage for Logic 1.
V_{INL}	Maximum Input Voltage for Logic 0.
I_I	Input Leakage Current at the Control Inputs.
I_{OZ}	OFF State Leakage Current. It is the maximum leakage current at the switch pin in the OFF state.
I_{OL}	ON State Leakage Current. It is the maximum leakage current at the switch pin in the ON state.
V_P	Maximum Pass Voltage. The maximum pass voltage relates to the clamped output voltage of an NMOS device when the switch input voltage is equal to the supply voltage.
R_{ON}	Ohmic Resistance Offered by a Switch in the ON State. It is measured at a given voltage by forcing a specified amount of current through the switch.
ΔR_{ON}	ON Resistance Match between Any Two Channels, i.e., R_{ON} max – R_{ON} min.
C_X OFF	OFF Switch Capacitance.
C_X ON	ON Switch Capacitance.
C_{IN}	Control Input Capacitance. This consists of IN.
I_{CC}	Quiescent Power Supply Current. This current represents the leakage current between the V_{CC} and ground pins. It is measured when all control inputs are at a logic high or low level and the switches are OFF.
t_{PLH}, t_{PHL}	Data Propagation Delay through the Switch in the ON State. Propagation delay is related to the RC time constant $R_{ON} \times C_L$, where C_L is the load capacitance.
t_{BBM}	On or Off time measured between the 90% points of both switches when switching from one to another.
t_{TRANS}	Time taken to switch from one channel to the other, measured from 50% of the IN signal to 90% of the OUT signal.
Max Data Rate	Maximum Rate at which Data Can Be Passed through the Switch.
Channel Jitter	Peak-to-Peak Value of the Sum of the Deterministic and Random Jitter of the Switch Channel.



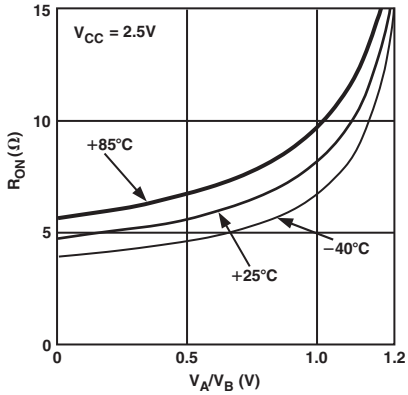
TPC 1. On Resistance vs. Input Voltage



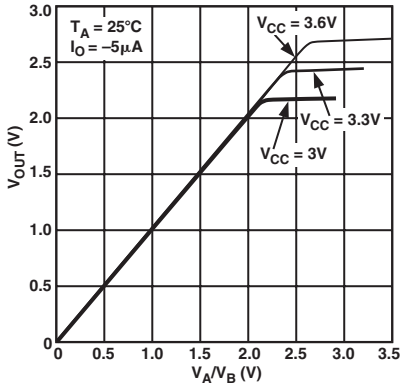
TPC 2. On Resistance vs. Input Voltage



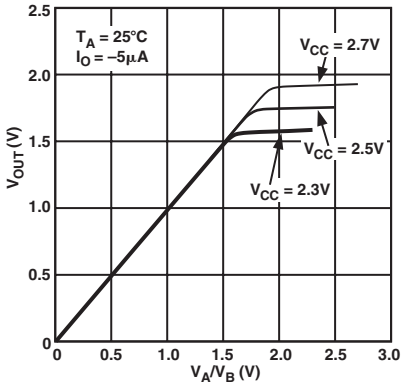
TPC 3. On Resistance vs. Input Voltage for Different Temperatures



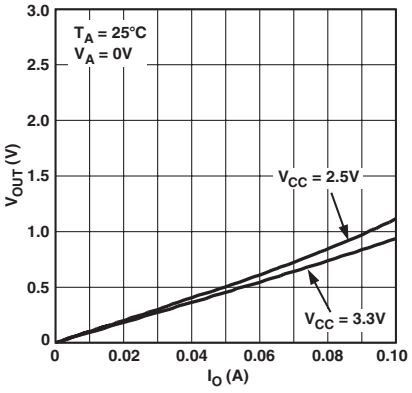
TPC 4. On Resistance vs. Input Voltage for Different Temperatures



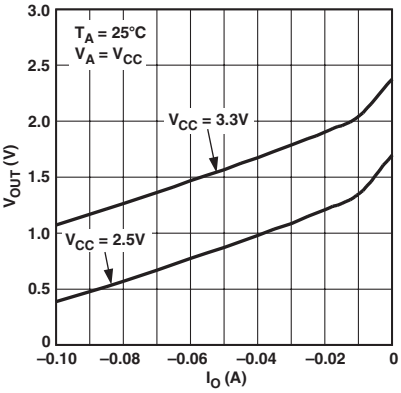
TPC 5. Pass Voltage vs. V_{CC}



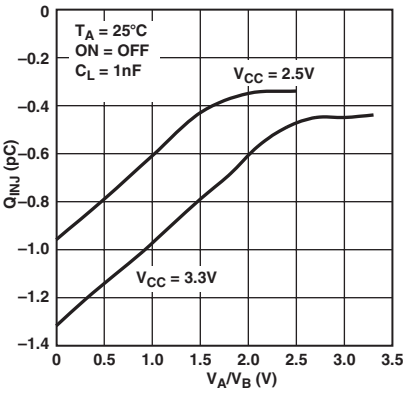
TPC 6. Pass Voltage vs. V_{CC}



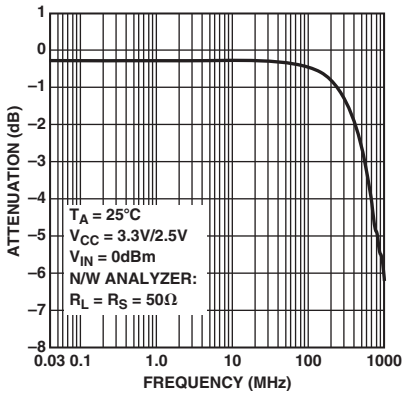
TPC 7. Output Low Characteristic



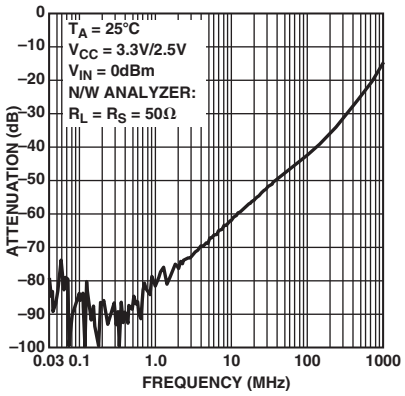
TPC 8. Output High Characteristic



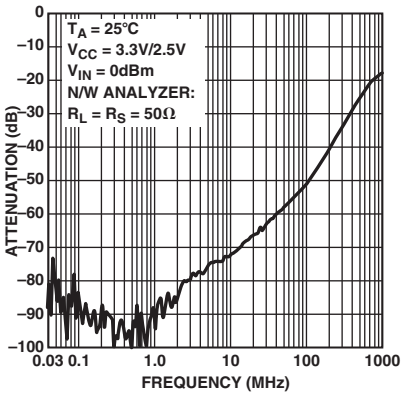
TPC 9. Charge Injection vs. Source Voltage



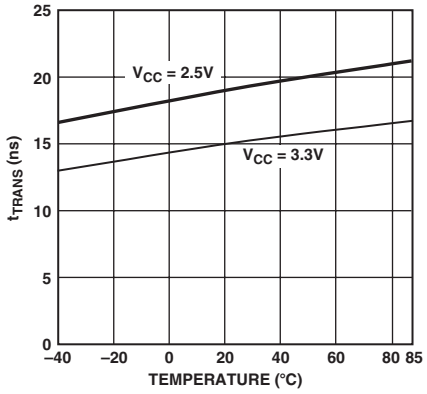
TPC 10. Bandwidth vs. Frequency



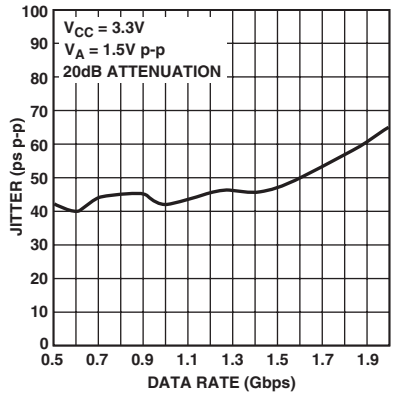
TPC 11. Crosstalk vs. Frequency



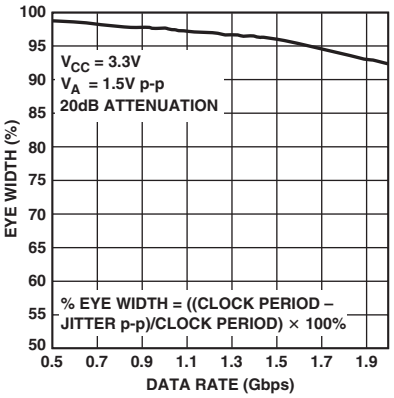
TPC 12. Off Isolation vs. Frequency



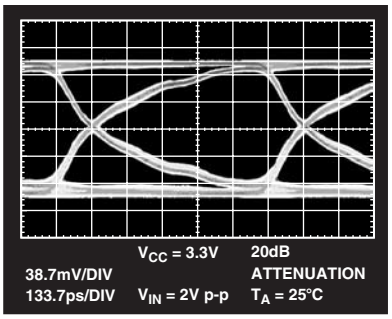
TPC 13. Transition Time vs. Temperature



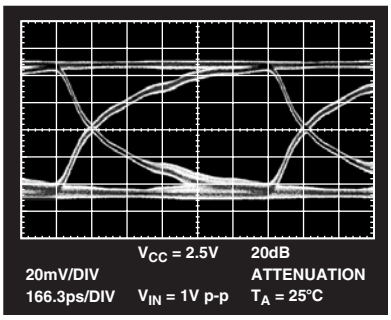
TPC 14. Jitter vs. Data Rate; PRBS 31



TPC 15. Eye Width vs. Data Rate; PRBS 31



TPC 16. Eye Pattern; 1.244 Gbps, V_{CC} = 3.3 V, PRBS 31



TPC 17. Eye Pattern; 1 Gbps, V_{CC} = 2.5 V, PRBS 31

BUS SWITCH APPLICATIONS

Mixed Voltage Operation, Level Translation

Bus switches can provide an ideal solution for interfacing between mixed voltage systems. The ADG3248 is suitable for applications where voltage translation from 3.3 V technology to a lower voltage technology is needed. This device can translate from 2.5 V to 1.8 V, or bidirectionally from 3.3 V directly to 2.5 V.

Figure 1 shows a block diagram of a typical application in which a user needs to interface between a 3.3 V ADC and a 2.5 V microprocessor. The microprocessor may not have 3.3 V tolerant inputs, therefore placing the ADG3248 between the two devices allows the devices to communicate easily. The bus switch directly connects the two blocks, thus introducing minimal propagation delay, timing skew, or noise.

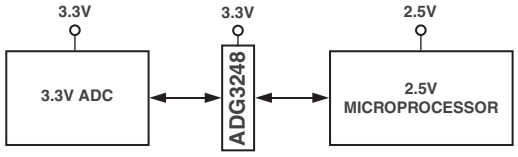


Figure 1. Level Translation between a 3.3 V ADC and a 2.5 V Microprocessor

3.3 V to 2.5 V Translation

When V_{CC} is 3.3 V and the input signal range is 0 V to V_{CC}, the maximum output signal will be clamped to within a voltage threshold below the V_{CC} supply.

In this case, the output will be limited to 2.5 V, as shown in Figure 3. This device can be used for translation from 2.5 V to 3.3 V devices and also between two 3.3 V devices.

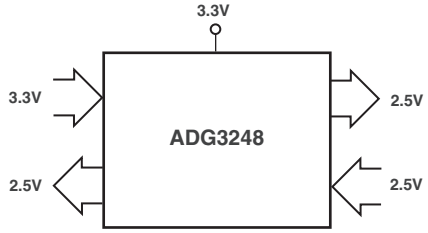


Figure 2. 3.3 V to 2.5 V Voltage Translation

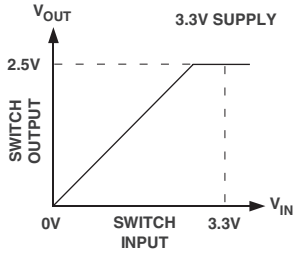


Figure 3. 3.3 V to 2.5 V Voltage Translation

2.5 V to 1.8 V Translation

When V_{CC} is 2.5 V and the input signal range is 0 V to V_{CC}, the maximum output signal will, as before, be clamped to within a voltage threshold below the V_{CC} supply. In this case, the output will be limited to approximately 1.8 V, as shown in Figure 5.

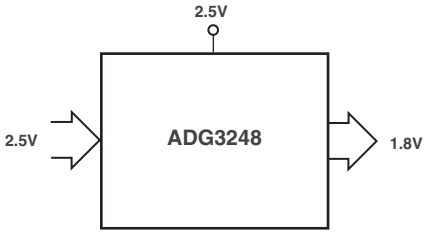


Figure 4. 2.5 V to 1.8 V Voltage Translation

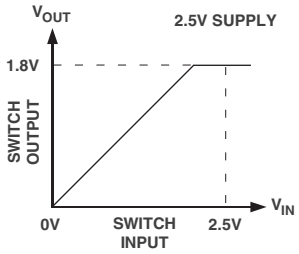


Figure 5. 2.5 V to 1.8 V Voltage Translation

Analog Switching

Bus switches can be used in many analog switching applications, for example, video graphics. Bus switches can have lower on resistance, smaller ON and OFF channel capacitance, and thus improved frequency performance than their analog counterparts. The bus switch channel itself, consisting solely of an NMOS switch, limits the operating voltage (see TPC 1 for a typical plot), but in many cases, this does not present an issue.

Multiplexing

Many systems, such as docking stations and memory banks, have a large number of common bus signals. Common problems faced by designers of these systems include

- Large delays caused by capacitive loading of the bus
- Noise due to simultaneous switching of the address and data bus signals

Figure 6 shows an array of memory banks in which each address and data signal is loaded by the sum of the individual loads. If a bus switch is used as shown in Figure 7, the output load on the memory address and data bits is halved. The speed at which the selected bank's data can flow is much improved because the capacitance loading is halved and the switches introduce negligible propagation delay. Bus noise is also reduced.

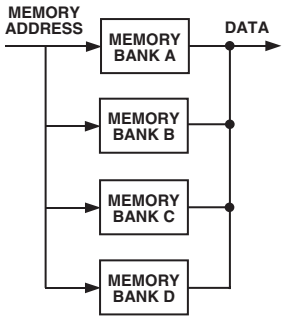


Figure 6. All Memory Banks Are Permanently Connected to the Bus

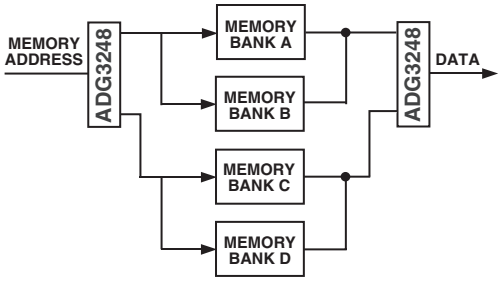
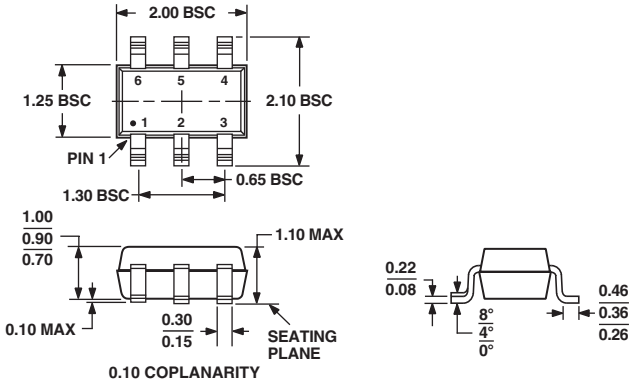


Figure 7. ADG3248 Used to Reduce Both Access Time and Noise

OUTLINE DIMENSIONS

6-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-6)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-203AB