elantec
HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

EL2075/EL2075C

2 GHz GBWP Gain-of-10 Stable Operational Amplifier

ELANTEC INC   T-79-06-10

Features

- 2 GHz gain-bandwidth product
- Gain-of-10 stable
- Conventional voltage-feedback topology
- Low offset voltage = 200 μV
- Low bias current = 2 μA
- Low offset current = 0.1 μA
- Output current = 50 mA over temperature
- Fast settling = 13 ns to 0.1%

Applications

- Active filters/integrators
- High-speed signal processing
- ADC/DAC buffers
- Pulse/RF amplifiers
- Pin diode receivers
- Log amplifiers
- Photo multiplier amplifiers
- High speed sample-and-holds

Ordering Information

Part No.	Temp. Range	Package	Outline #
EL2075CN	0°C to +75°C	8-Pin P-DIP	MDP0031
EL2075CS	0°C to +75°C	8-Lead SO	MDP0027
EL2075J/883B	−55°C to +125°C	8-Pin CerDIP	MDP0010

General Description

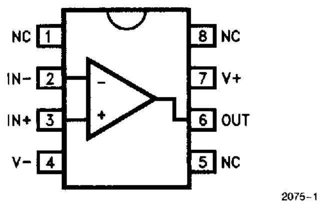
The EL2075 is a precision voltage-feedback amplifier featuring a 2 GHz gain-bandwidth product, fast settling time, excellent differential gain and differential phase performance, and a minimum of 50 mA output current drive over temperature.

The EL2075 is gain-of-10 stable with a −3 dB bandwidth of 400 MHz at $A_V = +10$. It has a very low 200 μV of input offset voltage, only 2 μA of input bias current, and a fully symmetrical differential input. Like all voltage-feedback operational amplifiers, the EL2075 allows the use of reactive or non-linear components in the feedback loop. This combination of speed and versatility makes the EL2075 the ideal choice for all op-amp applications at a gain of 10 or greater requiring high speed and precision, including active filters, integrators, sample-and-holds, and log amps. The low distortion, high output current, and fast settling makes the EL2075 an ideal amplifier for signal-processing and digitizing systems.

Elantec products and facilities comply with MIL-STD-883 Revision C, MIL-I-45208A, and other applicable quality specifications. For information on Elantec's military processing, see Elantec document, QRA-2: *Elantec's Military Processing, Monolithic Integrated Circuits.*

Connection Diagram

DIP and SO Package



1

August 1992 Rev B

EL2075/EL2075C

ELANTEC INC

2 GHz GBWP Gain-of-10 Stable Operational Amplifier

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S)	±7V
Output Current	Output is short-circuit protected to ground, however, maximum reliability is obtained if I_{OUT} does not exceed 70 mA.
Common-Mode Input	$\pm V_S$
Differential Input Voltage	5V
Thermal Resistance	θ_{JA} = 95°C/W P-DIP θ_{JA} = 125°C/W CerDIP θ_{JA} = 175°C/W SO-8
Operating Temperature	
EL2075	−55°C to +125°C
EL2075C	0°C to +75°C
Lead Temperature	
DIP Package	300°C
(Soldering: <5 seconds −CN <10 seconds −J)	
SO Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C
Junction Temperature	175°C
Storage Temperature	−60°C to +150°C

Note: See EL2071/EL2171 for Thermal Impedance curves.

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Open Loop DC Electrical Characteristics

V_S = ±5V, R_L = 100Ω, unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level EL2075	Test Level EL2075C	Units
V_{OS}	Input Offset Voltage	V_{CM} = 0V	25°C		0.2	1	I	I	mV
			T_{MIN}, T_{MAX}			2.5	I	III	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)	All		8		V	V	µV/°C
I_B	Input Bias Current	V_{CM} = 0V	All		2	6	I	II	µA
I_{OS}	Input Offset Current	V_{CM} = 0V	25°C		0.1	1	I	I	µA
			T_{MIN}, T_{MAX}			2	I	III	µA
PSRR	Power Supply Rejection Ratio	(Note 2)	All	70	90		I	II	dB
CMRR	Common Mode Rejection Ratio	(Note 3)	All	70	90		I	II	dB
I_S	Supply Current—Quiescent	No Load	25°C		21	23	I	I	mA
			T_{MIN}, T_{MAX}			25	I	III	mA
R_{IN} (diff)	R_{IN} (Differential)	Open-Loop	25°C		15		V	V	kΩ
C_{IN} (diff)	C_{IN} (Differential)	Open-Loop	25°C		1		V	V	pF
R_{IN} (cm)	R_{IN} (Common-Mode)		25°C		1		V	V	MΩ
C_{IN} (cm)	C_{IN} (Common-Mode)		25°C		1		V	V	pF

EL2075/EL2075C

2 GHz GBWP Gain-of-10 Stable Operational Amplifier

Open Loop DC Electrical Characteristics

V_S = ±5V, R_L = 100Ω, unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level EL2075	Test Level EL2075C	Units
R_{OUT}	Output Resistance		25°C		50		V	V	mΩ
CMIR	Common-Mode Input Range		25°C	±3	±3.5		IV	IV	V
			T_{MIN}, T_{MAX}	±2.5			IV	IV	V
I_{OUT}	Output Current		All	50	70		I	II	mA
V_{OUT}	Output Voltage Swing	No Load	All	±3.5	±4		I	II	V
V_{OUT} 100	Output Voltage Swing	100Ω	All	±3	±3.6		I	II	V
V_{OUT} 50	Output Voltage Swing	50Ω	All	±2.5	±3.4		I	II	V
A_{VOL} 100	Open-Loop Gain	100Ω	25°C	1000	2800		I	I	V/V
			T_{MIN}, T_{MAX}	800			I	III	V/V
A_{VOL} 50	Open-Loop Gain	50Ω	25°C	800	2300		I	I	V/V
			T_{MIN}, T_{MAX}	600			I	III	V/V
eN@ > 1 MHz	Noise Voltage 1–100 MHz		25°C		2.3		V	V	nV/√Hz
iN@ > 100 kHz	Noise Current 100k–100 MHz		25°C		3.2		V	V	pA/√Hz

Closed Loop AC Electrical Characteristics

V_S = ±5V, A_V = +20, Rf = 1500Ω, R_L = 100Ω unless otherwise specified

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level EL2075	Test Level EL2075C	Units
SSBW	−3 dB Bandwidth (V_{OUT} = 0.4V_{PP})	A_V = +10	25°C		400		V	V	MHz
		A_V = +20	25°C	150	200		I	III	MHz
			T_{MIN}, T_{MAX}	125			IV	IV	MHz
		A_V = +50	25°C		40		V	V	MHz
GBWP	Gain-Bandwidth Product	A_V = +100	25°C		2.0		V	V	GHz
LSBWa	−3 dB Bandwidth	V_{OUT} = 2 V_{PP} (Note 4)	All	80	128		IV	IV	MHz
LSBWb	−3 dB Bandwidth	V_{OUT} = 5 V_{PP} (Note 4)	All	32	50		IV	IV	MHz
GFPL	Peaking (<50 MHz)	V_{OUT} = 0.4 V_{PP}	25°C		0	0.5	I	III	dB
			T_{MIN}, T_{MAX}			0.5	IV	IV	dB
GFPH	Peaking (>50 MHz)	V_{OUT} = 0.4 V_{PP}	25°C		0	1	I	III	dB
			T_{MIN}, T_{MAX}			1	IV	IV	dB
GFR	Rolloff (<100 MHz)	V_{OUT} = 0.4 V_{PP}	25°C		0.1	0.5	I	III	dB
			T_{MIN}, T_{MAX}			0.5	I	IV	dB

EL2075/EL2075C

ELANTEC INC

2 GHz GBWP Gain-of-10 Stable Operational Amplifier

Closed Loop AC Electrical Characteristics

V_S = ±5V, A_V = +20, Rf = 1500Ω, R_L = 100Ω unless otherwise specified — Contd.

Parameter	Description	Test Conditions	Temp	Min	Typ	Max	Test Level		Units
							EL2075	EL2075C	
LPD	Linear Phase Deviation (<100 MHz)	V_{OUT} = 0.4 V_{PP}	All		1	1.8	IV	IV	°
PM	Phase Margin	A_V = +10	25°C		60		V	V	°
tr1, tf1	Rise Time, Fall Time	0.4V Step, A_V = +10	25°C		1.2		V	V	ns
tr2, tf2	Rise Time, Fall Time	5V Step, A_V = +10	25°C		6		V	V	ns
ts1	Settling to 0.1% (A_V = −20)	2V Step	25°C		13		V	V	ns
ts2	Settling to 0.01% (A_V = −20)	2V Step	25°C		25		V	V	ns
OS	Overshoot	2V Step, A_V = +10	25°C		10		V	V	%
SR	Slew Rate	2V Step, A_V = +10	All	500	800		IV	IV	V/μs
DISTORTION (Note 5)									
HD2	2nd Harmonic Distortion	@ 20 MHz, A_V = +20	25°C		−40	−30	I	III	dBc
			T_{MIN}, T_{MAX}			−30	IV	IV	dBc
HD3	3rd Harmonic Distortion	@ 20 MHz, A_V = +20	25°C		−65	−50	I	III	dBc
			T_{MIN}, T_{MAX}			−50	IV	IV	dBc

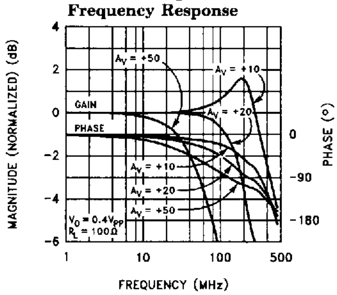
Note 1: Measured from T_{MIN}, T_{MAX}.
Note 2: $\pm V_{CC}$ = ±4.5V to 5.5V.
Note 3: $\pm V_{IN}$ = ±2.5V, V_{OUT} = 0V
Note 4: Large-signal bandwidth calculated using $LSBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$.
Note 5: All distortion measurements are made with V_{OUT} = 2 V_{PP}, R_L = 100Ω.

EL2075/EL2075C

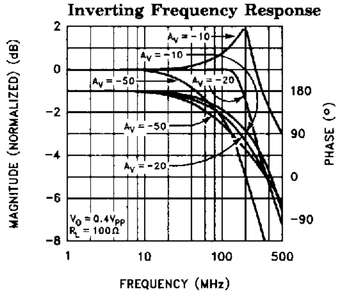
2 GHz GBWP Gain-of-10 Stable Operational Amplifier

Typical Performance Curves (T_A = 25°C)

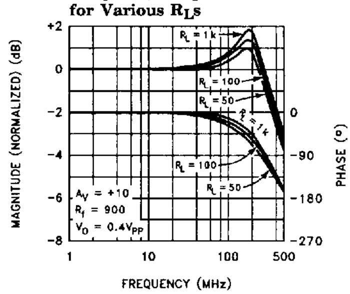
Non-Inverting Frequency Response



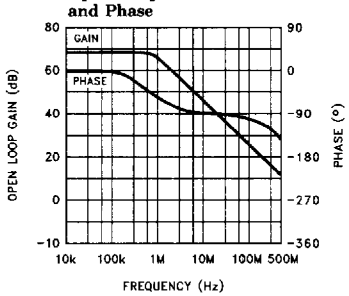
Inverting Frequency Response



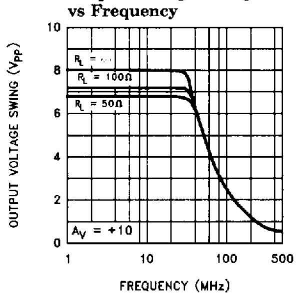
Frequency Response for Various R_Ls



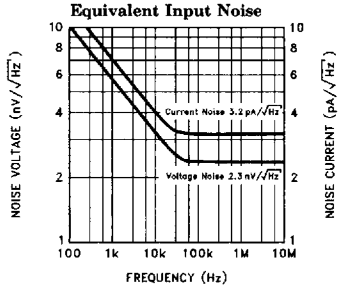
Open Loop Gain and Phase



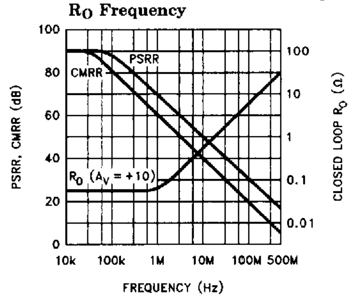
Output Voltage Swing vs Frequency



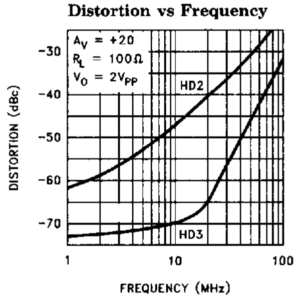
Equivalent Input Noise



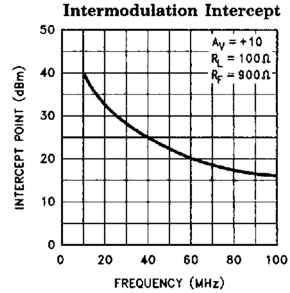
PSRR, CMRR, and Closed-Loop R_O Frequency



2nd and 3rd Harmonic Distortion vs Frequency



2-Tone, 3rd Order Intermodulation Intercept



2075-2

EL2075/EL2075C
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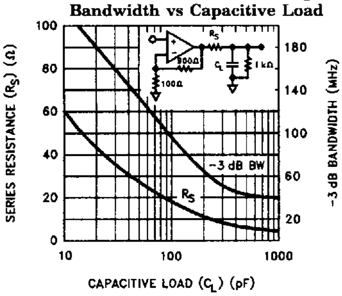
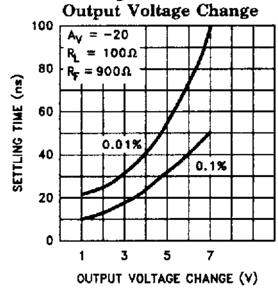
2 GHz GBWP Gain-of-10 Stable Operational Amplifier

Typical Performance Curves (T_A = 25°C unless otherwise specified) — Contd.

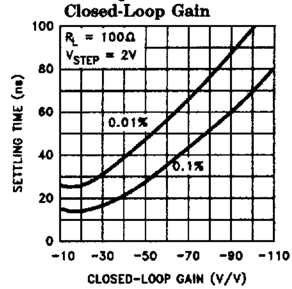
Series Resistor and Resulting Bandwidth vs Capacitive Load



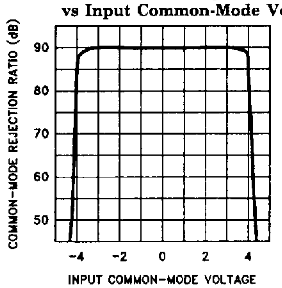
Settling Time vs Output Voltage Change



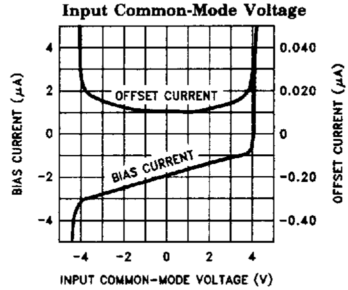
Settling Time vs Closed-Loop Gain



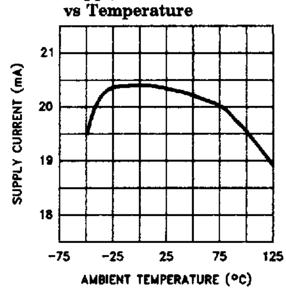
Common-Mode Rejection Ratio vs Input Common-Mode Voltage



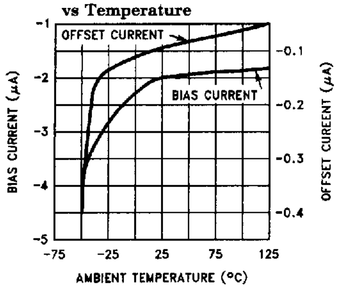
Bias and Offset Current vs Input Common-Mode Voltage



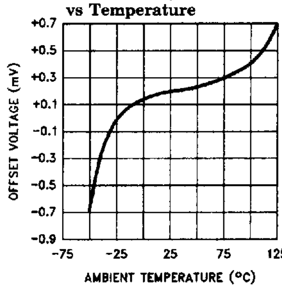
Supply Current vs Temperature



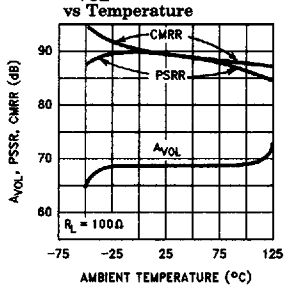
Bias and Offset Current vs Temperature



Offset Voltage vs Temperature



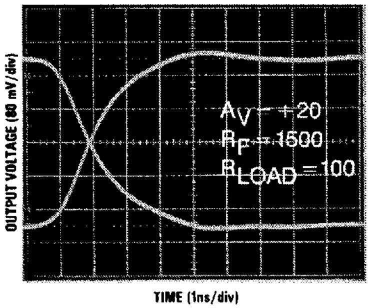
A_{VOL}, PSRR, and CMRR vs Temperature



2075-3

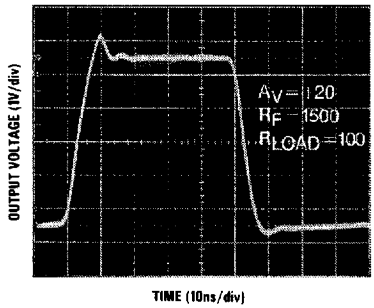
Typical Performance Curves (T_A = 25°C) — Contd.

Small Signal Transient Response



2075-4

Large Signal Transient Response



2075-5

EL2075/EL2075C

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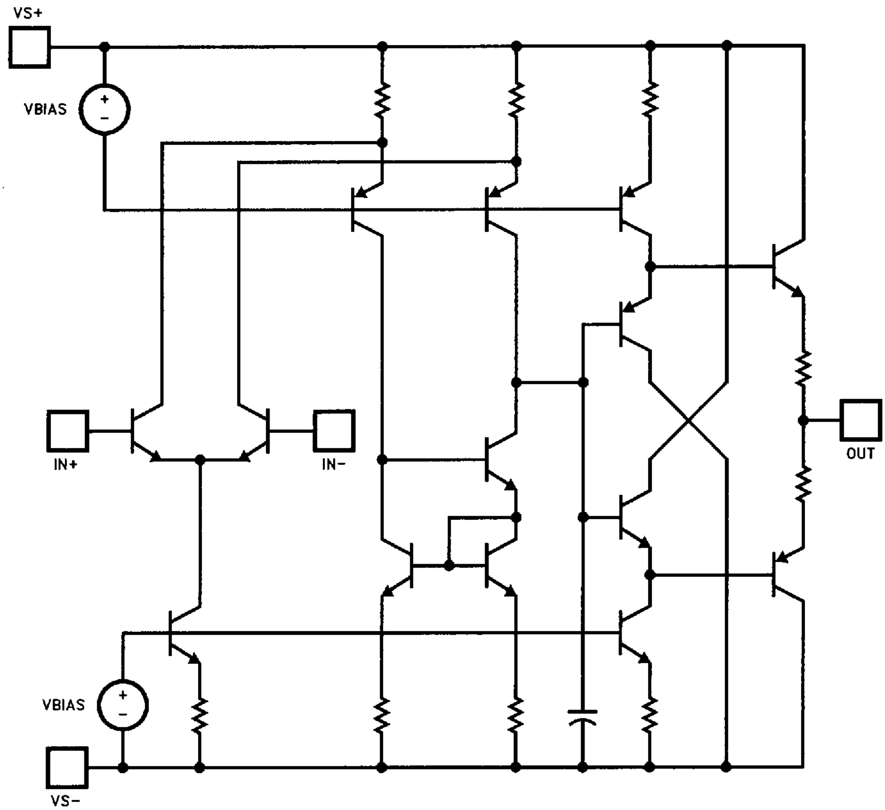
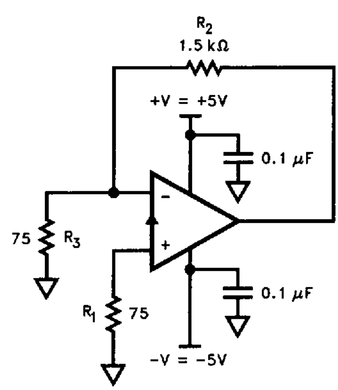
2 GHz GBWP Gain-of-10 Stable Operational Amplifier

Equivalent Circuit



2075-6

Burn-In Circuit



2075-7

All Packages Use The Same Schematic

EL2075/EL2075C

2 GHz GBWP Gain-of-10 Stable Operational Amplifier

Applications Information

Product Description

The EL2075 is a wideband monolithic operational amplifier built on a high-speed complementary bipolar process. The EL2075 uses a classical voltage-feedback topology which allows it to be used in a variety of applications requiring a noise gain ≥ 10 where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2075 allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators. Similarly, because of the ability to use diodes in the feedback network, the EL2075 is an excellent choice for applications such as log amplifiers.

The EL2075 also has excellent DC specifications: 200 μV, V_{OS}, 2 μA I_B, 0.1 μA I_{OS}, and 90 dB of CMRR. These specifications allow the EL2075 to be used in DC-sensitive applications such as difference amplifiers. Furthermore, the current noise of the EL2075 is only 3.2 pA/$\sqrt{Hz}$, making it an excellent choice for high-sensitivity transimpedance amplifier configurations.

Gain-Bandwidth Product

The EL2075 has a gain-bandwidth product of 2 GHz. For gains greater than 40, its closed-loop -3 dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 40, higher-order poles in the amplifier's transfer function contribute to even higher closed loop bandwidths. For example, the EL2075 has a -3 dB bandwidth of 400 MHz at a gain of $+10$, dropping to 200 MHz at a gain of $+20$. It is important to note that the EL2075 has been designed so that this "extra" bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2075 in a gain of $+10$ only exhibits 1.5 dB of peaking with a 100Ω load.

Output Drive Capability

The EL2075 has been optimized to drive 50Ω and 75Ω loads. It can easily drive 6 V_{PP} into a 50Ω load. This high output drive capability makes the EL2075 an ideal choice for RF and IF applications. Furthermore, the current drive of the EL2075 remains a minimum of 50 mA at low temperatures. The EL2075 is current-limited at the output, allowing it to withstand momentary shorts to ground. However, power dissipation with the output shorted can be in excess of the power-dissipation capabilities of the package.

Capacitive Loads

Although the EL2075 has been optimized to drive resistive loads as low as 50Ω, capacitive loads will decrease the amplifier's phase margin which may result in peaking, overshoot, and possible oscillation. For optimum AC performance, capacitive loads should be reduced as much as possible or isolated via a series output resistor. Coax lines can be driven, as long as they are terminated with their characteristic impedance. When properly terminated, the capacitance of coaxial cable will not add to the capacitive load seen by the amplifier. Capacitive loads greater than 10 pF should be buffered with a series resistor (Rs) to isolate the load capacitance from the amplifier output. A curve of recommended Rs vs Cload has been included for reference. Values of Rs were chosen to maximize resulting bandwidth without additionl peaking.

Printed-Circuit Layout

As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 1 μF–10 μF tantalum capacitor is recommended in parallel with a 0.01 μF ceramic capacitor. All lead lengths should be as short as possible, and all bypass capacitors should be as close to the device pins as possible. Parasitic capacitances should be kept to an absolute minimum at both inputs and at the output. Resistor values should be kept under 1000Ω to 2000Ω because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of parasitic inductance. Similarly, capacitors should be low-inductance for best performance. If possible, solder the EL2075 directly to the PC board without a socket. Even high quality sockets add parasitic capacitance and inductance which can potentially degrade performance. Because of the degradation of AC performance due to parasitics, the use of surface-mount components (resistors, capacitors, etc.) is also recommended.

EL2075/EL2075C

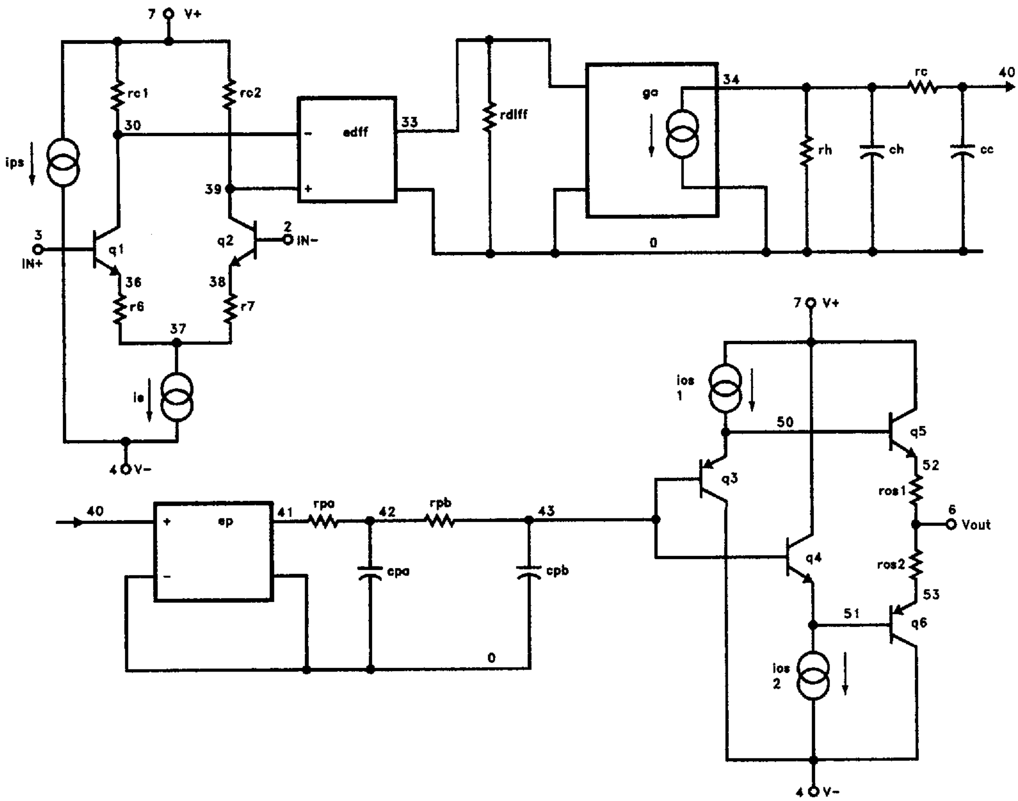
ELANTEC INC

2 GHz GBWP Gain-of-10 Stable Operational Amplifier

EL2075 Macromodel

```
*
* Connections:                +input
*                             | -input
*                             | |   +Vsupply
*                             | |   |   -Vsupply
*                             | |   |   |   output
*                             | |   |   |   |
.subckt M2075                 3 2   7   4   6
*
*Input Stage
*
ie 37 4 1 mA
r6 36 37 15
r7 38 37 15
rc1 7 30 200
rc2 7 39 200
q1 30 3 36 qn
q2 39 2 38 qna
ediff 33 0 39 30 1
rdiff 33 0 1 Meg
*
* Compensation Section
*
ga 0 34 33 0 2m
rh 34 0 500K
ch 34 0 0.4 pF
rc 34 40 50
cc 40 0 0.05 pF
*
* Poles
*
ep 41 0 40 0 1
rpa 41 42 250
cpa 42 0 0.8 pF
rpb 42 43 50
cpb 43 0 0.5 pF
*
* Output Stage
*
ios1 7 50 3.0 mA
ios2 51 4 3.0 mA
q3 4 43 50 qp
q4 7 43 51 qn
q5 7 50 52 qn
q6 4 51 53 qp
ros1 52 6 2
ros2 6 53 2
*
* Power Supply Current
*
ips 7 4 11.4 mA
*
* Models
*
.model qna npn(is=800e-18 bf=170 tf=0.2 ns)
.model qn  npn(is=810e-18 bf=200 tf=0.2 ns)
.model qp  pnp(is=800e-18 bf=200 tf=0.2 ns)
.ends
```

EL2075 Macromodel — Contd.



2075-8