

NTD4969N

Power MOSFET

30 V, 41 A, Single N-Channel, DPAK/IPAK

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Three Package Variations for Design Flexibility
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- CPU Power Delivery
- DC-DC Converters

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit		
Drain-to-Source Voltage	V_{DSS}	30	V		
Gate-to-Source Voltage	V_{GS}	± 20	V		
Continuous Drain Current $R_{\theta JA}$ (Note 1)	I_D	$T_A = 25^\circ\text{C}$	12.7	A	
		$T_A = 100^\circ\text{C}$	9.0		
Power Dissipation $R_{\theta JA}$ (Note 1)	P_D	$T_A = 25^\circ\text{C}$	2.56	W	
		$T_A = 100^\circ\text{C}$			
Continuous Drain Current $R_{\theta JA}$ (Note 2)	I_D	$T_A = 25^\circ\text{C}$	9.4	A	
		$T_A = 100^\circ\text{C}$	6.6		
Power Dissipation $R_{\theta JA}$ (Note 2)	P_D	$T_A = 25^\circ\text{C}$	1.38	W	
		$T_A = 100^\circ\text{C}$			
Continuous Drain Current $R_{\theta JC}$ (Note 1)	I_D	$T_C = 25^\circ\text{C}$	41	A	
		$T_C = 100^\circ\text{C}$	29		
Power Dissipation $R_{\theta JC}$ (Note 1)	P_D	$T_C = 25^\circ\text{C}$	26.3	W	
		$T_C = 100^\circ\text{C}$			
Pulsed Drain Current	$t_p = 10\mu\text{s}$	$T_A = 25^\circ\text{C}$	I_{DM}	150	A
Current Limited by Package	$T_A = 25^\circ\text{C}$	$I_{DmaxPkg}$	40	A	
Operating Junction and Storage Temperature	T_J, T_{STG}	-55 to +175		$^\circ\text{C}$	
Source Current (Body Diode)	I_S	24		A	
Drain to Source dV/dt	dV/dt	6.0		V/ns	
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}$, $V_{DD} = 24\text{ V}$, $V_{GS} = 10\text{ V}$, $I_L = 19\text{ A}_{pk}$, $L = 0.1\text{ mH}$, $R_G = 25\ \Omega$)	EAS	18		mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260		$^\circ\text{C}$	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

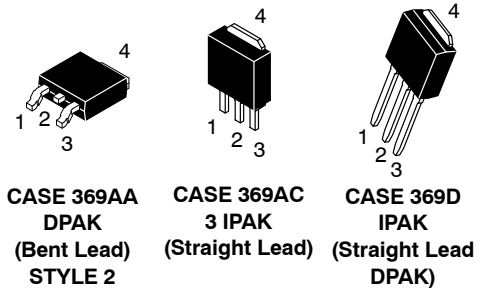
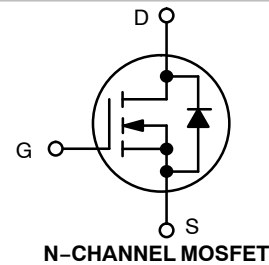
1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.



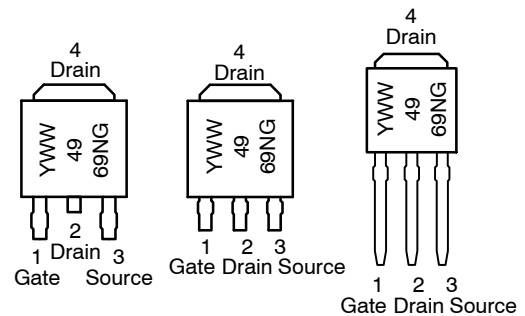
ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
30 V	9.0 m Ω @ 10 V	41 A
	19 m Ω @ 4.5 V	



MARKING DIAGRAMS & PIN ASSIGNMENTS



Y = Year
 WW = Work Week
 4969N = Device Code
 G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

NTD4969N

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	5.7	°C/W
Junction-to-TAB (Drain)	$R_{\theta JC-TAB}$	4.3	
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	58.6	
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	108.6	

- Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
- Surface-mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
-----------	--------	----------------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			17		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.5	1.8	2.5	V	
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			4.5		mV/°C	
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 30\text{ A}$		6.9	9.0	m Ω
			$I_D = 15\text{ A}$		6.9		
		$V_{GS} = 4.5\text{ V}$	$I_D = 30\text{ A}$		13.6	19	
			$I_D = 15\text{ A}$		13.2		
Forward Transconductance	g_{FS}	$V_{DS} = 1.5\text{ V}, I_D = 30\text{ A}$		36		S	

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 15\text{ V}$		837		pF
Output Capacitance	C_{OSS}			347		
Reverse Transfer Capacitance	C_{RSS}			180		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		9.0		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.42		
Gate-to-Source Charge	Q_{GS}			2.8		
Gate-to-Drain Charge	Q_{GD}			4.8		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		16.5		nC

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		10		ns
Rise Time	t_r			27		
Turn-Off Delay Time	$t_{d(OFF)}$			13.3		
Fall Time	t_f			6.4		

- Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.
- Assume terminal length of 110 mils.

NTD4969N

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 6)						
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$		6.5		ns
Rise Time	t_r			20.2		
Turn-Off Delay Time	$t_{d(OFF)}$			17.2		
Fall Time	t_f			4.2		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V},$ $I_S = 30\text{ A}$	$T_J = 25^\circ\text{C}$		0.91	1.1	V
			$T_J = 125^\circ\text{C}$		0.82		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 30\text{ A}$			20.8		ns
Charge Time	t_a				9.8		
Discharge Time	t_b				11		
Reverse Recovery Charge	Q_{RR}				8.0		

PACKAGE PARASITIC VALUES

Source Inductance (Note 7)	L_S	$T_A = 25^\circ\text{C}$		2.85		nH
Drain Inductance, DPAK	L_D			0.0164		
Drain Inductance, IPAK (Note 7)	L_D			1.88		
Gate Inductance (Note 7)	L_G			4.9		
Gate Resistance	R_G			1.0	2.2	

5. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
6. Switching characteristics are independent of operating junction temperatures.
7. Assume terminal length of 110 mils.

ORDERING INFORMATION

Device	Package	Shipping [†]
NTD4969NT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NTD4969N-1G	IPAK (Pb-Free)	75 Units / Rail
NTD4969N-35G	IPAK Trimmed Lead (Pb-Free)	75 Units / Rail

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL PERFORMANCE CURVES

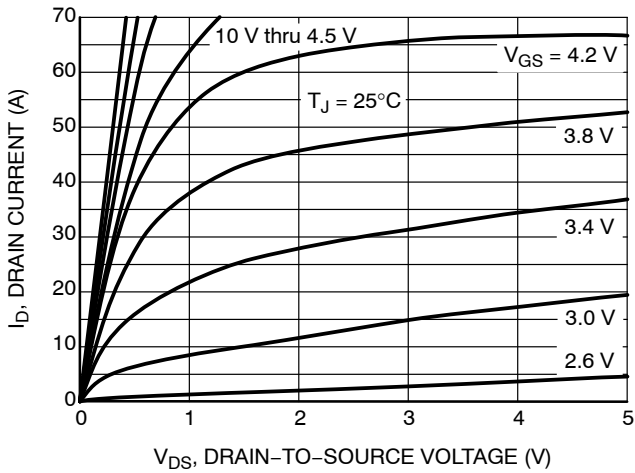


Figure 1. On-Region Characteristics

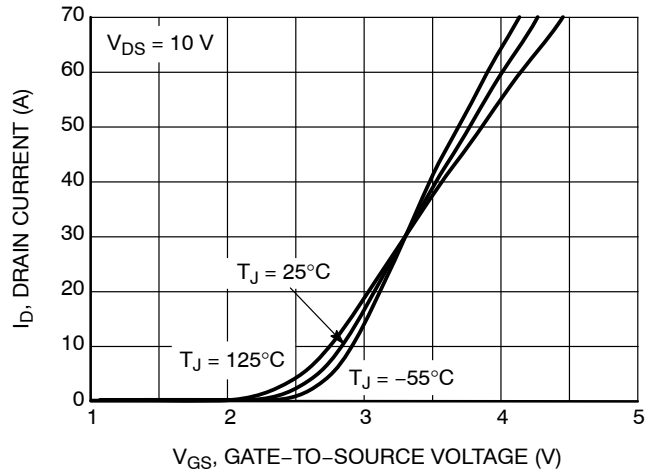


Figure 2. Transfer Characteristics

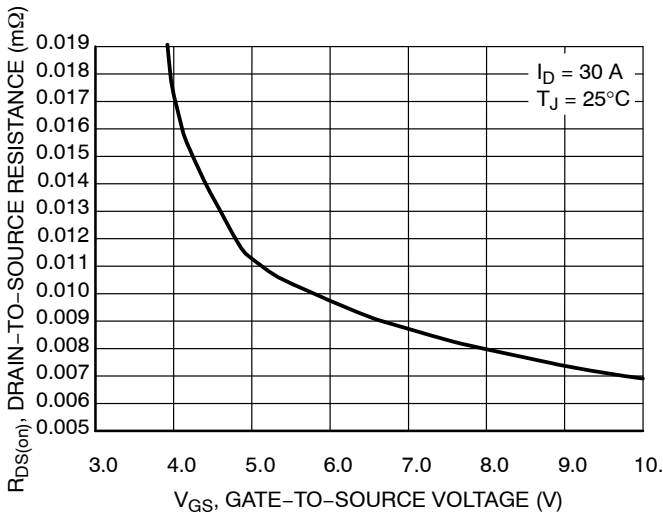


Figure 3. On-Resistance vs. Gate-to-Source Voltage

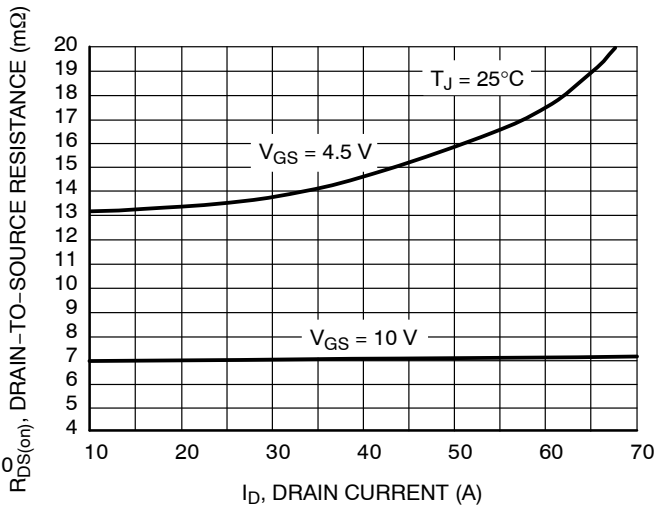


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

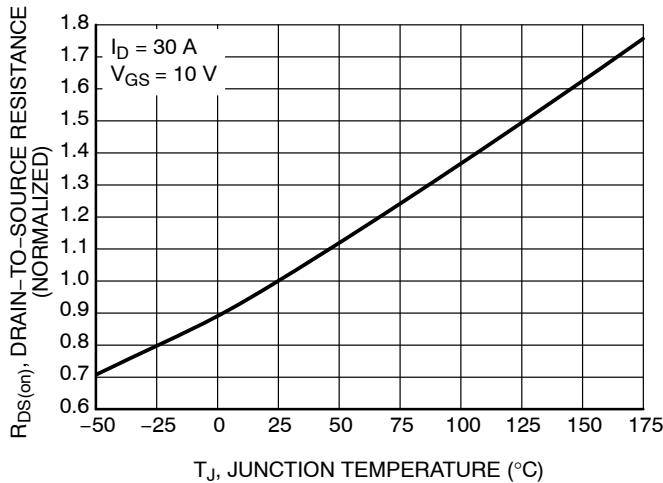


Figure 5. On-Resistance Variation with Temperature

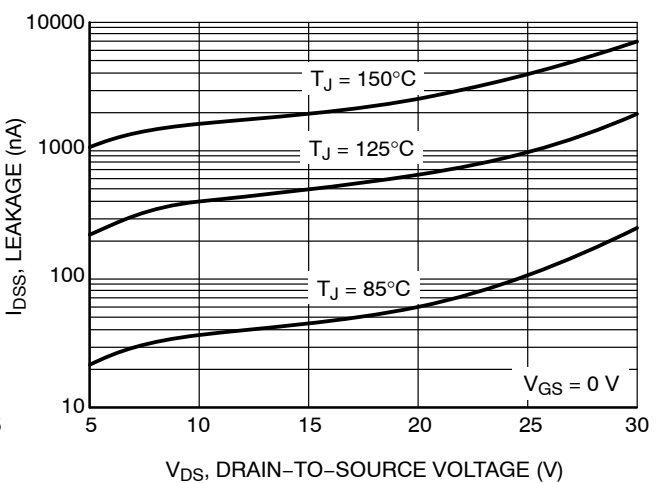


Figure 6. Drain-to-Source Leakage Current vs. Voltage

NTD4969N

TYPICAL PERFORMANCE CURVES

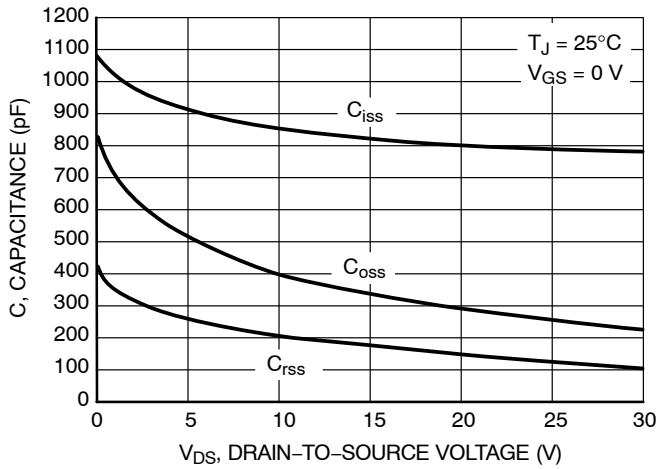


Figure 7. Capacitance Variation

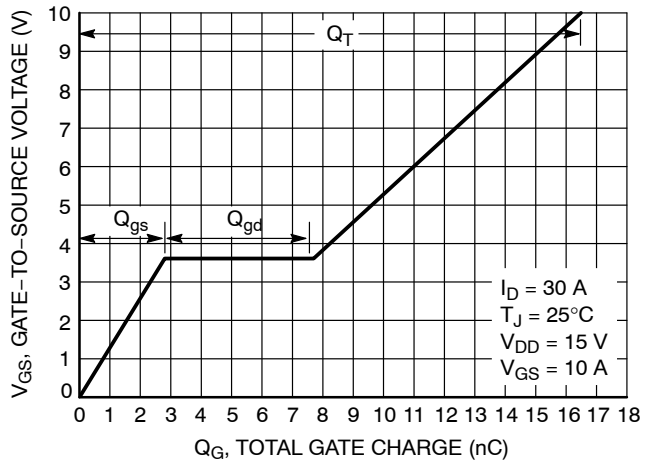


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

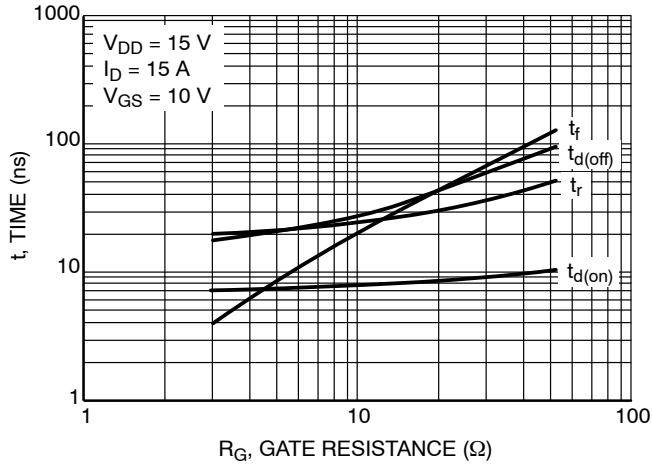


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

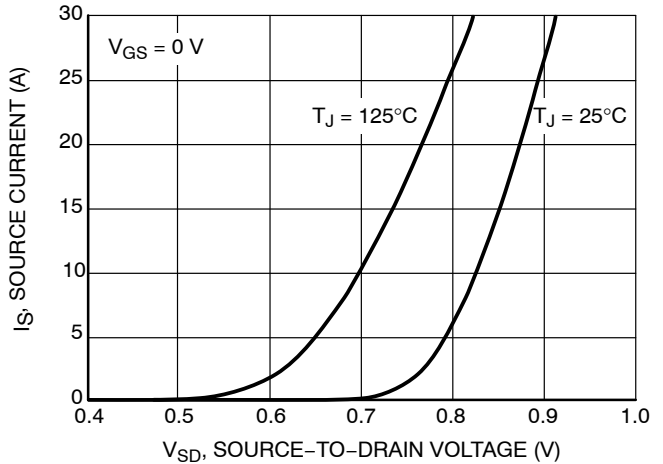


Figure 10. Diode Forward Voltage vs. Current

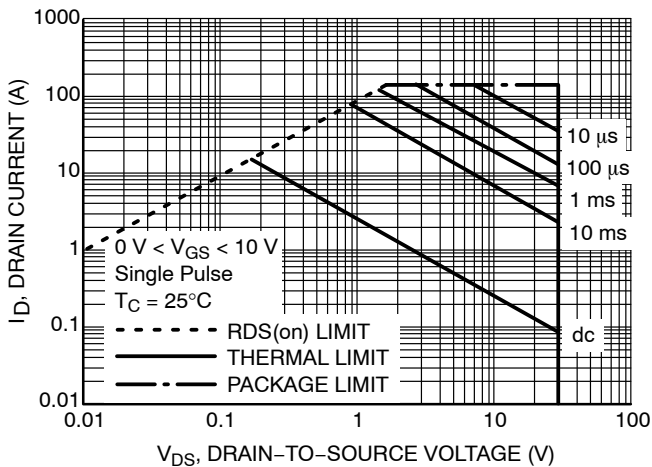


Figure 11. Maximum Rated Forward Biased Safe Operating Area

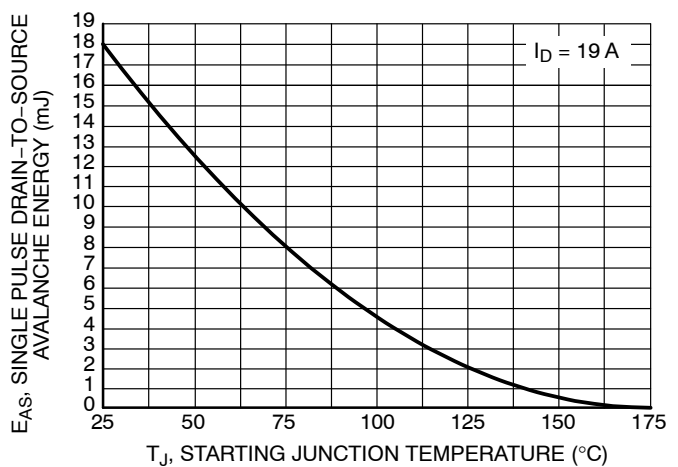
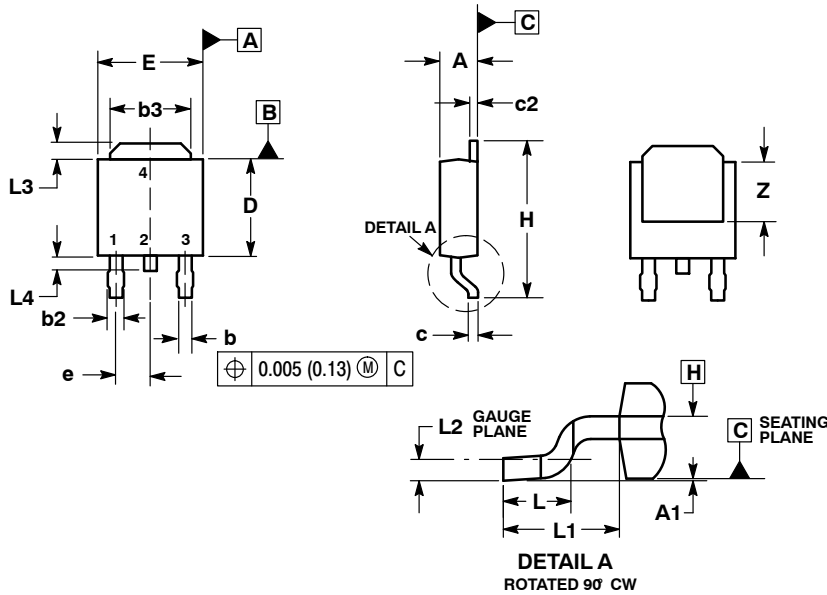


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

NTD4969N

PACKAGE DIMENSIONS

DPAK (SINGLE GUAGE) CASE 369AA-01 ISSUE B

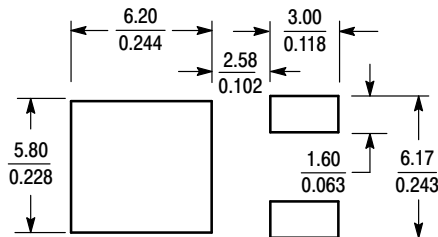


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

STYLE 2:

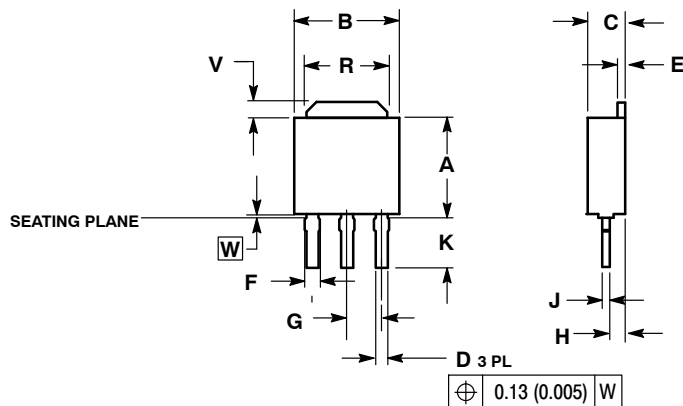
- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTD4969N

PACKAGE DIMENSIONS

3 IPAK, STRAIGHT LEAD CASE 369AC-01 ISSUE O

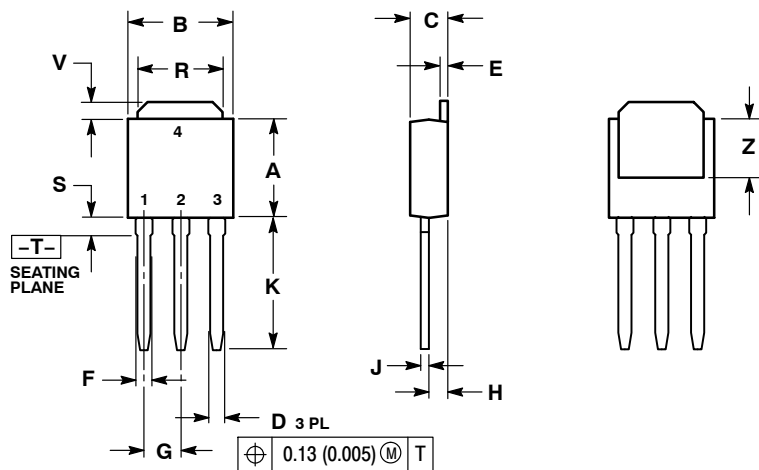


NOTES:

- 1.. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2.. CONTROLLING DIMENSION: INCH.
3. SEATING PLANE IS ON TOP OF DAMBAR POSITION.
4. DIMENSION A DOES NOT INCLUDE DAMBAR POSITION OR MOLD GATE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.043	0.94	1.09
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.134	0.142	3.40	3.60
R	0.180	0.215	4.57	5.46
V	0.035	0.050	0.89	1.27
W	0.000	0.010	0.000	0.25

IPAK CASE 369D-01 ISSUE C



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:

- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

ON Semiconductor and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative