NEC

MOS INTEGRATED CIRCUIT

μPD16908

DC-DC CONVERTER IC FOR ORGANIC EL DISPLAYS

DESCRIPTION

The μPD16908 is composed of a 4ch step-up circuit (chopper method), a 2ch polarity-inverted circuit (chopper method) and a 3ch series regulator, and is ideal for the power supply for organic EL displays.

FEATURES

- Output voltage setting function via serial interface
- On-chip soft start circuit
- Low current consumption achieved by full CMOS
- On-chip timer latch short-circuit protection circuit
- Adjustable oscillation frequency (200 to 800 kHz)
- MOS FET directly driven by push-pull-configured output stage
- Mounted on 56-pin plastic WQFN (8 x 8)

★ ORDERING INFORMATION

Part Number	Package
μPD16908K9-5B4-A	56-pin plastic WQFN (8 x 8)

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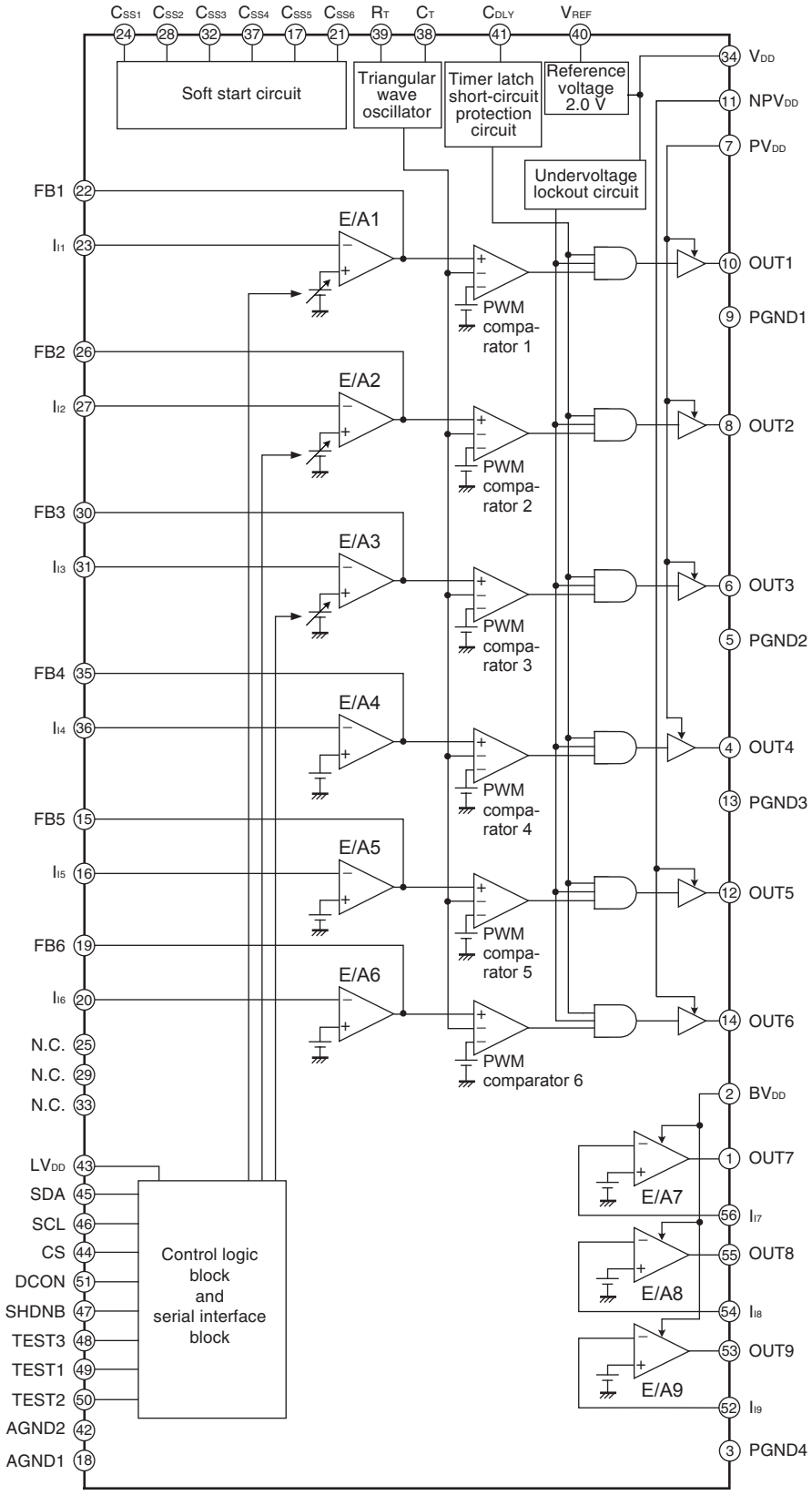
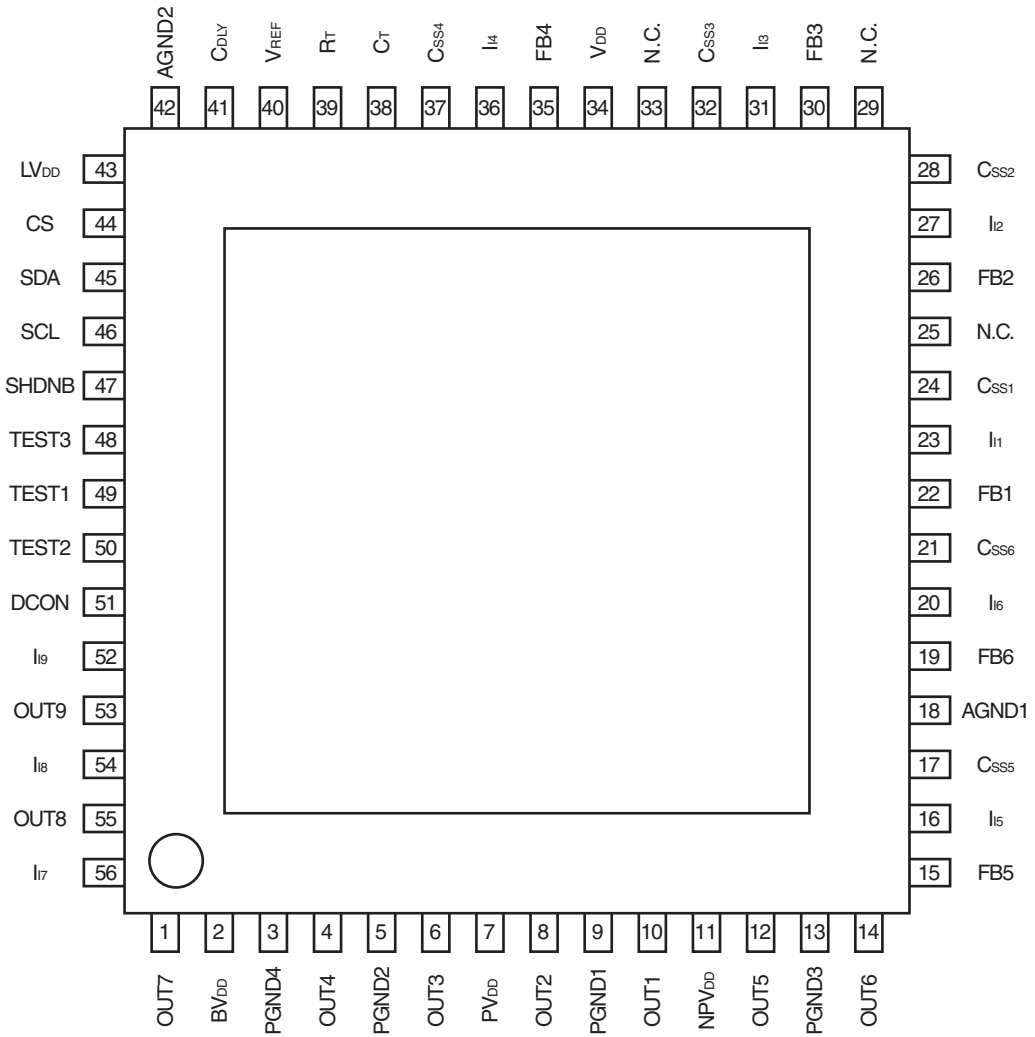
The mark ★ shows major revised points.

1. BLOCK DIAGRAM



2. PIN CONFIGURATION (Top View)



3. PIN FUNCTIONS

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Pin No.	Symbol	Pin Name	I/O	Description
1	OUT7	Output 7	Output	Output of ch7 series regulator (E/A)
2	BV_{DD}	Buffer regulator power supply	Power supply	Power supply for series regulator (ch7 to ch9)
3	PGND4	Power ground	Ground	Power ground
4	OUT4	Output 4	Output	Output for driving Power MOS FET of ch4
5	PGND2	Power ground	Ground	Power ground
6	OUT3	Output 3	Output	Output for driving Power MOS FET of ch3
7	PV_{DD}	Power supply for output buffer stage	Power supply	Power supply for output buffer stage of ch1 to ch4
8	OUT2	Output 2	Output	Output for driving Power MOS FET of ch2
9	PGND1	Power ground	Ground	Power ground
10	OUT1	Output 1	Output	Output for driving Power MOS FET of ch1
11	NPV_{DD}	Power supply for output buffer stage	Power supply	Power supply for output buffer stage of ch5 and ch6
12	OUT5	Output 5	Output	Output for driving Power MOS FET of ch5
13	PGND3	Power ground	Ground	Power ground
14	OUT6	Output 6	Output	Output for driving Power MOS FET of ch6
15	FB5	Feedback	Output	Feedback of ch5 E/A
16	I_{I5}	Inversion input	Input	Inversion input of ch5 E/A
17	C_{SS5}	Soft start capacitance 5	Output	Capacitance connection pin for ch5 soft start
18	AGND1	Analog ground	Ground	Analog ground
19	FB6	Feedback	Output	Feedback of ch6 E/A
20	I_{I6}	Inversion input	Input	Inversion input of ch6 E/A
21	C_{SS6}	Soft start capacitance 6	Output	Capacitance connection pin for ch6 soft start
22	FB1	Feedback	Output	Feedback of ch1 E/A
23	I_{I1}	Inversion input	Input	Inversion input of ch1 E/A
24	C_{SS1}	Soft start capacitance 1	Output	Capacitance connection pin for ch1 soft start
25	N.C.	–	–	Leave open, or short to GND or LV_{DD}
26	FB2	Feedback	Output	Feedback of ch2 E/A
27	I_{I2}	Inversion input	Input	Inversion input of ch2 E/A
28	C_{SS2}	Soft start capacitance 2	Output	Capacitance connection pin for ch2 soft start
29	N.C.	–	–	Leave open, or short to GND or LV_{DD}
30	FB3	Feedback	Output	Feedback of ch3 E/A
31	I_{I3}	Inversion input	Input	Inversion input of ch3 E/A
32	C_{SS3}	Soft start capacitance 3	Output	Capacitance connection pin for ch3 soft start
33	N.C.	–	–	Leave open, or short to GND or LV_{DD}
34	V_{DD}	Power supply	Power supply	Power supply for DC-DC converter
35	FB4	Feedback	Output	Feedback of ch4 E/A
36	I_{I4}	Inversion input	Input	Inversion input of ch4 E/A
37	C_{SS4}	Soft start capacitance 4	Output	Capacitance connection pin for ch4 soft start

(2/2)

Pin No.	Symbol	Pin Name	I/O	Description
38	C_T	Timing capacitor	Output	Capacitor connection for triangular wave generation
39	R_T	Timing resistance	Output	Resistance connection for triangular wave generation
40	V_{REF}	Reference voltage	Output	Power supply for reference voltage
41	C_{DLY}	Short-circuit protection circuit delay capacitance	Output	Capacitor connection for timer latch
42	AGND2	Analog ground	Ground	Analog ground
43	LV_{DD}	Power supply for control logic	Power supply	Power supply for control logic
44	CS	Chip select	Input	Chip select
45	SDA	Serial data input	input	Serial data input for controlling each output
46	SCL	Serial clock input	input	Serial clock input for controlling each output
47	SHDNB	Shut-down input	input	Shut down the IC
48	TEST3	Test 3	Input	Short to LV_{DD}
49	TEST1	Test 1	Input	Short to GND
50	TEST2	Test 2	Input	Short to GND
51	DCON	Output turn-on control	Input	Output of the channel selected by serial data is switched ON.
52	I_{I9}	Inversion input	Input	Inversion input of ch9 E/A
53	OUT9	Output 9	Output	Output of ch9 series regulator (E/A)
54	I_{I8}	Inversion input	Input	Inversion input of ch8 E/A
55	OUT8	Output 8	Output	Output of ch8 series regulator (E/A)
56	I_{I7}	Inversion input	Input	Inversion input of ch7 E/A

4. ELECTRICAL SPECIFICATIONS

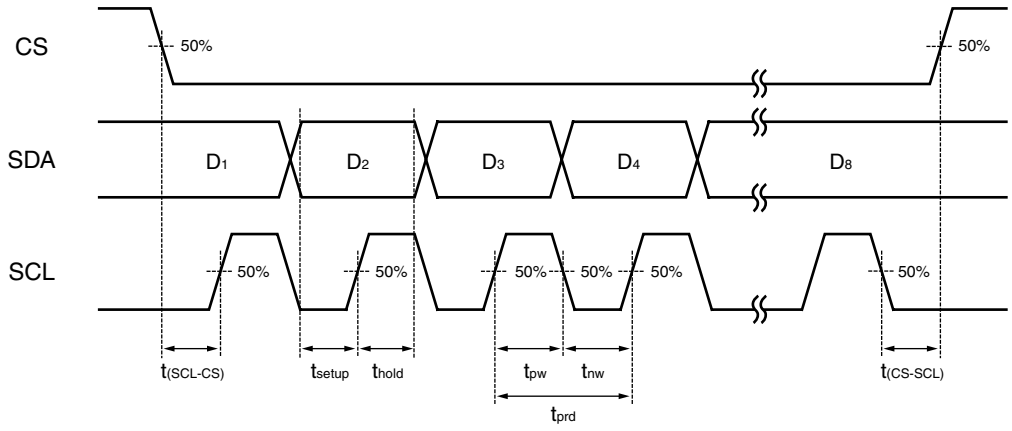
Absolute Maximum Ratings (Unless otherwise specified, T_A = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}		−0.5 to +6	V
Power supply voltage for output buffer stage 1	PV_{DD}	(ch1 to ch4)	−0.5 to +6	V
Power supply voltage for output buffer stage 2	NPV_{DD}	(ch5 and ch6)	−0.5 to +6	V
Buffer regulator power supply voltage	BV_{DD}		−0.5 to +6	V
Control logic power supply voltage	LV_{DD}		−0.5 to +6	V
Analog input pin voltage	V_{AIN}	FB, I_I	−0.5 to +6	V
Control logic input voltage	V_{CLIN}	SHDNB, DCON, SDA, SCL, CS	−0.5 to LV_{DD} + 0.5	V
Output current (DC) 1-6	$I_{O(DC)1-6}$	OUT1 to OUT6	20	mA
Output current (pulse) 1-6	$I_{O(pulse)1-6}$	OUT1 to OUT6	200	mA
Output current (DC) 7-9	$I_{O(DC)7-9}$	OUT7 to OUT9	20	mA
Total power dissipation	P_T	Glass epoxy board of 100 mm x 100 mm x 1 mm with copper foil area of 15%	0.8	W
Operating ambient temperature	T_A		−30 to +75	°C
Operating junction temperature	T_J		−30 to +125	°C
Storage temperature	T_{stg}		−55 to +125	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Recommended Operating Conditions (Unless otherwise specified, T_A = 25°C)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Power supply voltage	V_{DD}		2.7	3.3	5.5	V
Power supply voltage for output buffer stage 1	PV_{DD}	(ch1 to ch4)	2.7	3.3	5.5	V
Power supply voltage for output buffer stage 2	NPV_{DD}	(ch5 and ch6)	2.7	3.3	5.5	V
Buffer regulator power supply voltage	BV_{DD}		3.0	3.3	5.5	V
Control logic power supply voltage	LV_{DD}		2.7	3.3	3.6	V
Control logic input voltage	V_{CLIN}	SHDNB, DCON, SDA, SCL, CS	2.7	3.3	3.6	V
Operating frequency	f_{OSC}		200	700	800	kHz
Timing capacitance	C_{CT}	Capacitance connected to C_T	60		240	pF
Timing resistance	R_{RT}	Resistance connected to R_T	5.1		22	kΩ
Serial clock period	t_{prd}				10	μs
SCL waiting time	$t_{(SCL-CS)}$		500			ns
CS waiting time	$t_{(CS-SCL)}$		50			ns
SDA set-up time	t_{setup}		50			ns
SDA hold time	t_{hold}		50			ns
SCL high-pulse time	t_{pw}		2			μs
SCL low-pulse time	t_{nw}		2			μs



★ **Electrical Characteristics (Unless otherwise specified, V_{DD} = NPV_{DD} = PV_{DD} = LV_{DD} = BV_{DD} = 3.3 V, f_{OSC} = 700 kHz, T_A = 25°C)**

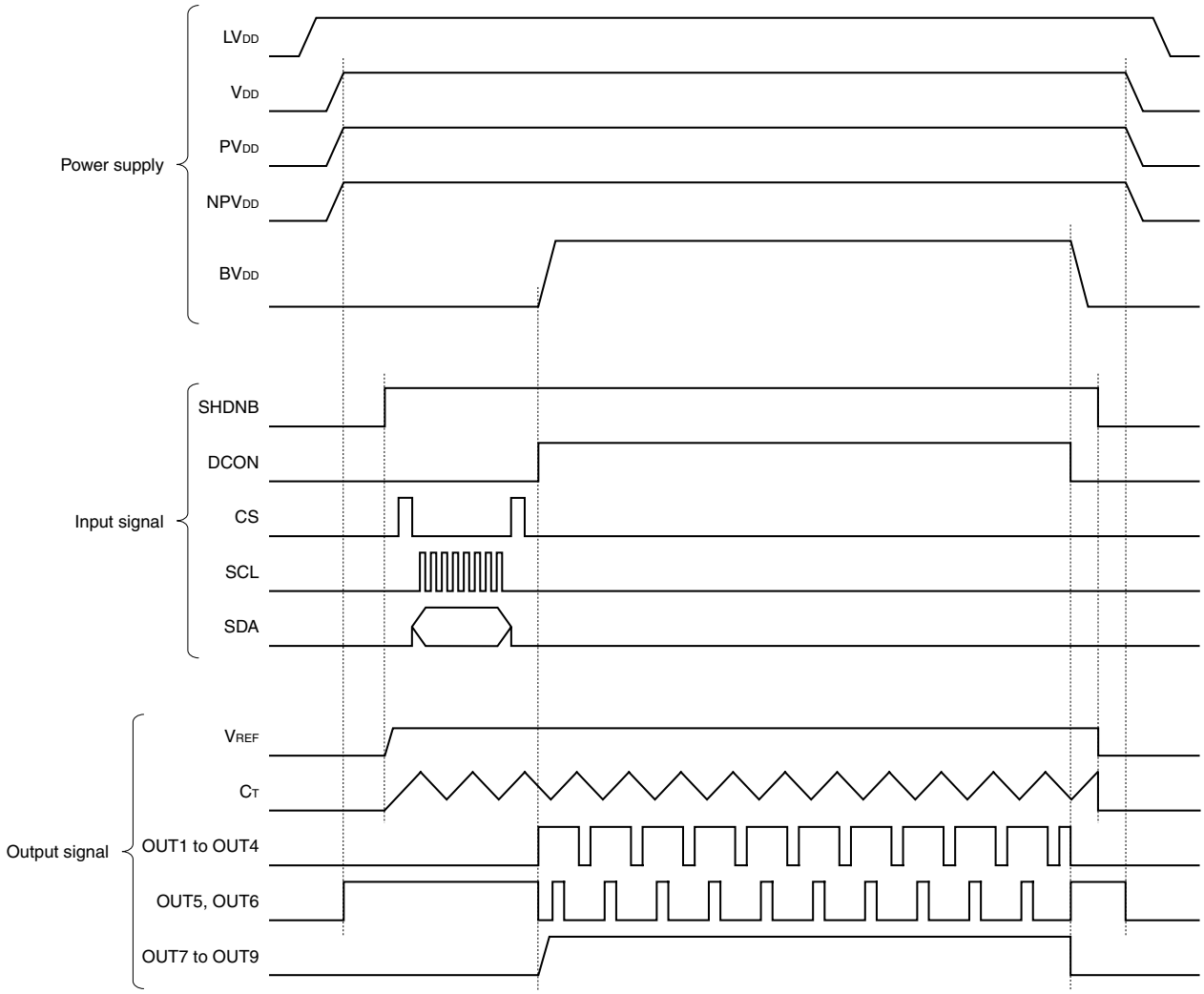
(1/2)

Overall						
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Shut-down current	$I_{DD(SHD)}$	SHDNB = L, V_{DD} + NPV_{DD} + PV_{DD} + BV_{DD} + LV_{DD}		5	8	μA
Standby current	$I_{DD(SB)}$	DCON = L, SHDNB = H, V_{DD} + NPV_{DD} + PV_{DD} + BV_{DD} + LV_{DD}		2.04	3.75	mA
Circuit operation current 1	I_{DD}	V_{DD}		2.04	3.75	mA
Circuit operation current 2	PI_{DD}	PV_{DD}, CL = 150 pF, FB = V_{DD}		3.0	5.7	mA
Circuit operation current 3	NPI_{DD}	NPV_{DD}, CL = 150 pF, FB = AGND		0.96	1.8	mA
Circuit operation current 4	BI_{DD}	BV_{DD}, no-load, I_I = BV_{DD}		180	345	μA
Circuit operation current 5	LI_{DD}	LV_{DD}		24	45	μA
Triangular Wave Oscillator Block						
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Oscillation frequency setting accuracy	f_{OSC}	C_{CT} = 150 pF, R_{RT} = 11 kΩ	−10		+10	%
Triangular wave low-level voltage	$V_{TH(L)}$			1.1		V
Triangular wave high-level voltage	$V_{TH(H)}$			1.8		V
Reference Voltage Block						
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Reference voltage	V_{REF}	I_{REF} = 1 mA	1.97	2.0	2.03	V
Maximum output current	I_{REF}			1	2	mA
PWM Comparator Block						
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Maximum duty 1-4	$D_{MAX.1-4}$	ch1 to ch4		85		%
Maximum duty 5-6	$D_{MAX.5-6}$	ch5 and ch6		85		%
Undervoltage Lockout Circuit Block						
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation start voltage at power application	$V_{DD(L-H)}$		1.01	1.45	1.89	V
Operation stop voltage	$V_{DD(H-L)}$		0.89	1.27	1.65	V
Hysteresis width	V_H		5	60		mV
Short-circuit Protection Circuit Block						
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FB detection voltage 1-4	$V_{TH(FB)1-4}$	FB (ch1 to ch4)	1.9	2	2.1	V
FB detection voltage 5-6	$V_{TH(FB)5-6}$	FB (ch5 and ch6)	0.76	0.8	0.84	V
DLY detection voltage	$V_{TH(DLY)}$	C_{DLY}	0.76	0.8	0.84	V
Short-circuit source current	I_{DLY}		1	2	4	μA

(2/2)

Soft Start Block						
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
C_{SS} detection voltage 1-4	$V_{TH(CSS)1-4}$	C_{SS1} to C_{SS4}	1.47	1.55	1.63	V
C_{SS} detection voltage 5-6	$V_{TH(CSS)5-6}$	C_{SS5} and C_{SS6}	0.79	1.35	1.59	V
Charge current	I_{CSS}		1	2	4	μA
Output Block (ch1 to ch6)						
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output turn-on resistance-p	R_{onp}	I_O = 15 mA		10	15	Ω
Output turn-off resistance-n	R_{onn}	I_O = 15 mA		10	15	Ω
E/A Block (ch1 to ch4)						
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
E/A1 input threshold voltage	V_{ITH1}	ch1OUT control bit is fixed to default setting (D [0:5] = 000000), offset is not included.	0.666	0.680	0.694	V
E/A2 input threshold voltage	V_{ITH2}	ch2OUT control bit is fixed to default setting (D [0:5] = 000000), offset is included.	0.680	0.700	0.720	V
E/A3 input threshold voltage	V_{ITH3}	ch3OUT control bit is fixed to default setting (D [0:5] = 000000), offset is not included.	0.666	0.680	0.694	V
E/A4 input threshold voltage	V_{ITH4}	Offset is not included.	0.980	1.000	1.020	V
E/A1 input offset voltage	V_{IOFF1}	V_{REF} = 2 V	0		40	mV
E/A3 input offset voltage	V_{IOFF3}		0		40	mV
E/A4 input offset voltage	V_{IOFF4}		0		40	mV
E/A Block (ch5 and ch6)						
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
E/A5 input threshold voltage	V_{ITH5}	Offset is not included.	0.980	1.000	1.020	V
E/A6 input threshold voltage	V_{ITH6}		0.980	1.000	1.020	V
E/A5 input offset voltage	V_{IOFF5}	V_{REF} = 2 V	0		40	mV
E/A6 input offset voltage	V_{IOFF6}		0		40	mV
E/A Block (ch7 to ch9)						
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
E/A7 input threshold voltage	V_{ITH7}	Offset is not included.	0.980	1.000	1.020	V
E/A8 input threshold voltage	V_{ITH8}		0.980	1.000	1.020	V
E/A9 input threshold voltage	V_{ITH9}		0.980	1.000	1.020	V
E/A7 input offset voltage	V_{IOFF7}	V_{REF} = 2 V	−10		30	mV
E/A8 input offset voltage	V_{IOFF8}		−10		30	mV
E/A9 input offset voltage	V_{IOFF9}		−10		30	mV
I/O differential voltage	V_{DIFF}	BV_{DD} – OUT7 to OUT9, I_O = 10 mA	1			V
Control Logic Block and Serial Interface Block						
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level input voltage	$V_{IH(L)}$	SHDNB, DCON, SDA, SCL, CS	LV_{DD} x 0.8			V
Low-level input voltage	$V_{IL(L)}$	SHDNB, DCON, SDA, SCL, CS			LV_{DD} x 0.2	V
Input leak current	I_L	SHDNB, DCON, SDA, SCL, CS, V_{IN} = AGND to LV_{DD}			1	V

5. TIMING CHART



6. I/O PIN EQUIVALENT CIRCUIT (Protection Circuit)

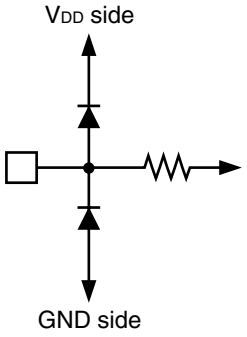
Pin No.	Symbol	Internal Circuit Configuration	Specified Protection Element	Power Supply Connection (refer to **Figure 6–1**)	
				V_{DD} Side	GND Side
1	OUT7	Analog output	Output protection 1	BV_{DD}	AGND, PGND
2	BV_{DD}	Power supply	Power supply protection	BV_{DD}	AGND, PGND
3	PGND4	Ground	Power supply protection	V_{DD}, PV_{DD}, NPV_{DD}, LV_{DD}	PGND
4	OUT4	Logic output	Output protection 1	PV_{DD}	AGND, PGND
5	PGND2	Ground	Power supply protection	V_{DD}, PV_{DD}, NPV_{DD}, LV_{DD}	PGND
6	OUT3	Logic output	Output protection 1	PV_{DD}	AGND, PGND
7	PV_{DD}	Power supply	Power supply protection	PV_{DD}	AGND, PGND
8	OUT2	Logic output	Output protection 1	PV_{DD}	AGND, PGND
9	PGND1	Ground	Power supply protection	V_{DD}, PV_{DD}, NPV_{DD}, LV_{DD}	AGND, PGND
10	OUT1	Logic output	Output protection 1	PV_{DD}	AGND, PGND
11	NPV_{DD}	Power supply	Power supply protection	NPV_{DD}	AGND, PGND
12	OUT5	Logic output	Output protection 1	NPV_{DD}	AGND, PGND
13	PGND3	Ground	Power supply protection	V_{DD}, PV_{DD}, NPV_{DD}, LV_{DD}	PGND
14	OUT6	Logic output	Output protection 1	NPV_{DD}	AGND, PGND
15	FB5	Analog output	Output protection 1	V_{DD}	AGND
16	I_{I5}	Gate input	Input protection 1	V_{DD}	AGND
17	C_{SS5}	Analog output	Output protection 1	V_{DD}	AGND
18	AGND1	Ground	Power supply protection	V_{DD}, PV_{DD}, NPV_{DD}, LV_{DD}	AGND
19	FB6	Analog output	Output protection 1	V_{DD}	AGND
20	I_{I6}	Gate input	Input protection 1	V_{DD}	AGND
21	C_{SS6}	Analog output	Output protection 1	V_{DD}	AGND
22	FB1	Analog output	Output protection 1	V_{DD}	AGND
23	I_{I1}	Gate input	Input protection 1	V_{DD}	AGND
24	C_{SS1}	Analog output	Output protection 2	V_{DD}	AGND
25	N.C.	–	–	–	–
26	FB2	Analog output	Output protection 1	V_{DD}	AGND
27	I_{I2}	Gate input	Input protection 1	V_{DD}	AGND
28	C_{SS2}	Analog output	Output protection 2	V_{DD}	AGND
29	N.C.	–	–	–	–
30	FB3	Analog output	Output protection 1	V_{DD}	AGND
31	I_{I3}	Gate input	Input protection 1	V_{DD}	AGND
32	C_{SS3}	Analog output	Output protection 2	V_{DD}	AGND
33	N.C.	–	–	–	–
34	V_{DD}	Power supply	Power supply protection	V_{DD}	AGND, PGND
35	FB4	Analog output	Output protection 1	V_{DD}	AGND
36	I_{I4}	Gate input	Input protection 1	V_{DD}	AGND
37	C_{SS4}	Analog output	Output protection 2	V_{DD}	AGND
38	C_T	Analog output	Output protection 2	V_{DD}	AGND
39	R_T	Analog output	Output protection 2	V_{DD}	AGND
40	V_{REF}	Analog output	Output protection 2	V_{DD}	AGND

(2/2)

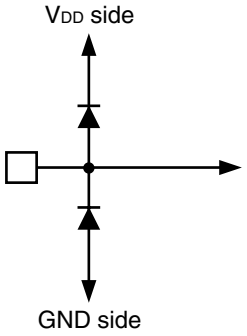
Pin No.	Symbol	Internal Circuit Configuration	Specified Protection Element	Power Supply Connection (refer to **Figure 6–1**)	
				V_{DD} Side	GND Side
41	C_{DLY}	Analog output	Output protection 2	V_{DD}	AGND
42	AGND2	Ground	Power supply protection	V_{DD}, PV_{DD}, NPV_{DD}, LV_{DD}	AGND
43	LV_{DD}	Power supply	Power supply protection	LV_{DD}	AGND, PGND
44	CS	Gate input	Input protection 1	LV_{DD}	AGND
45	SDA	Gate input	Input protection 1	LV_{DD}	AGND
46	SCL	Gate input	Input protection 1	LV_{DD}	AGND
47	SHDNB	Gate input	Input protection 1	LV_{DD}	AGND
48	TEST3	Gate input	Input protection 1	LV_{DD}	AGND
49	TEST1	Gate input	Input protection 1	LV_{DD}	AGND
50	TEST2	Gate input	Input protection 1	LV_{DD}	AGND
51	DCON	Gate input	Input protection 1	LV_{DD}	AGND
52	I_{I9}	Gate input	Input protection 1	BV_{DD}	AGND
53	OUT9	Analog output	Output protection 1	BV_{DD}	AGND, PGND
54	I_{I8}	Gate input	Input protection 1	BV_{DD}	AGND
55	OUT8	Analog output	Output protection 1	BV_{DD}	AGND, PGND
56	I_{I7}	Gate input	Input protection 1	BV_{DD}	AGND

Figure 6–1.

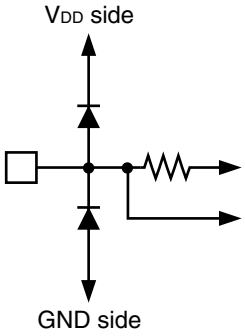
Input Protection 1



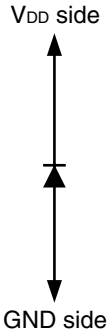
Output Protection 1



Output Protection 2



Power Supply Protection



7. CONTROL LOGIC BLOCK

7.1 SHDNB Pin (Pin No. 47)

The internal circuits (E/A, PWM comparator, triangular wave oscillator) are stopped by the SHDNB pin and the serial interface registers are reset. The capacitor connected between the C_{SS1} to C_{SS6} pins also discharges.

SHDNB	State of IC	Serial Interface
L	Shut down (OUT1 to OUT4 = fixed to GND, OUT5 and OUT6 = fixed to V_{DD}, and OUT7 to OUT9 = fixed to GND)	Input disable
H	ON	Input enable

7.2 DCON Pin (Pin No. 51)

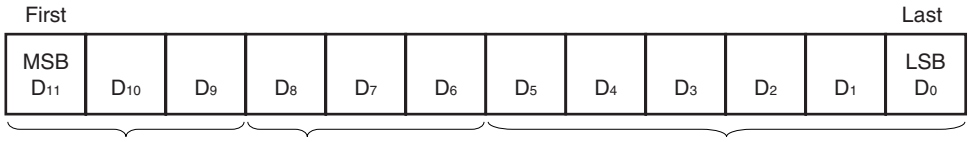
The outputs are switched OFF by the DCON pin while the internal circuits are operating (serial interface input possible). The capacitor connected between the C_{SS1} to C_{SS6} pins also discharges.

DCON	State of IC	Serial Interface
L	Standby (All channel output turns off, and the internal circuits operate.) (OUT1 to OUT4 = fixed to GND, OUT5 and OUT6 = fixed to V_{DD}, and OUT7 to OUT9 = fixed to GND)	Input enable
H	The channel specified by ON/OFF control bit of the serial interface turns on.	

8. SERIAL INTERFACE BLOCK

8.1 Control Data (Default = All "0")

Data is the turn of D_{11}, D_{10}, D_9, ···, and D_0, and please input it.



Output voltage control bit

D_5	D_4	D_3	D_2	D_1	D_0	Output Voltage
0	0	0	0	0	0	Refer to **8.2 Details of Output Voltage Control Bits**.
0	0	0	0	0	1	
⋮	⋮	⋮	⋮	⋮	⋮	
1	1	1	1	1	0	
1	1	1	1	1	1	

Unused

Output voltage control bit

D_{11}	D_{10}	D_9	Input Data	Output
0	0	0	Unused	–
0	0	1	ch1 output voltage	ch1OUT
0	1	0	ch2 output voltage	ch2OUT
0	1	1	ch3 output voltage	ch3OUT
1	0	0	Unused	–
1	0	1	ON/OFF control 1	ch1OUT to ch6OUT
1	1	0	ON/OFF control 2	ch7OUT to ch9OUT
1	1	1	Unused	–

8.2 Details of Output Voltage Control Bits

Input data configuration of input address control bit

D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	1	Unused			ch1 output voltage					

Table 8–1. ch1 Output Voltage (ch1OUT) Control Bit

D_5	D_4	D_3	D_2	D_1	D_0	E/A1 Threshold Voltage TYP. V_{ITH1} [V]
0	0	0	0	0	0	0.68
0	0	0	0	0	1	0.69
0	0	0	0	1	0	0.70
0	0	0	0	1	1	0.71
0	0	0	1	0	0	0.72
0	0	0	1	0	1	0.73
0	0	0	1	1	0	0.74
0	0	0	1	1	1	0.75
0	0	1	0	0	0	0.76
0	0	1	0	0	1	0.77
0	0	1	0	1	0	0.78
0	0	1	0	1	1	0.79
0	0	1	1	0	0	0.80
0	0	1	1	0	1	0.81
0	0	1	1	1	0	0.82
0	0	1	1	1	1	0.83
0	1	0	0	0	0	0.84
0	1	0	0	0	1	0.85
0	1	0	0	1	0	0.86
0	1	0	0	1	1	0.87
0	1	0	1	0	0	0.88
0	1	0	1	0	1	0.89
0	1	0	1	1	0	0.90
0	1	0	1	1	1	0.91
0	1	1	0	0	0	0.92
0	1	1	0	0	1	0.93
0	1	1	0	1	0	0.94
0	1	1	0	1	1	0.95
0	1	1	1	0	0	0.96
0	1	1	1	0	1	0.97
0	1	1	1	1	0	0.98
0	1	1	1	1	1	0.99
1	0	0	0	0	0	1.00
1	0	0	0	0	1	1.01
1	0	0	0	1	0	1.02
1	0	0	0	1	1	1.03
1	0	0	1	0	0	1.04
1	0	0	1	0	1	1.05
1	0	0	1	1	0	1.06
1	0	0	1	1	1	1.07
1	0	1	0	0	0	1.08
1	0	1	0	0	1	1.09
1	0	1	0	1	0	1.10
1	0	1	0	1	1	1.11
1	0	1	1	0	0	1.12
1	0	1	1	0	1	1.13
1	0	1	1	1	0	1.14
1	0	1	1	1	1	1.15
1	1	0	0	0	0	1.16
1	1	0	0	0	1	1.17
1	1	0	0	1	0	1.18
1	1	0	0	1	1	1.19
1	1	0	1	0	0	1.20
1	1	0	1	0	1	1.21
1	1	0	1	1	0	1.22
1	1	0	1	1	1	1.23
1	1	1	0	0	0	1.24
1	1	1	0	0	1	1.25
1	1	1	0	1	0	1.26
1	1	1	0	1	1	1.27
1	1	1	1	0	0	1.28
1	1	1	1	0	1	1.29
1	1	1	1	1	0	1.30
1	1	1	1	1	1	1.31

Caution The output voltage value becomes ch1OUT ≅ V_{ITH1} x ((R11 + R12) /R12).

Input data configuration of input address control bit

D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	0	Unused			ch2 output voltage					

Table 8–2. ch2 Output Voltage (ch2OUT) Control Bit

D_5	D_4	D_3	D_2	D_1	D_0	E/A2 Threshold VoltageTYP. V_{ITH2} [V]
0	0	0	0	0	0	0.68
0	0	0	0	0	1	0.69
0	0	0	0	1	0	0.70
0	0	0	0	1	1	0.71
0	0	0	1	0	0	0.72
0	0	0	1	0	1	0.73
0	0	0	1	1	0	0.74
0	0	0	1	1	1	0.75
0	0	1	0	0	0	0.76
0	0	1	0	0	1	0.77
0	0	1	0	1	0	0.78
0	0	1	0	1	1	0.79
0	0	1	1	0	0	0.80
0	0	1	1	0	1	0.81
0	0	1	1	1	0	0.82
0	0	1	1	1	1	0.83
0	1	0	0	0	0	0.84
0	1	0	0	0	1	0.85
0	1	0	0	1	0	0.86
0	1	0	0	1	1	0.87
0	1	0	1	0	0	0.88
0	1	0	1	0	1	0.89
0	1	0	1	1	0	0.90
0	1	0	1	1	1	0.91
0	1	1	0	0	0	0.92
0	1	1	0	0	1	0.93
0	1	1	0	1	0	0.94
0	1	1	0	1	1	0.95
0	1	1	1	0	0	0.96
0	1	1	1	0	1	0.97
0	1	1	1	1	0	0.98
0	1	1	1	1	1	0.99
1	0	0	0	0	0	1.00
1	0	0	0	0	1	1.01
1	0	0	0	1	0	1.02
1	0	0	0	1	1	1.03
1	0	0	1	0	0	1.04
1	0	0	1	0	1	1.05
1	0	0	1	1	0	1.06
1	0	0	1	1	1	1.07
1	0	1	0	0	0	1.08
1	0	1	0	0	1	1.09
1	0	1	0	1	0	1.10
1	0	1	0	1	1	1.11
1	0	1	1	0	0	1.12
1	0	1	1	0	1	1.13
1	0	1	1	1	0	1.14
1	0	1	1	1	1	1.15
1	1	0	0	0	0	1.16
1	1	0	0	0	1	1.17
1	1	0	0	1	0	1.18
1	1	0	0	1	1	1.19
1	1	0	1	0	0	1.20
1	1	0	1	0	1	1.21
1	1	0	1	1	0	1.22
1	1	0	1	1	1	1.23
1	1	1	0	0	0	1.24
1	1	1	0	0	1	1.25
1	1	1	0	1	0	1.26
1	1	1	0	1	1	1.27
1	1	1	1	0	0	1.28
1	1	1	1	0	1	1.29
1	1	1	1	1	0	1.30
1	1	1	1	1	1	1.31

Caution The output voltage value becomes ch2OUT ≅ V_{ITH2} x ((R21 + R22) /R22).

Input data configuration of input address control bit

D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	1	1	Unused			ch3 output voltage					

Table 8–3. ch3 Output Voltage (ch3OUT) Control Bit

D_5	D_4	D_3	D_2	D_1	D_0	E/A3 Threshold Voltage TYP. V_{ITH3} [V]
0	0	0	0	0	0	0.68
0	0	0	0	0	1	0.69
0	0	0	0	1	0	0.70
0	0	0	0	1	1	0.71
0	0	0	1	0	0	0.72
0	0	0	1	0	1	0.73
0	0	0	1	1	0	0.74
0	0	0	1	1	1	0.75
0	0	1	0	0	0	0.76
0	0	1	0	0	1	0.77
0	0	1	0	1	0	0.78
0	0	1	0	1	1	0.79
0	0	1	1	0	0	0.80
0	0	1	1	0	1	0.81
0	0	1	1	1	0	0.82
0	0	1	1	1	1	0.83
0	1	0	0	0	0	0.84
0	1	0	0	0	1	0.85
0	1	0	0	1	0	0.86
0	1	0	0	1	1	0.87
0	1	0	1	0	0	0.88
0	1	0	1	0	1	0.89
0	1	0	1	1	0	0.90
0	1	0	1	1	1	0.91
0	1	1	0	0	0	0.92
0	1	1	0	0	1	0.93
0	1	1	0	1	0	0.94
0	1	1	0	1	1	0.95
0	1	1	1	0	0	0.96
0	1	1	1	0	1	0.97
0	1	1	1	1	0	0.98
0	1	1	1	1	1	0.99
1	0	0	0	0	0	1.00
1	0	0	0	0	1	1.01
1	0	0	0	1	0	1.02
1	0	0	0	1	1	1.03
1	0	0	1	0	0	1.04
1	0	0	1	0	1	1.05
1	0	0	1	1	0	1.06
1	0	0	1	1	1	1.07
1	0	1	0	0	0	1.08
1	0	1	0	0	1	1.09
1	0	1	0	1	0	1.10
1	0	1	0	1	1	1.11
1	0	1	1	0	0	1.12
1	0	1	1	0	1	1.13
1	0	1	1	1	0	1.14
1	0	1	1	1	1	1.15
1	1	0	0	0	0	1.16
1	1	0	0	0	1	1.17
1	1	0	0	1	0	1.18
1	1	0	0	1	1	1.19
1	1	0	1	0	0	1.20
1	1	0	1	0	1	1.21
1	1	0	1	1	0	1.22
1	1	0	1	1	1	1.23
1	1	1	0	0	0	1.24
1	1	1	0	0	1	1.25
1	1	1	0	1	0	1.26
1	1	1	0	1	1	1.27
1	1	1	1	0	0	1.28
1	1	1	1	0	1	1.29
1	1	1	1	1	0	1.30
1	1	1	1	1	1	1.31

Caution The output voltage value becomes ch3OUT ≅ V_{ITH3} x ((R31 + R32) /R32).

Input data configuration of input address control bit

D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	1	Unused			ON/OFF control 1					
1	1	0	Unused			ON/OFF control 2					

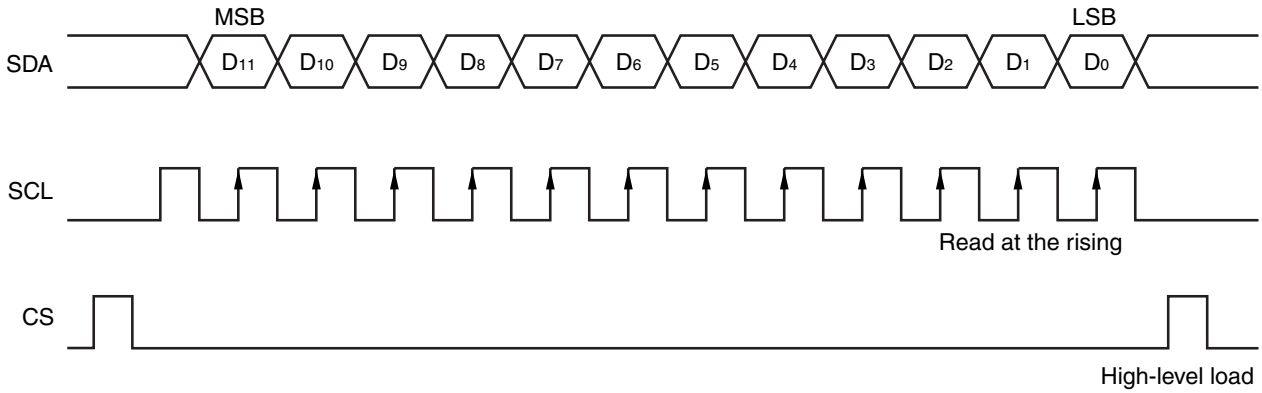
• ON/OFF control bit 1

Input Data	D_5	D_4	D_3	D_2	D_1	D_0
	Output of ch6	Output of ch5	Output of ch4	Output of ch3	Output of ch2	Output of ch1
0	ON					
1	OFF (E/A and PWM operation stop)					

• ON/OFF control bit 2

Input Data	D_5	D_4	D_3	D_2	D_1	D_0
	Unused	Unused	Unused	Output of ch9	Output of ch8	Output of ch7
0	–			ON		
1	–			OFF (E/A and PWM operation stop)		

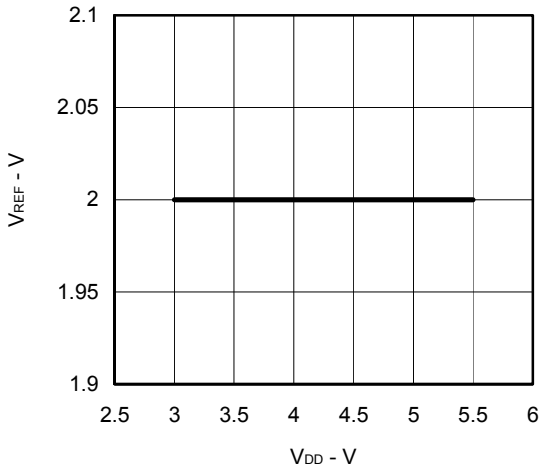
8.3 Serial Correspondence Timing



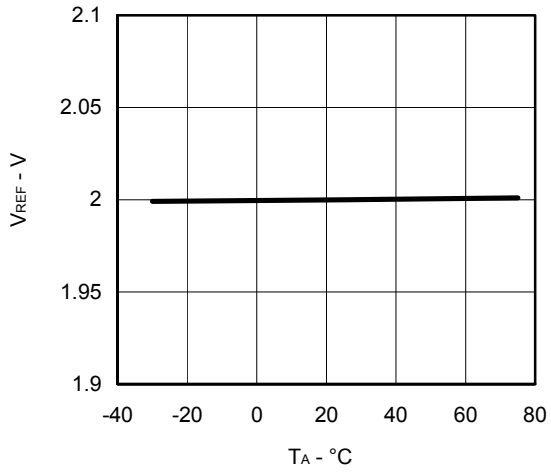
- The 12-bit serial data inputted by the SDA pin is loaded to the shift register at the rising edge of the signal inputted to the SCL pin. The loaded data is loaded to the shift register at the rising edge of the signal inputted to the CS pin. Be sure to fix the signal input to the SCL pin to low level at the rising and falling edges of the signal input to the CS pin.
- If the data which is loaded to shift register while the CS pin is low level is less than 12 bits, the loaded data is cancelled. If the loaded data is more than 12 bits, the 12-bit data is valid in the last of the loaded data.

★ 9. TYPICAL CHARACTERISTICS (Unless Otherwise Specified, V_{DD} = NPV_{DD} = PV_{DD} = LV_{DD} = BV_{DD} = 3.3 V, f_{OSC} = 700 kHz, T_A = 25°C, Reference Value)

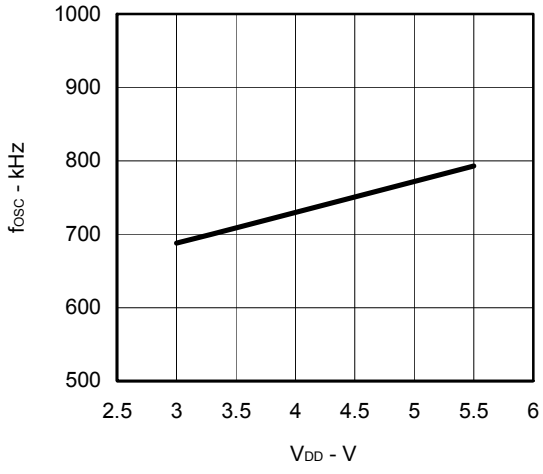
V_{REF} vs. V_{DD}



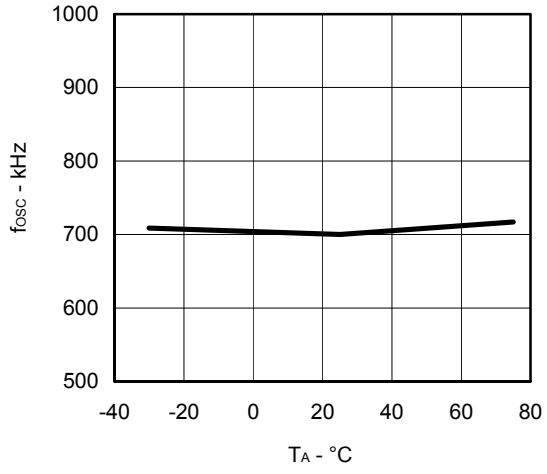
V_{REF} vs. T_A



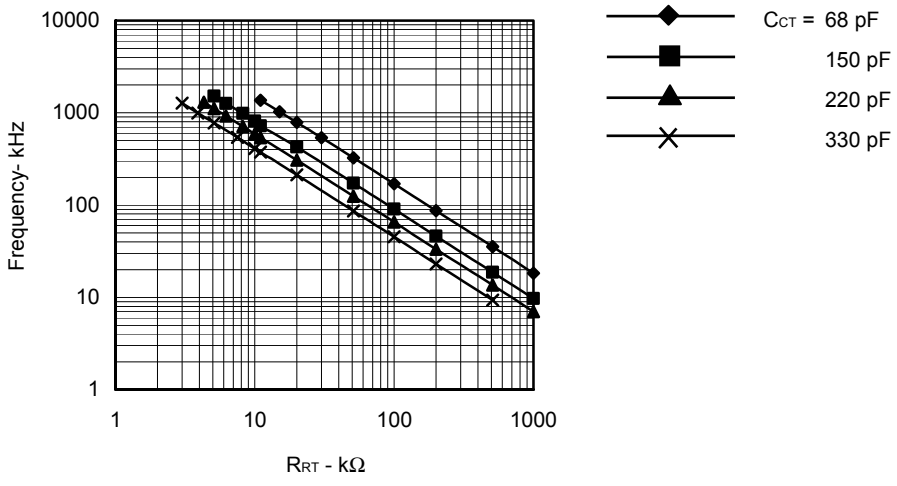
f_{OSC} vs. V_{DD}



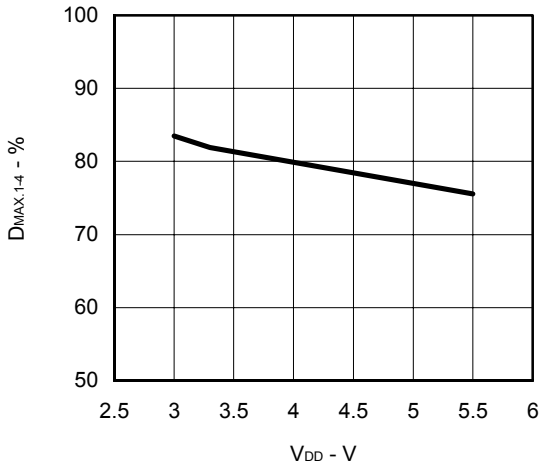
f_{OSC} vs. T_A



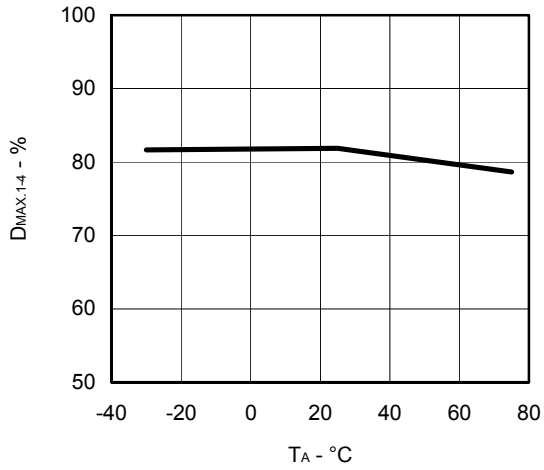
f_{OSC} vs. R_{RT}



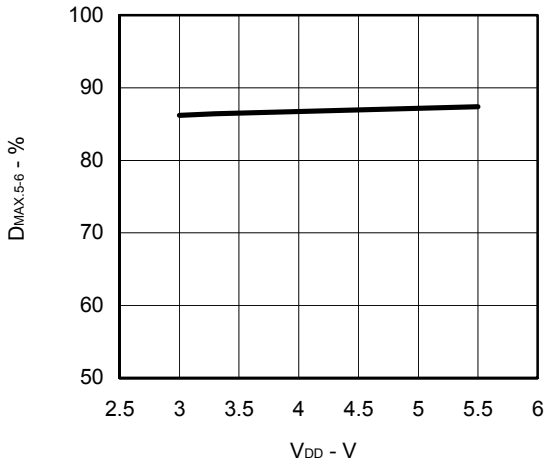
$D_{MAX.1-4}$ vs. V_{DD}



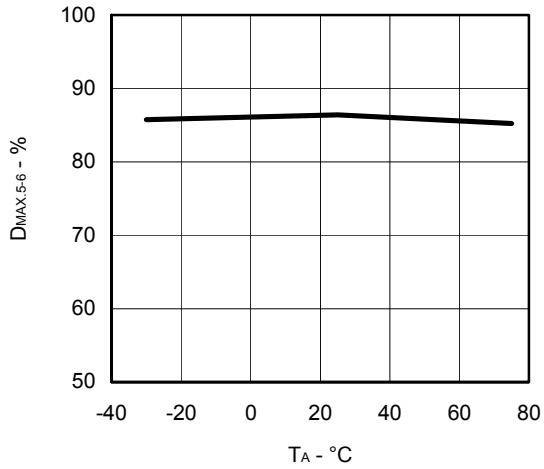
$D_{MAX.1-4}$ vs. T_A



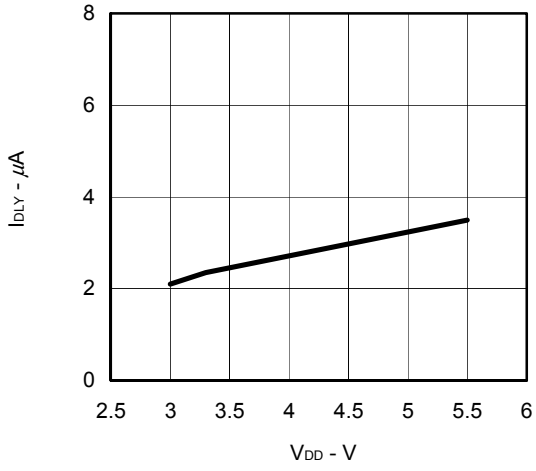
$D_{MAX.5-6}$ vs. V_{DD}



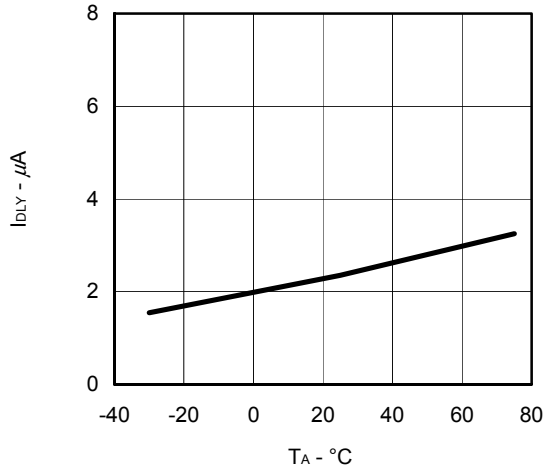
$D_{MAX.5-6}$ vs. T_A



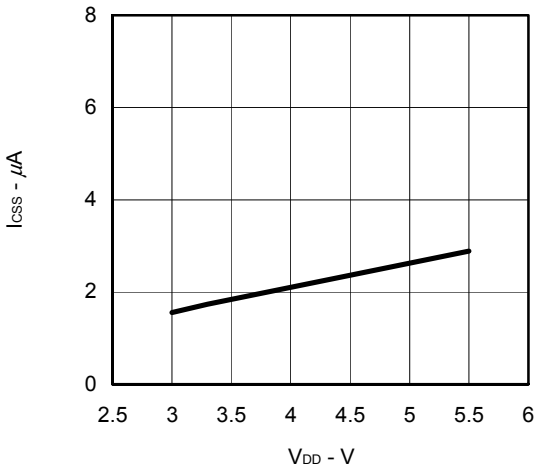
I_{DLY} vs. V_{DD}



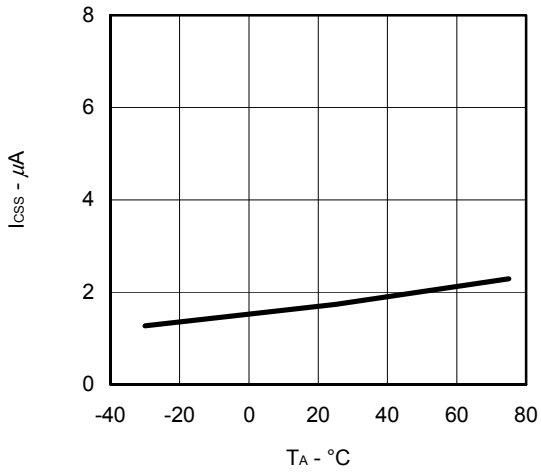
I_{DLY} vs. T_A



I_{CSS} vs. V_{DD}



I_{CSS} vs. T_A



10. OPERATION EXPLANATION OF EACH BLOCK

10.1 Reference Voltage Circuit Block

The reference voltage circuit block outputs reference voltage (2.0 V TYP.) by which temperature compensation is carried out by supplying voltage by the V_{DD} (No. 34) pin. The reference voltage is used as the reference voltage of each internal circuit, and can be extracted to outside by the V_{REF} (No. 40) pin to 1 mA TYP..

10.2 Triangular Wave Oscillator Block

The triangular wave oscillator block performs self-excited oscillation using the timing capacitance and timing resistor externally attached to the C_T (No. 38) pin and R_T (No. 39) pin, respectively, and outputs a symmetric triangular wave with an amplitude of 1.1 to 1.8 V TYP. to the C_T (No. 38) pin.

This triangular wave is supplied to the inversion input pin of the PWM comparator.

10.3 E/A Block

The input threshold voltage of E/A is the voltage set by the output voltage control bit of the serial interface for E/A1 to E/A3 (default = all zero; 0.68 V TYP.), and 1.0 V TYP. for E/A4 to E/A9.

Note that E/A7 to E/A9 operate as a series regulator.

10.4 PWM Comparator Block

The PWM comparator compares the triangular wave signal and E/A output signal (or maximum duty) and controls the output ON duty.

10.5 Output Circuit Block

The output circuit block of ch1 to ch6 is of push-pull configuration and can directly drive a Power MOS FET. The output current capacity is 200 mA MAX. for pulse output and 20 mA MAX. for DC output.

The output current capacity of the output circuit block of ch7 to ch9 is 20 mA MAX. for DC output

10.6 Undervoltage Lockout Circuit Block

The undervoltage lockout circuit block shuts down the IC if the power supply voltage is insufficient at power application or shut down in order to prevent malfunction of the IC.

10.7 Soft Start Block of the Step-up DC-DC Converter Output (ch1 to ch4)

ch1 is soft-started by a capacitor connected to the C_{SS1} (No. 24) pin. Also, ch2 to ch4 are respectively soft-started by a capacitor connected to the C_{SS2} (No. 28) pin, C_{SS3} (No. 32) pin, and C_{SS4} (No. 37) pin.

Soft start is executed by charging the capacitor connected to each C_{SS} pin and gradually increasing the voltage at the C_{SS} pin. On starting the IC, the voltage at each C_{SS} pin is connected to the non-inverted input of E/A. Soft start is executed by increasing the non-inverted input voltage of E/A from 0 V and gradually prolonging the output ON duty. (**Figure 10–1** and **10–2**)

Figure 10–1.

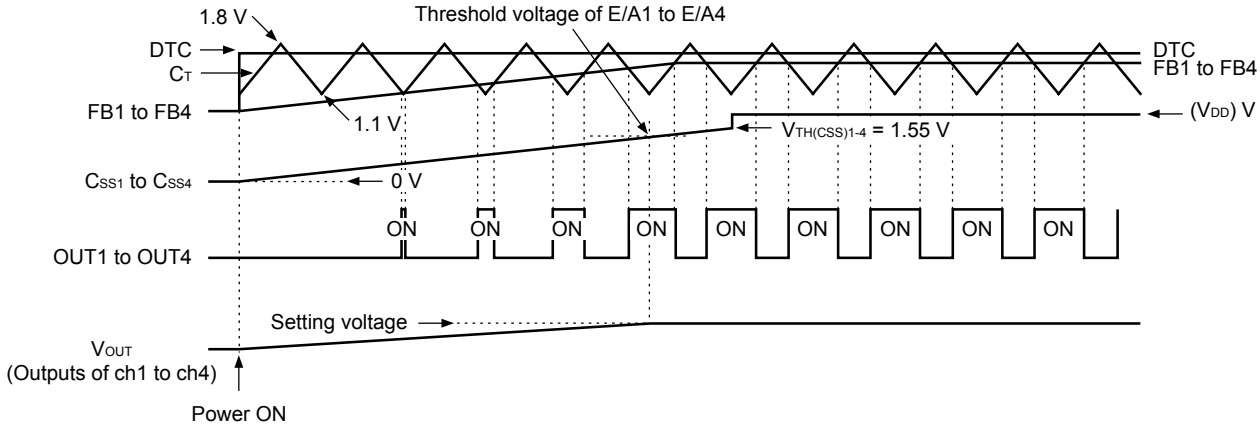
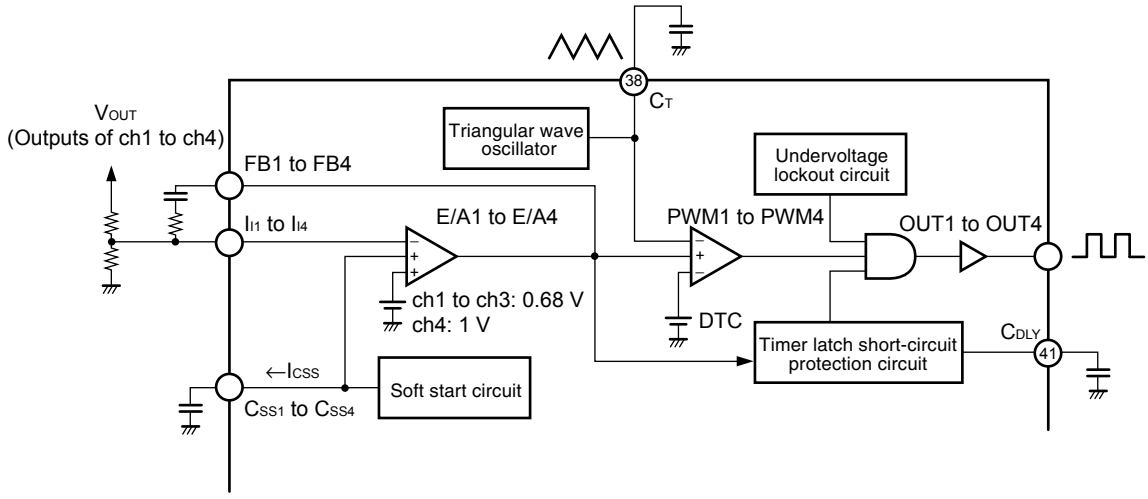


Figure 10–2.



10.8 Soft Start Block of the Polarity-inverted DC-DC Converter Output (ch5 and ch6)

ch5 is soft-started by a capacitor connected to the C_{SS5} (No. 17) pin. Also, ch6 is soft-started by a capacitor connected to the C_{SS6} (No. 21) pin.

Soft start is executed by charging the capacitor connected to each C_{SS} pin and gradually increasing the voltage at the C_{SS} pin. The C_{SS} pin voltage is connected to the PWM non-inverted input (DTC) via a 200 kΩ resistor. At startup, raising the PWM non-inverted input (DTC) voltage from about 0.4 gradually lengthens the output ON duty, causing a soft start (**Figure 10–3** and **10–4**).

Note that if the DTC voltage and FB voltage are switched while the output ON duty is still small (less than 50%) following a soft start, inrush current may occur at the point of switching. In this case, suppress the inrush current by either raising the operating frequency or increasing the inductance of the coil used by the DC-DC converter.

Figure 10–3.

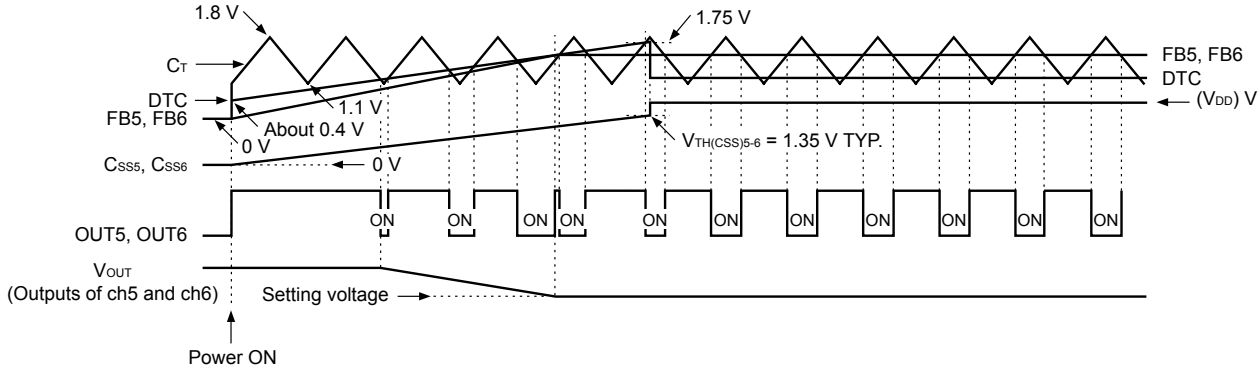
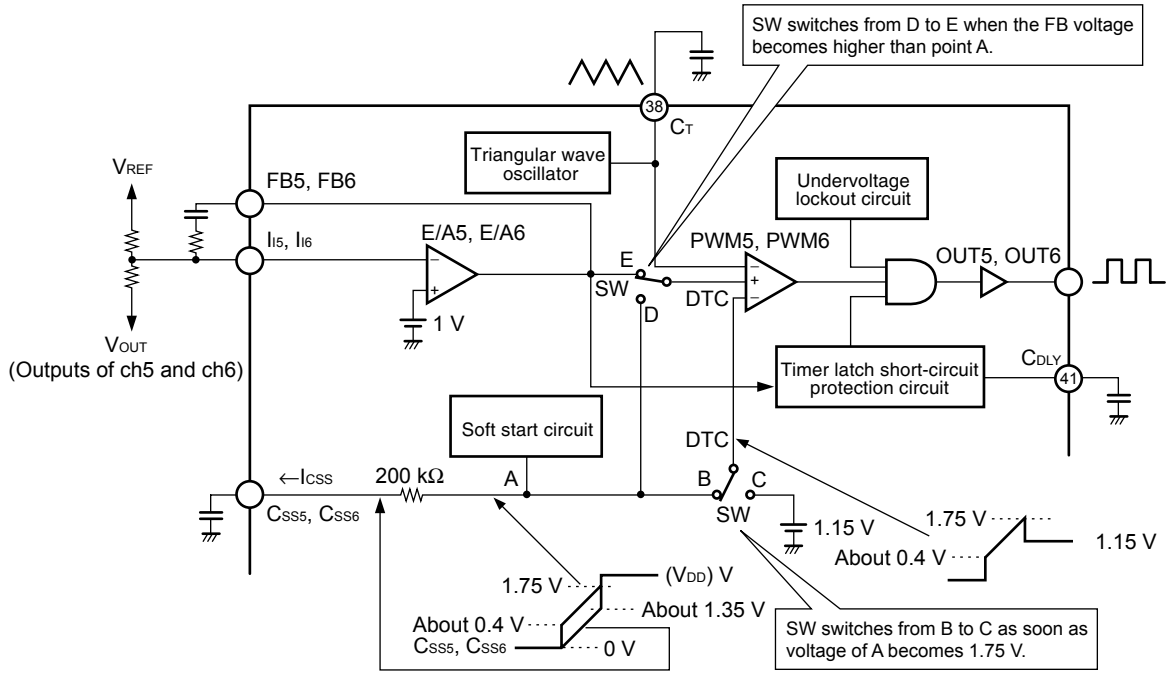


Figure 10–4.



10.9 Short-circuit Protection Circuit Block (Timer latch type)

If the voltage of ch1 to ch4, which are the step-up DC-DC converter outputs, drops, the voltage of the inversion input pin of the E/A, which is feeding back the output, also drops, and the E/A output (FB) is stepped up. If the voltage of this E/A output (FB) reaches or exceeds the FB detection voltage of the short-circuit protection circuit ($V_{TH(FB)1-4}$ = 2.0 V TYP.), the timer circuit starts operating and the capacitor connected to the C_{DLY} (No. 41) pin starts charging. When the voltage of the capacitor connected the C_{DLY} (No. 41) pin reaches the C_{DLY} protection voltage ($V_{TH(DLY)}$ = 0.8 V TYP.), all the outputs of the IC are latched to OFF (**Figure 10–5** and **10–6**).

If the voltage of ch5 and ch6, which are the polarity-inverted DC-DC converter outputs, is stepped up, the voltage of the inversion input pin of the E/A, which is feeding back the output, is also stepped up, and the E/A output (FB) is stepped down. If the voltage of this E/A output (FB) falls below the FB detection voltage of the short-circuit protection circuit ($V_{TH(FB)5-6}$ = 0.8 V TYP.), the timer circuit starts operating and the capacitor connected to the C_{DLY} (No. 41) pin starts charging. When the voltage of the capacitor connected to the C_{DLY} (No. 41) pin reaches the C_{DLY} detection voltage ($V_{TH(DLY)}$ = 0.8 V TYP.), all the outputs of the IC are latched to OFF (**Figure 10–5** and **10–7**).

As long as the E/A output (FB) of any of ch1 to ch6 is at least the FB detection voltage of the short-circuit protection circuit, the capacitor connected to the C_{DLY} (No. 41) pin continues to charge. (**Figure 10–8**)

To reset the latch circuit when the short-circuit protection circuit is activated, decrease the supply voltage (V_{DD}) to the operation stop voltage level ($V_{DD(H-L)}$ = 1.39 V TYP.), or set the SHDNB (No. 47) pin or DCON (No. 51) pin to low level.

Figure 10–5.

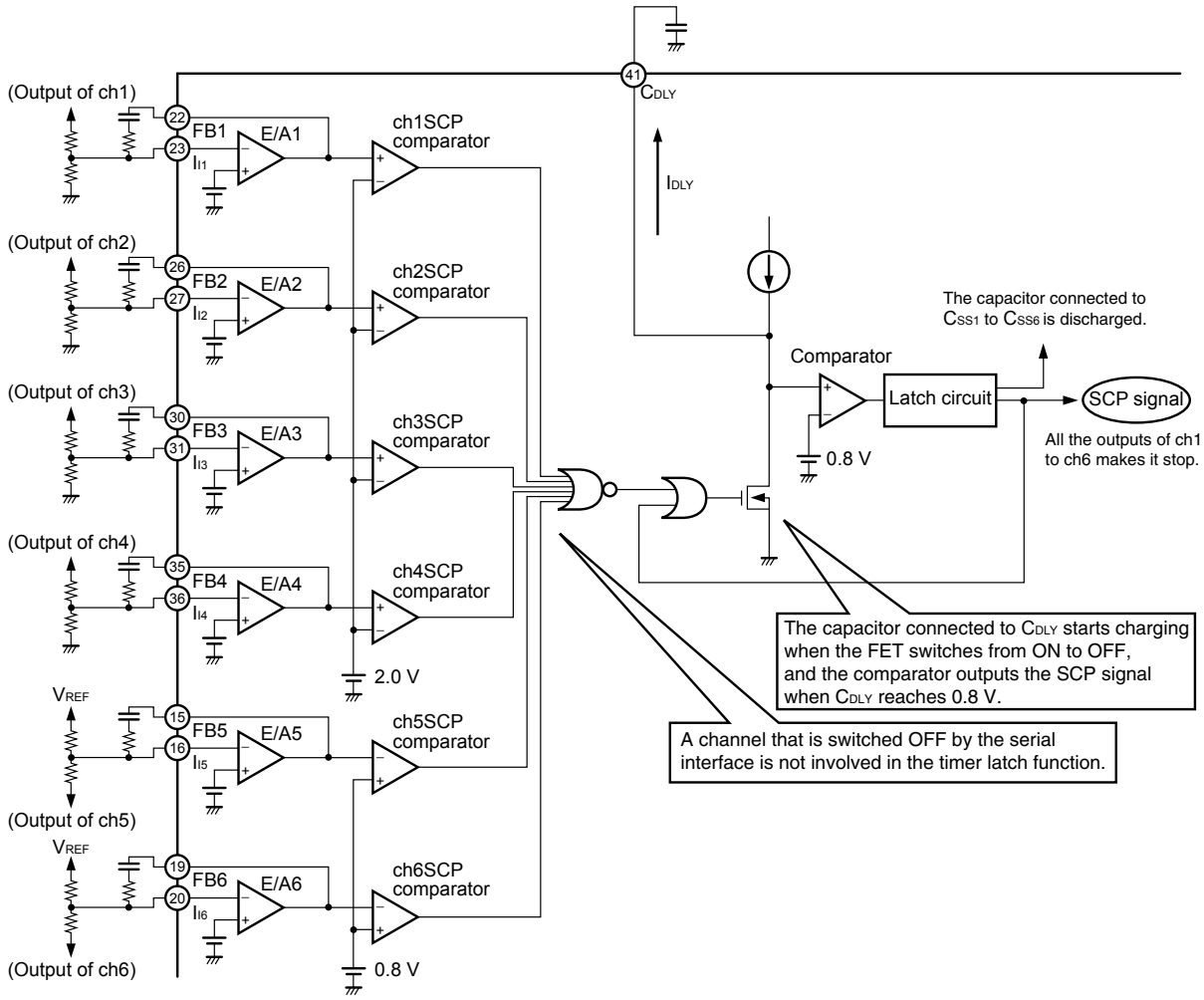


Figure 10–6.

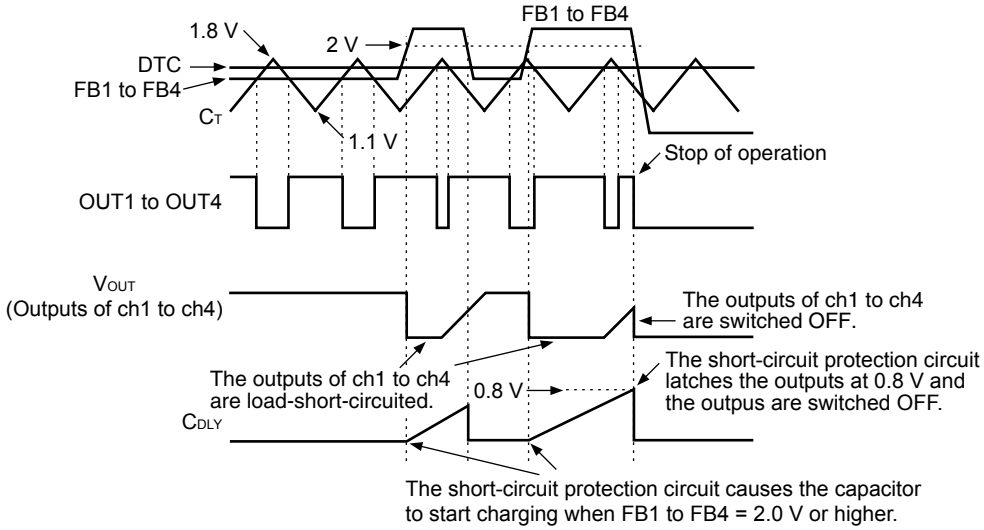


Figure 10–7.

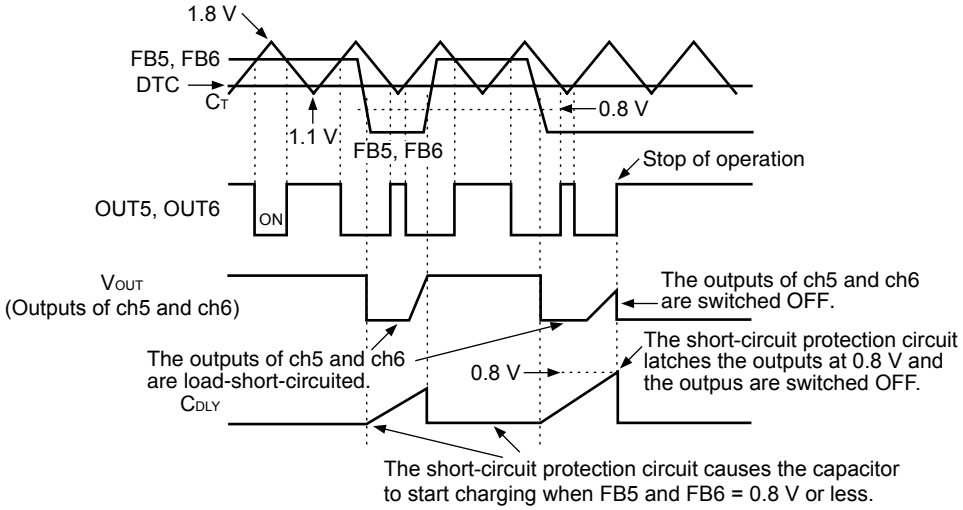
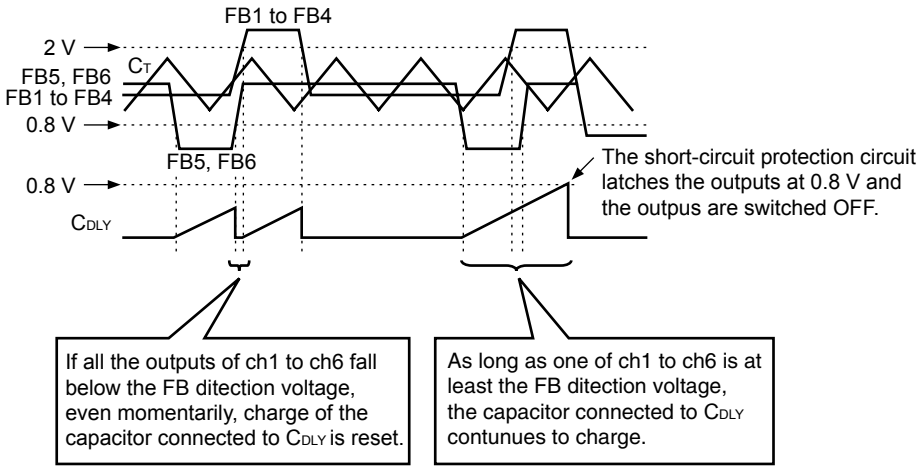


Figure 10–8.



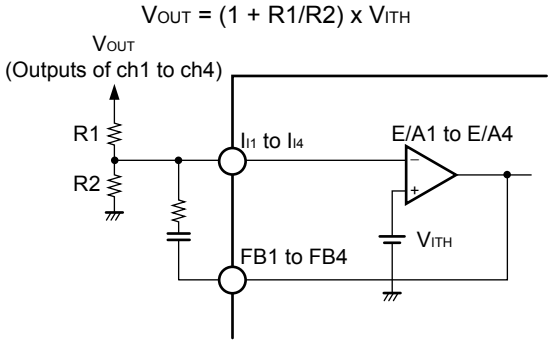
11. NOTES ON USE

11.1 Method of Setting Output Voltage

The method of setting the output voltage of ch1 to ch4 is shown in **Figure 11–1**, the method of setting the output voltage of ch5 and ch6 is shown in **Figure 11–2**, and the method of setting the output voltage of ch5 to ch7 is shown in **Figure 11–3**.

The output voltage can be calculated by using the expression in the figure.

Figure 11–1. The Method of Setting the Output Voltage of the Step-up Circuit of ch1 to ch4



Caution V_{ITH} of ch1 to ch3 depends on the serial interface.
V_{ITH} of ch4 is 1.0 V TYP..

Figure 11–2. The Method of Setting the Output Voltage of the Polarity-inverted Circuit of ch5 and ch6

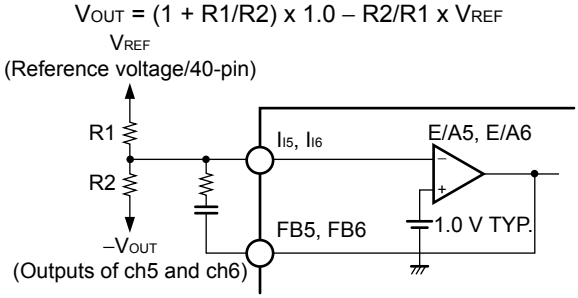
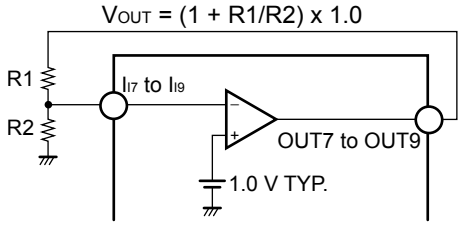


Figure 11–3. The Method of Setting the Output Voltage of ch7 to ch9



11.2 Method of Handling Pins of Unused Channels

Figure 11–4 to **11–8** show how to handle the pins when not using ch1 to ch3, ch5 and ch6, ch7 to ch9, and the serial interface, respectively.

Figure 11–4. Handling of Pins When Not Using ch1 to ch3

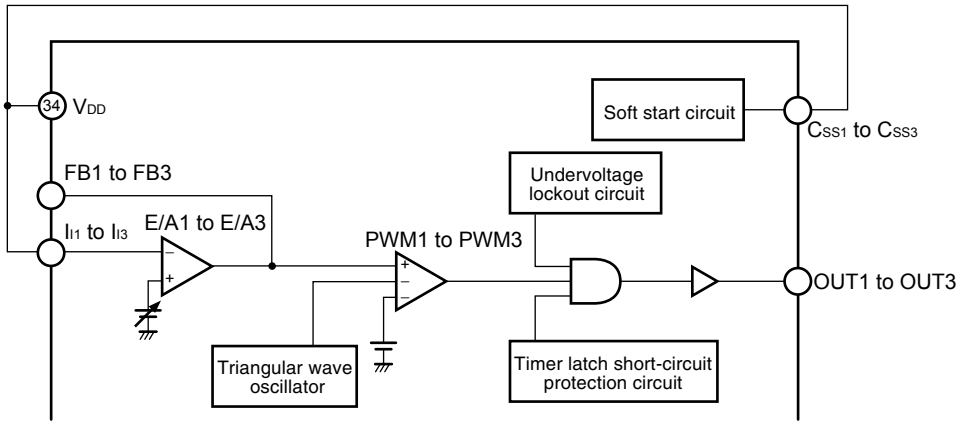


Figure 11–5. Handling of Pins When Not Using ch4

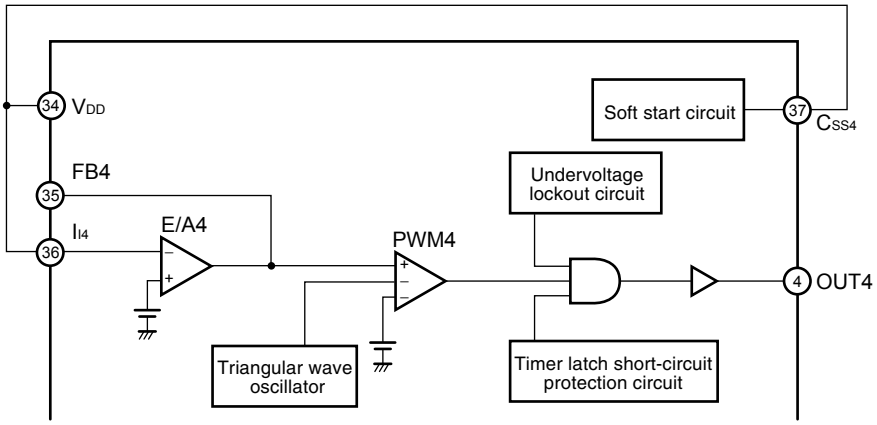


Figure 11–6. Handling of Pins When Not Using ch5 and ch6

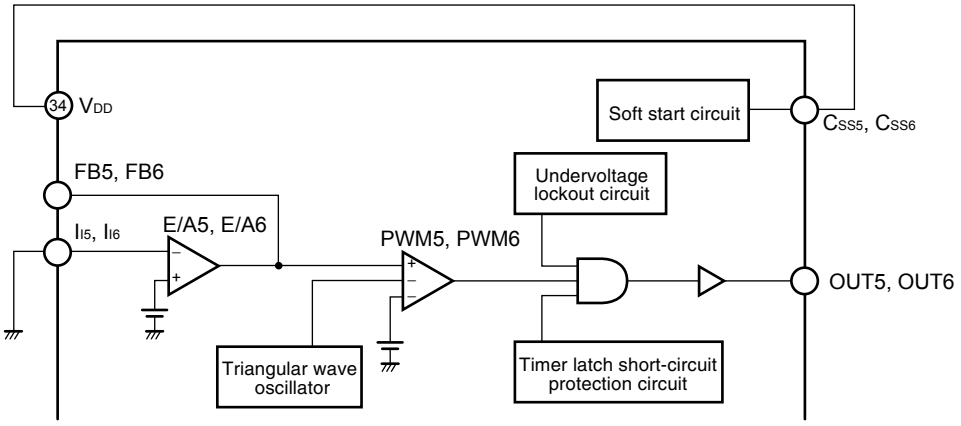


Figure 11–7. Handling of Pins When Not Using ch7 to ch9

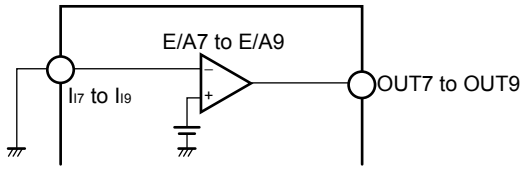
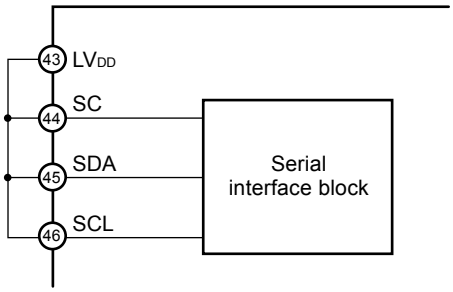


Figure 11–8. Handling of Pins When Not Using the Serial Interface



11.3 Method of Setting Oscillation Frequency

The oscillation frequency can be arbitrarily set by the timing resistor (R_{RT}) connected to the R_T (No. 39) pin, and the timing capacitance (C_{CT}) value connected to the C_T (No. 38) pin.

Expression <1> shows an approximate expression of the oscillation frequency (f_{OSC}). However, because this is an approximate expression, be sure to check the frequency on the actual device, especially when using a high frequency.

f_{OSC} [Hz] = 1.43/ (R_{RT} [Ω] x C_{CT} [F]) ····· <1>

11.4 Method of Setting Soft-start Time

Expression <2> shows an approximate expression of the soft-start charge time of ch1 to ch4, t_{SS1} to t_{SS4}.

t_{SS1} to t_{SS4} [s] = 0.775 x C_{SS} [μF] ····· <2>

Expression <3> shows an approximate expression of the soft-start charge time of ch5 and ch6, t_{SS5} and t_{SS6}.

t_{SS5} and t_{SS6} [s] = 0.675 x C_{SS} [μF] ····· <3>

Note, however, that the startup characteristics of each channel differ depending on the load conditions of that channel, as mentioned in **10.7 Soft Start Block of the Step-up DC-DC Converter Output (ch1 to ch4) (Figure 10–1),** and **10.8 Soft Start Block of the Polarity-inverted DC-DC Converter Output (ch5 and ch6) (Figure 10–3)**,so t_{SS} does not equal the rise time of the output voltage of each channel. Therefore, be sure to check the soft-start time on the actual device.

11.5 Method of Calculating Delay Time of Short-circuit Protection Circuit

Expression <4> shows an approximate expression of the short-circuit protection circuit delay time, t_{DLY}.

t_{DLY} [s] = 0.4 x C_{DLY} [μF] ····· <4>

11.6 Method of Handling Pins When Short-circuit Protection Circuit is Unused

When the short-circuit protection circuit is unused, connected the C_{DLY} (No. 41) pin to the AGND (No. 18 and 42) pin.

11.7 Method of Preventing Malfunction of Short-circuit Protection Circuit

If noise is superimposed on the C_{DLY} (No. 41) pin, the internal latch circuit may malfunction, causing the outputs to stop operating.

To prevent this kind of malfunction, reduce the wiring impedance between the C_{DLY} (No. 41) pin and the AGND (No. 18 and 42) pins, and take measures so that noise is not superimposed on the C_{DLY} (No. 41) pin.

Note that if the soft-start time is longer than the short-circuit protection circuit may operate before the output of the channel rises. Therefore, be sure to determine the short-circuit protection circuit delay time on the actual device.

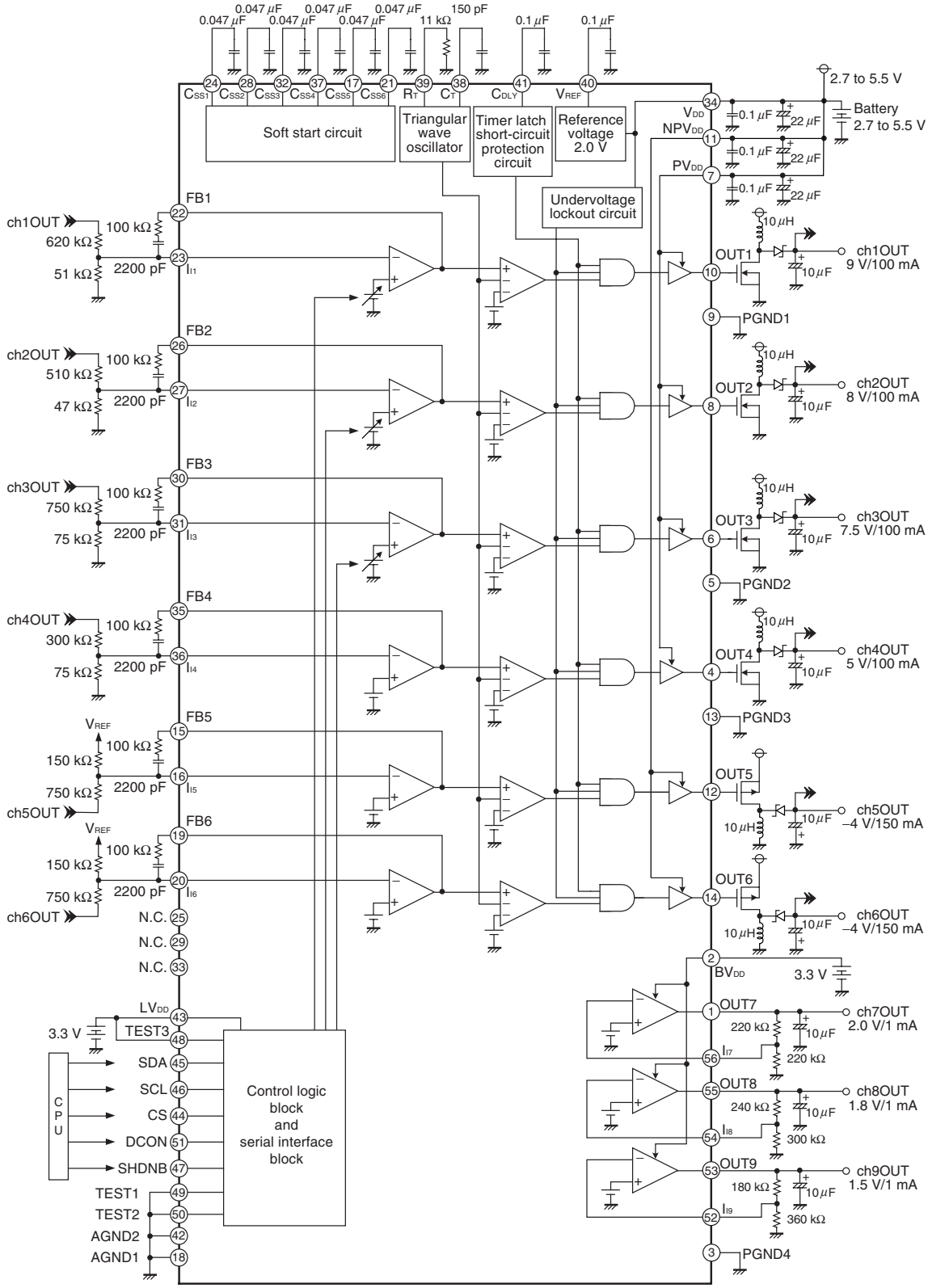
11.8 Notes on Actual Pattern Wiring

When actually wiring the pattern, separate the ground of the control lines from the ground of the power lines, so that there is as little common impedance by using a bypass capacitor (etc.), so that noise is not superimposed on the V_{DD} (No. 34) pin or the V_{REF} (No. 40) pin.

11.9 Notes on Pin Connections

If there is more than one pin of any pin type, ensure that all the pins are connected. Also, always apply the same potential to the power supply pins V_{DD} (No. 34) pin, PV_{DD} (No. 7) pin, and NPV_{DD} (No. 11) pin.

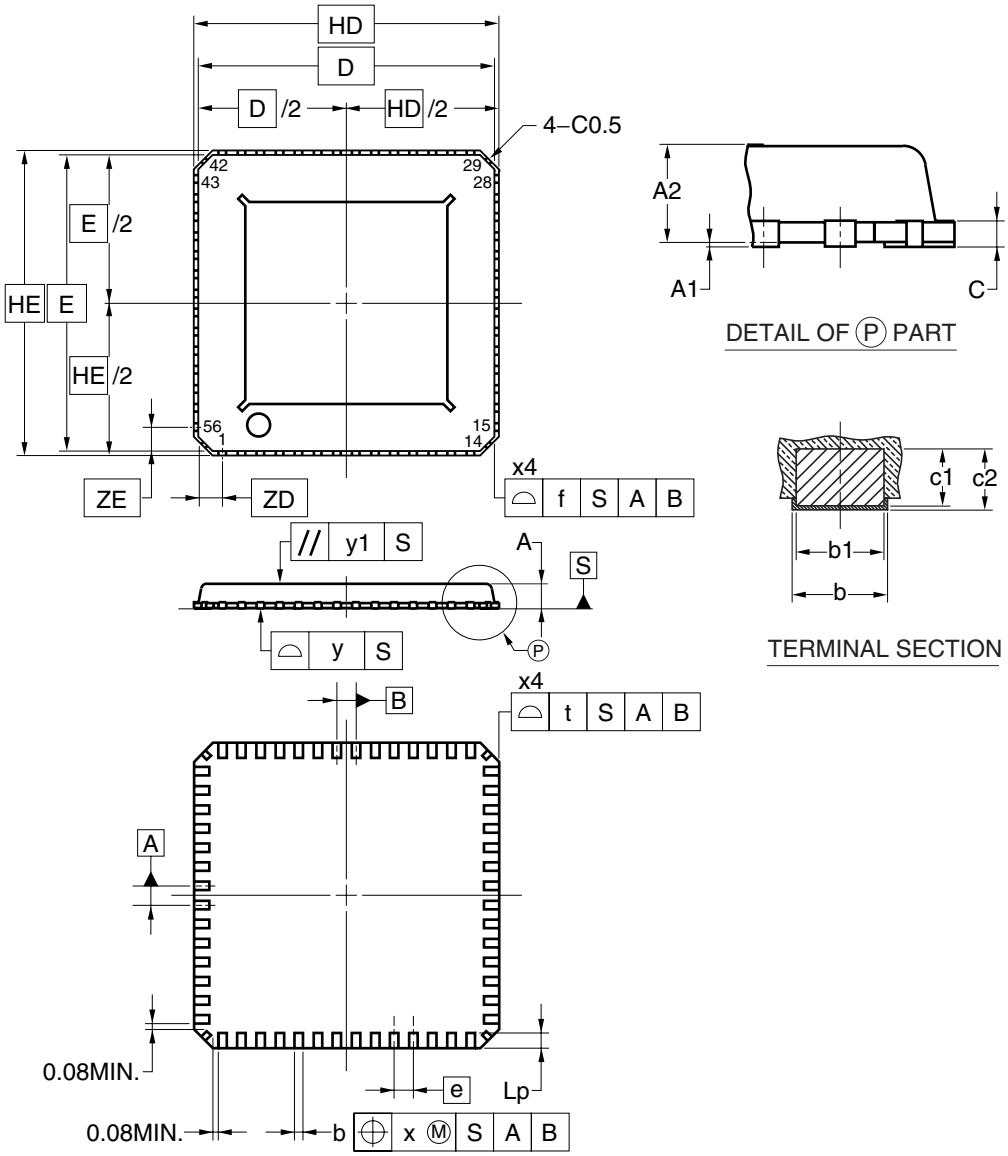
12. EXAMPLE OF APPLICATION CIRCUIT



Caution The constants shown in this figure are for reference only and do not guarantee the characteristics. Set the constants and use appropriate components in accordance with the actual operating conditions.

13. PACKAGE DRAWING

56-PIN PLASTIC WQFN (8x8)



(UNIT:mm)

ITEM	DIMENSIONS
D	7.75
E	7.75
f	0.20
HD	8.00
HE	8.00
t	0.20
A	$0.67^{+0.08}_{-0.04}$
A1	$0.03^{+0.02}_{-0.025}$
A2	0.64
b	0.23±0.05
b1	0.20±0.03
c	0.17
c1	0.14–0.16
c2	0.14–0.20
e	0.50
Lp	0.40±0.10
x	0.05
y	0.08
y1	0.10
ZD	0.625
ZE	0.625

P56K9-50-9B4

NOTES

※1 "t" AND "f" EXCLUDES MOLD FLASH

※2 ALTHOUGH THERE ARE 4 TERMINALS IN THE CORNER PART OF A PACKAGE, THESE TERMINALS ARE NOT DESIGNED FOR INTERCONNECTION, BUT FOR MANUFACTURING PROCESS OF THE PACKAGE, THEREFOR DO NOT INTEND TO SOLDER THESE 4 TERMINALS, SOLDERABLITY OF THE 4 TERMINALS ARE NOT GUARANTEED.

★ 14. RECOMMENDED SOLDERING CONDITIONS

The μPD168103 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Type of Surface Mount Device

μPD16908K9-9B4-A: 56-pin plastic WQFN (8 x 8)

Process	Conditions	Symbol
Infrared reflow	Package peak temperature: 260°C, Time: 60 seconds MAX. (at 220°C or higher), Count: Three times or less, Exposure limit: 3 days Note (after that, prebake at 125°C for 10 hours), Flux: Rosin flux with low chlorine (0.2 Wt% or below) recommended. <Precaution> Products other than in heat-resistant trays (such as those packaged in a magazine, taping, or non-thermal-resistant tray) cannot be baked in their package.	IR60-103-3

Note After opening the dry pack, store it a 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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