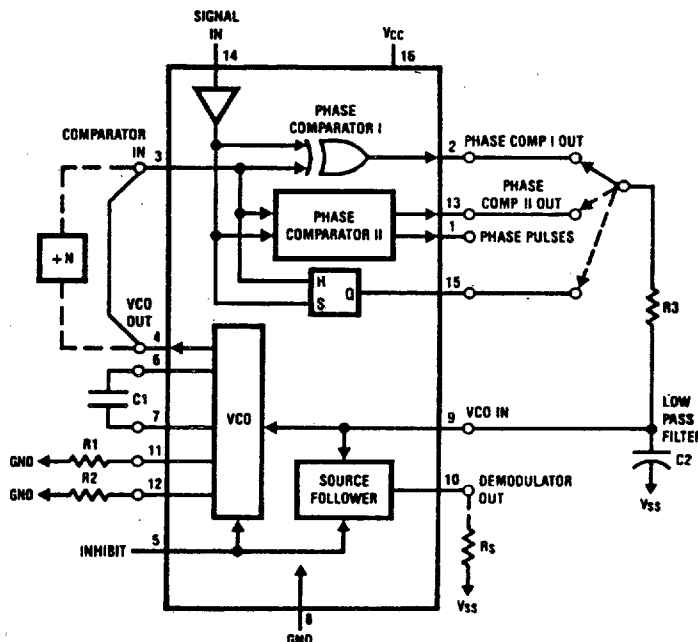


CMOS Phase Lock Loop - Radiation Hardened 54HC4046RP

For Space Applications

SET's 54HC4046RP (RP for RAD-PAK®) high speed Phase Lock Loop microcircuit features a 100 kilorad (Si) total dose tolerance. Fully equivalent to the commercial MM54HC4046, the 54HC4046RP combines National Semiconductor's MM54HC4046 low power phase lock loop and SET's radiation hardened RAD-PAK® packaging. This device uses 3.5u silicon-gate P-well microCMOS Technology to obtain high frequency operation both in the phase comparator and VCO sections. This device contains a low power linear voltage controlled oscillator (VCO), a source follower, and three phase comparators. The three phase comparators have a common signal input and a common comparator input. The signal input has a self biasing amplifier allowing signals to be either capacitively coupled to the phase comparators with a small signal or directly coupled with standard input logic levels. Capable of surviving space environments, the 54HC4046RP is ideal for many satellite, spacecraft, and space probe missions. The radiation hardened RAD-PAK® technology incorporates radiation shielding in the microcircuit package. The 54HC4046RP is available in Class S packaging and screening.

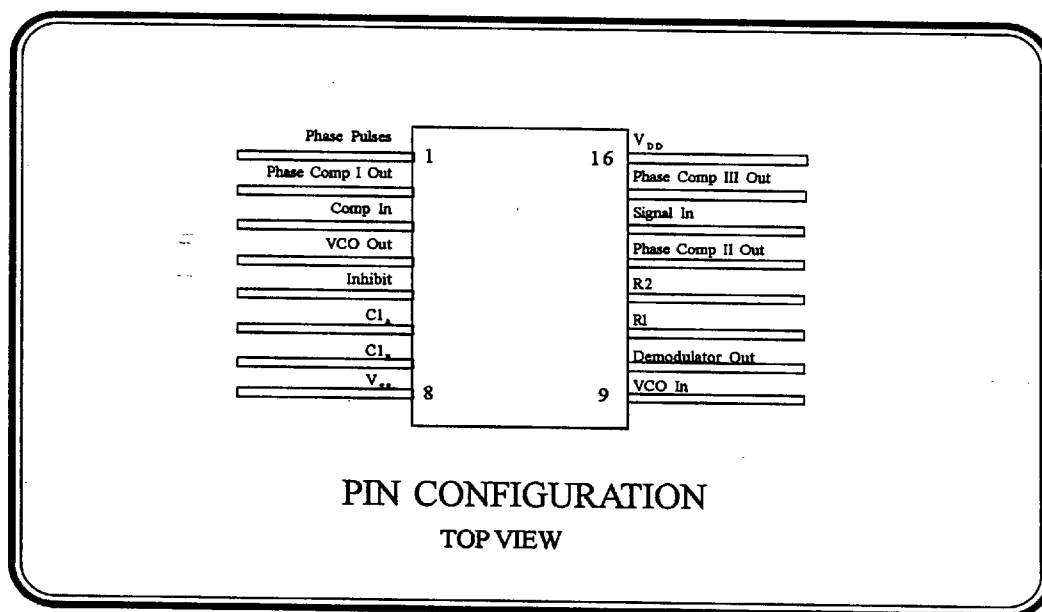


**SPACE
ELECTRONICS
INCORPORATED**

Tel: (619) 452-4167 Fax: (619) 452-5499

Radiation Hardened 54HC4046RP

CMOS
Phase Lock Loop



Features

- ▲ Low Power PLL
- ▲ Pin Compatible with National Semiconductor MM54HC4046
- ▲ RAD-PAK® Radiation Hardened Against Natural Space Radiation
- ▲ Total Dose Hardness >100 krad (Si)
- ▲ Package:
 - 16 Pin RAD-PAK® DIP (640 mils x 420 mils)
 - Weight - 2.0 grams
- ▲ Fast Conversion Times
- ▲ Low Dynamic Power Consumption
 - $V_{CC} = 4.5V$
- ▲ Maximum VCO Operating Frequency
 - 20 MHz ($V_{CC} = 4.5V$)
- ▲ Fast Comparator Response Time ($V_{CC} = 4.5V$)
 - Comparator I: 20 ns
 - Comparator II: 25 ns
 - Comparator III: 20 ns
- ▲ Screening per TM 5004
- ▲ QCI per TM5005

Specifications and design are subject to change without notice.



August 1995

For Further Information Contact:

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54HC4046RP ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{CC}	-0.5	+7.0	V
DC Input Voltage	V_{IN}	-0.5	$V_{CC}+0.5$	V
DC Output Voltage	V_{OUT}	-0.5	$V_{CC}+0.5$	V
Clamp Diode Current	I_{IK}, I_{OK}		+20	mA
DC V_{CC} or GND Current, per pin	I_{CC}		+50	mA
Storage Temperature Range	T_{STG}	-65	+150	°C
Power Dissipation	P_D		500	mW
Lead Temperature (Soldering, 10 seconds)	T_L		+300	°C

54HC4046RP OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	V_{CC}	+2.0	+6.0	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	V_{CC}	V
Operating Temperature Range	T_A	-55	+125	°C
Input Rise or Fall Times $V_{CC}=2.0V$ $V_{CC}=4.5V$ $V_{CC}=6.0V$	t_r, t_f	0 0 0	1000 500 400	ns



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54HC4046RP DC ELECTRICAL CHARACTERISTICS¹

PARAMETER	SYMBOL	MIN	MAX	UNIT
Minimum High Level Input Voltage @ $V_{CC}=3.0V$	V_{IH}	2.1		V
Maximum Low Level Input Voltage @ $V_{CC}=3.0V$	V_{IL}		0.9	V
Minimum High Level Output Voltage $V_{IH}=V_{IH}$ or V_{IL} $I_{OUT} \leq 20\mu A$ @ $V_{CC}=3.0V$ $V_{CC}=4.5V$ $V_{CC}=6.0V$ $V_{IH}=V_{IH}$ or V_{IL} $I_{OUT} \leq 4.0mA$ @ $V_{CC}=4.5V$ $I_{OUT} \leq 5.2mA$ @ $V_{CC}=6.0V$	V_{OH}	2.9 4.4 5.9 3.98 5.48		V
Maximum Low Level Output Voltage $V_{IH}=V_{IH}$ or V_{IL} $I_{OUT} \leq 20\mu A$ @ $V_{CC}=3.0V$ $V_{CC}=4.5V$ $V_{CC}=6.0V$ $V_{IH}=V_{IH}$ or V_{IL} $I_{OUT} \leq 4.0mA$ @ $V_{CC}=4.5V$ $I_{OUT} \leq 5.2mA$ @ $V_{CC}=6.0V$	V_{OL}		0.1 0.1 0.1 0.4 0.4	V
Input Leakage Current $V_{IN}=V_{CC}$ or GND @ $V_{CC}=6.0V$	I_{INH} I_{INL}	-1.0	+1.0	μA
R1 and R2 Range $V_{CC}=4.5V$	R_{RING}	0	No Max	kOhm
VCO _{IN} Operating Voltage Range $V_{CC}=3.0V$ $V_{CC}=4.5V$ $V_{CC}=6.0V$	V_{OP}	0.9 0.9 0.9	1.9 3.2 4.6	μA
Maximum Frequency C1=50pF, R1=3.5kOhms, R2=infinity, $V_{CC}=4.5V$ C1=0pF, R1=9.1kOhms, R2=infinity, $V_{CC}=4.5V$	I_{CC}	24 38		MHz

Note:

1. For a power supply of $5V \pm 10\%$ the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC}=5.5V$ and 4.5V respectively. The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.



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54HC4046RP AC ELECTRICAL CHARACTERISTICS²

PARAMETER	SYMBOL	MIN	MAX	UNIT
PHASE COMPARATOR				
Maximum Output Rise and Fall Time $V_{CC}=2.0V$ $V_{CC}=3.0V$ $V_{CC}=6.0V$	t_r, t_f		110 22 19	ns
C1 Capacitance Range @ $V_{CC}=4.5V$	C_{IN}	0.0	No Max	pF
Output Transition Time ³ @ $C_L=50$ pF $V_{CC}=2.0V$ $V_{CC}=4.5V$ $V_{CC}=6.0V$	t_{PHL}, t_{PLH}		75 15 13	ns
Output Enable Time ³ @ $C_L=50$ pF $V_{CC}=2.0V$ $V_{CC}=4.5V$ $V_{CC}=6.0V$	t_{PDH}, t_{PLZ}		265 80 68	ns
Output Disable Time ³ $V_{CC}=2.0V$ $V_{CC}=4.5V$ $V_{CC}=6.0V$	t_{PDZ}, t_{PLZ}		315 95 74	ns
PHASE COMPARATOR I				
Maximum Propagation Delay ³ $V_{CC}=2.0V$ $V_{CC}=4.5V$ $V_{CC}=6.0V$	t_{PHL}, t_{PLH}		200 40 34	ns
PHASE COMPARATOR II				
Maximum Propagation Delay ³ $V_{CC}=2.0V$ $V_{CC}=4.5V$ $V_{CC}=6.0V$	t_{PLH2}, t_{PHL2}		300 60 70	ns
PHASE COMPARATOR III				
Maximum Propagation Delay ³ $V_{CC}=2.0V$ $V_{CC}=4.5V$ $V_{CC}=6.0V$	t_{PHL3}, t_{PLH3}		245 49 42	ns

Note:

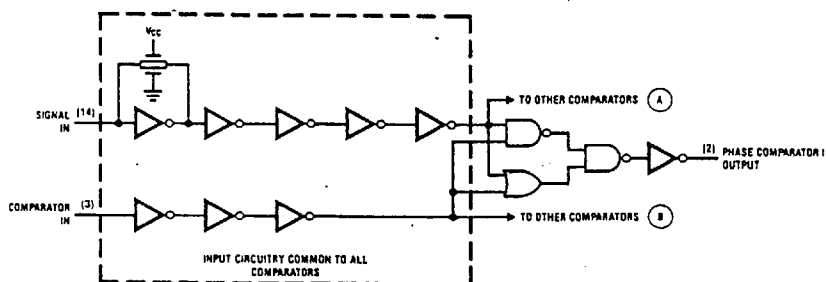
2. $V_{CC}=2.0$ to $6.0V$, $C_L=50pF$, $t_r=t_f=6ns$ (unless otherwise specified.)
 3. $T_A=25^\circ C$.

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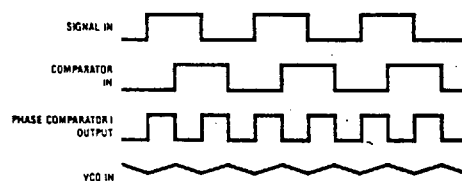
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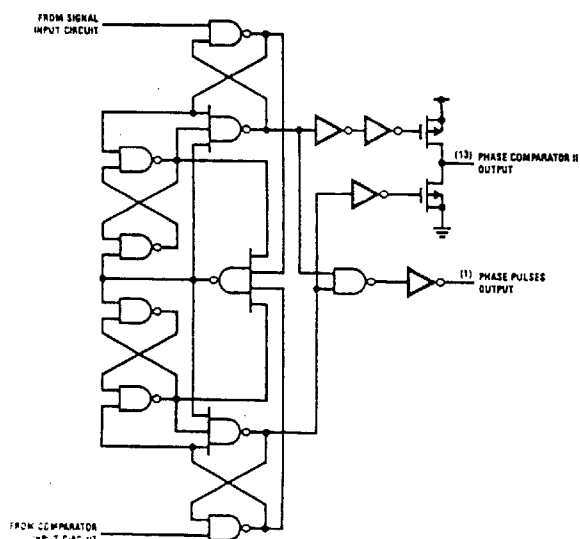
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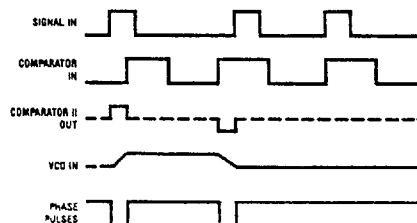
Logic Diagram for Phase Comparator I and the Common Input Circuit for All Three Comparators



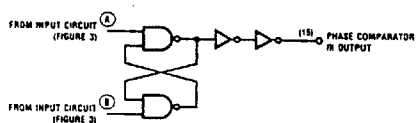
Typical Phase Comparator I Waveforms



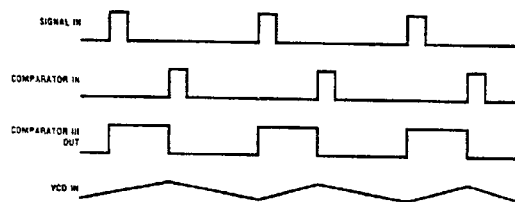
Logic Diagram for Phase Comparator II



Typical Phase Comparator II Output Waveforms



Phase Comparator III Logic Diagram



Typical Waveforms for Phase Comparator III



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54HC4046RP AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	MAX	UNIT
DEMODULATOR OUTPUT				
Output Voltage Versus Input Frequency @ $V_{CC}=4.5V$ R1=100kOhms R2=infinity C1=100pF RS=10kOhms R3=100kOhms C2=100pF	V_{OUT}/f_{IN}		330	mV/KHz
Offset Voltage (V_{CO_IN} to V_{DEM}) $V_{CC}=3.0V$ $V_{CC}=4.5V$ $V_{CC}=6.0V$	V_{OFF}		+30.0 +20.0 +10.0	mV
Output Resistance @ DEM_{OUT} ($V_{DEM(OUT)}=V_{CC}$) $V_{CC}=3.0V$ $V_{CC}=4.5V$ $V_{CC}=6.0V$	R_O		25 0.1 0.1	Ohms

54HC4046RP Package Ordering Guide

Package Style	Case Outline 1/	Description
D	D-16	16 Pin Dual In Line Package
F	F-16	16 Pin Flat Package

Note:

1/ For outline information, see Appendix A (Package Information - Outline Dimension)

54HC4046RP PINOUT

PIN	SIGNAL	DESCRIPTION
1	Phase Pulses	Phase Comparator Pulse Output
2	Phase Comp 1 Out	Phase Comparator 1 Output
3	Comp In	Comparator Input
4	VCO Out	VCO Output
5	Inhibit	Inhibit Input
6	C1a	Capacitor C1 Connection A
7	C1b	Capacitor C1 Connection B
8	Vss	Ground
9	VCOin	VCO Input
10	Demodulator Out	Demodulator Output
11	R1	Resistor R1 Connection
12	R2	Resistor R2 Connection
13	Phase Comp II Out	Phase Comparator 2 Output
14	Signal In	Signal Input
15	Phase Comp III Out	Phase Comparator 3 Output
16	Vdd	Positive Supply Voltage



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