PowerMOS transistor BUK482-100A

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope suitable for surface mount applications.
The device is intended for use in automotive and general purpose switching applications.

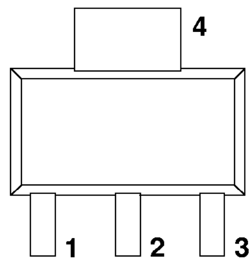
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (DC)	1.8	A
P_{tot}	Total power dissipation	1.8	W
T_j	Junction temperature	150	˚C
$R_{DS(ON)}$	Drain-source on-state resistance; V_{GS} = 10 V	0.28	Ω

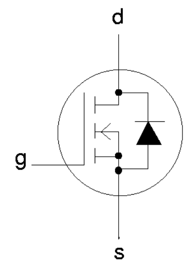
PINNING - SOT223

PIN	DESCRIPTION
1	gate
2	drain
3	source
4	drain (tab)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	100	V
$\pm V_{GS}$	Gate-source voltage	-	-	30	V
I_D	Drain current (DC)	T_{amb} = 25 ˚C	-	1.8	A
I_D	Drain current (DC)	T_{amb} = 100 ˚C	-	1.1	A
I_{DM}	Drain current (pulse peak value)	T_{amb} = 25 ˚C	-	7.2	A
P_{tot}	Total power dissipation	T_{amb} = 25 ˚C	-	1.8	W
T_{stg}	Storage temperature	-	- 55	150	˚C
T_j	Junction Temperature	-	-	150	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-b}$	From junction to board[1]	Mounted on any PCB	-	40	-	K/W
$R_{th\ j-amb}$	From junction to ambient	Mounted on PCB of Fig.17	-	-	70	K/W

1 Temperature measured 1-3 mm from tab.

STATIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA	100	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.1	3.0	4.0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V;	-	1	10	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 ˚C	-	0.1	1.0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±30 V; V_{DS} = 0 V	-	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1.8 A	-	0.21	0.28	Ω

DYNAMIC CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1.8 A	1.5	2.5	-	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	300	500	pF
C_{oss}	Output capacitance		-	90	120	pF
C_{rss}	Feedback capacitance		-	35	50	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A;	-	9	14	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_{GS} = 50 Ω;	-	25	40	ns
$t_{d\ off}$	Turn-off delay time	R_{gen} = 50 Ω	-	30	45	ns
t_f	Turn-off fall time		-	20	40	ns

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25 ˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	1.8	A
I_{DRM}	Pulsed reverse drain current	-	-	-	7.2	A
V_{SD}	Diode forward voltage	I_F = 1.8 A; V_{GS} = 0 V	-	0.85	1.1	V
t_{rr}	Reverse recovery time	I_F = 1.8 A; -dI_F/dt = 100 A/µs;	-	80	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 30 V	-	0.30	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 1.8 A; V_{DD} ≤ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{amb} = 25 ˚C	-	-	40	mJ

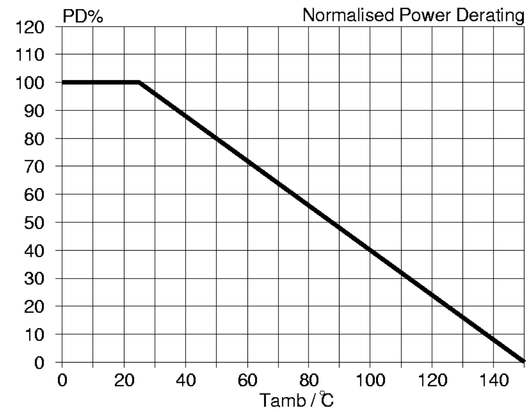


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D/P_{D\ 25\ ^\circ C} = f(T_{amb})$

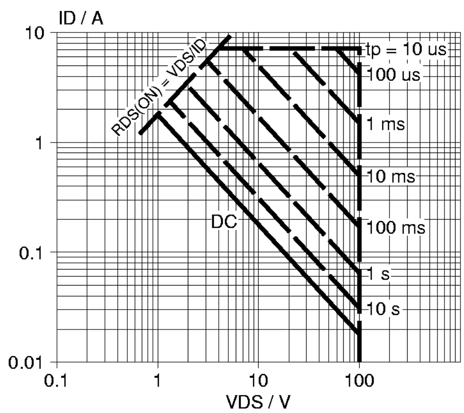


Fig.4. Safe operating area. $T_{amb} = 25\ ^\circ C$.
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

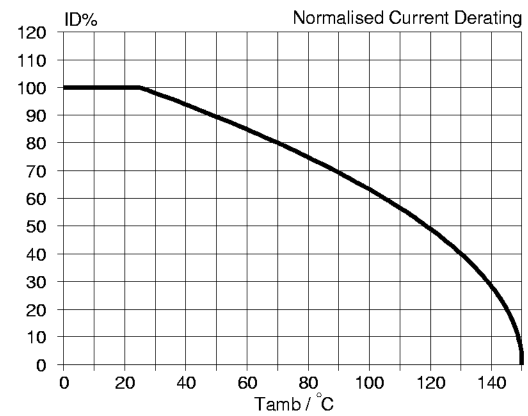


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D/I_{D\ 25\ ^\circ C} = f(T_{amb})$; conditions: $V_{GS} \geq 10$ V

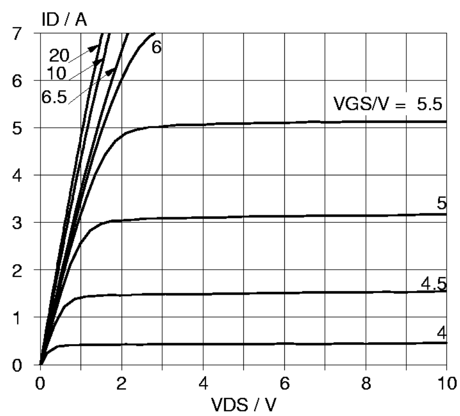


Fig.5. Typical output characteristics, $T_j = 25\ ^\circ C$.
$I_D = f(V_{DS})$; parameter V_{GS}

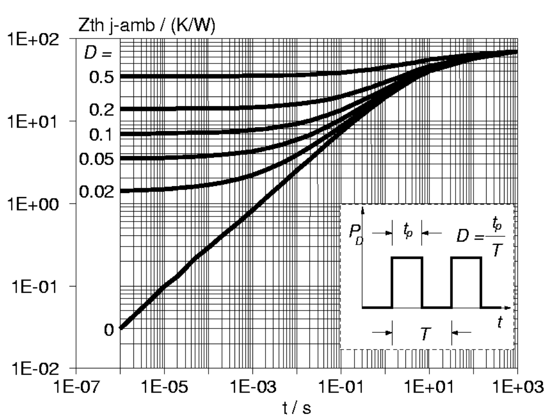


Fig.3. Transient thermal impedance.
$Z_{th\ j\text{-}amb} = f(t)$; parameter $D = t_p/T$

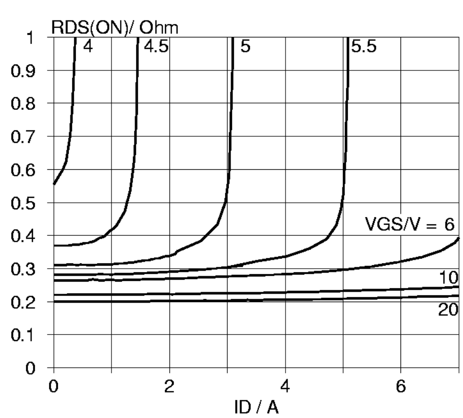


Fig.6. Typical on-state resistance, $T_j = 25\ ^\circ C$.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

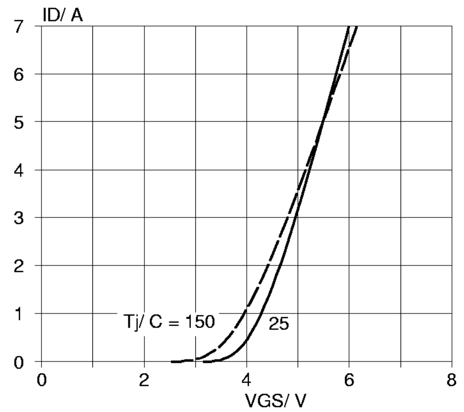


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; conditions: V_{DS} = 25 V; parameter T_j

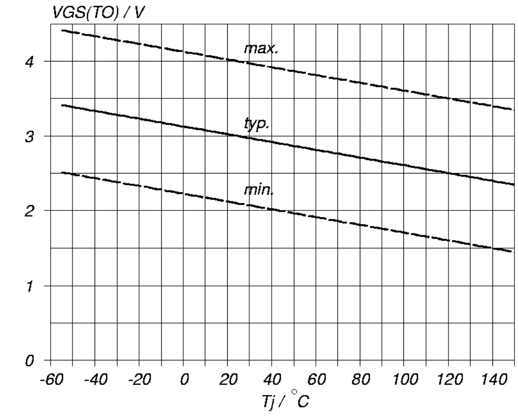


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

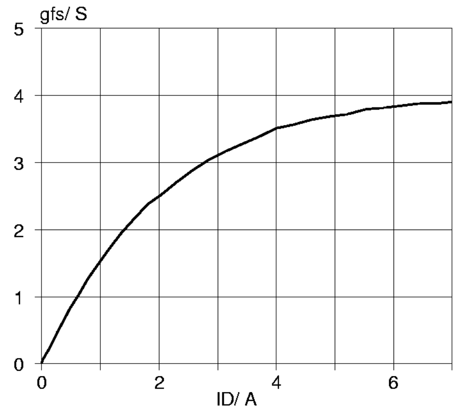


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$; conditions: V_{DS} = 25 V

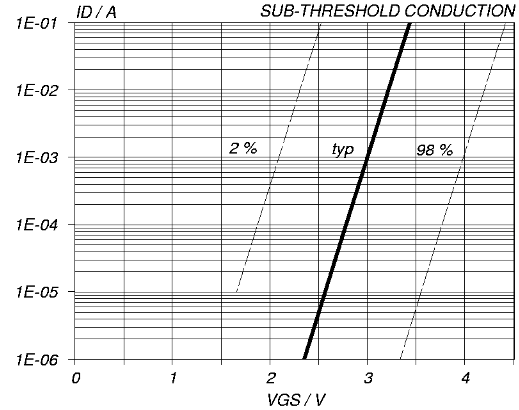


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: T_j = 25 ˚C; $V_{DS} = V_{GS}$

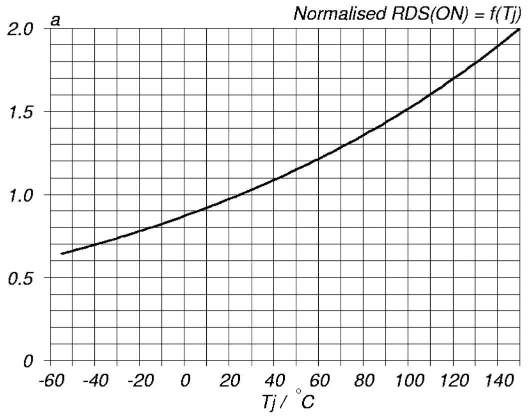


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\,^{\circ}C} = f(T_j)$; I_D = 1.8 A; V_{GS} = 10 V

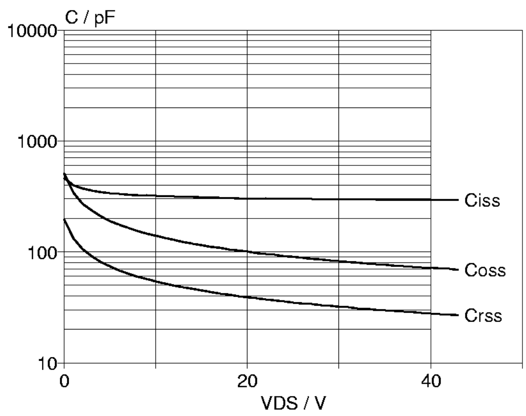


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: V_{GS} = 0 V; f = 1 MHz

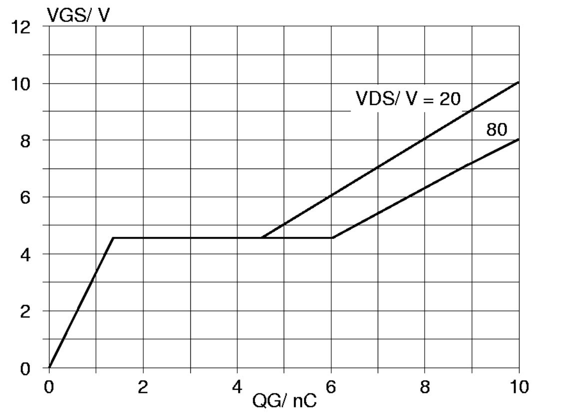


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; conditions: I_D = 1.8 A; parameter V_{DS}

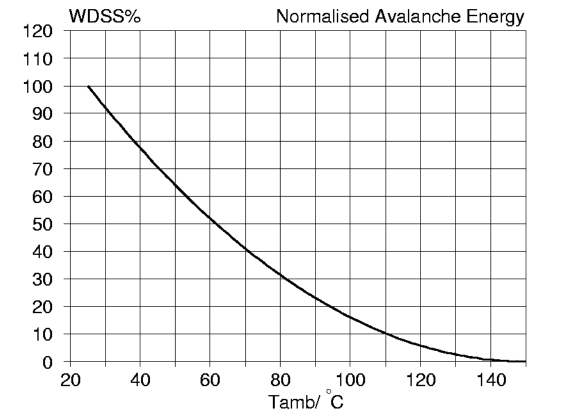


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{amb})$; conditions: I_D = 1.8 A

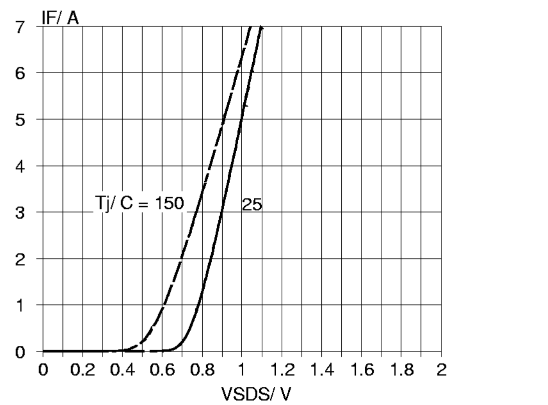


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; conditions: V_{GS} = 0 V; parameter T_j

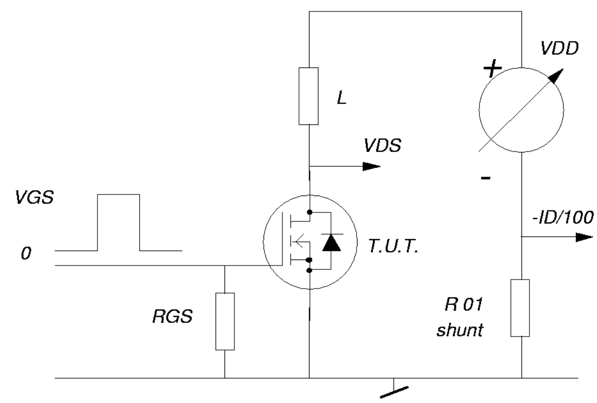


Fig.16. Avalanche energy test circuit.

$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

PRINTED CIRCUIT BOARD

Dimensions in mm.

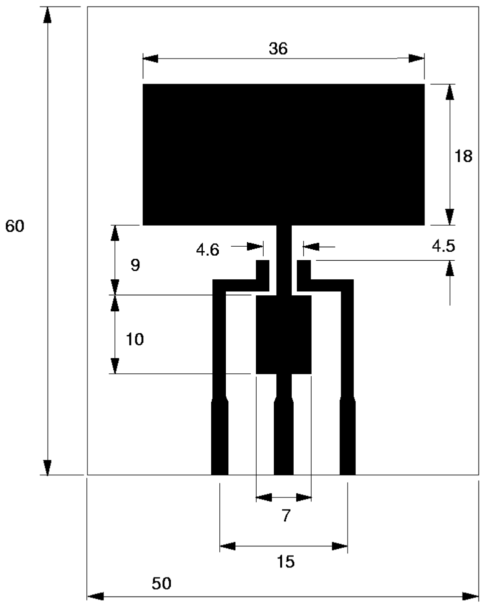


Fig.17. PCB for thermal resistance and power rating for SOT223.
PCB: FR4 epoxy glass (1.6 mm thick), copper laminate (35 µm thick).

MECHANICAL DATA

Dimensions in mm

Net Mass: 0.11 g

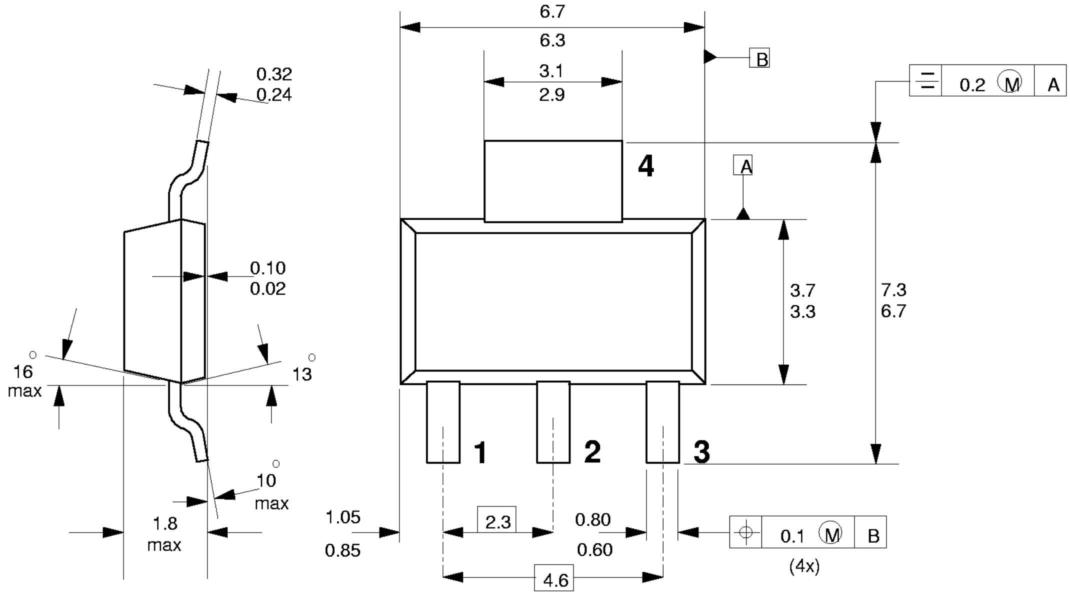


Fig.18. SOT223 surface mounting package.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to surface mounting instructions for SOT223 envelope.
3. Epoxy meets UL94 V0 at 1/8".