

Cordless Telephone Modem IC

Description

CXD1233BM/BQ developed for cordless telephones, provides a modem when used in conjunction with microcomputer and filter.

Features

- Uses the low error rate manchester code, decoder and encoder.
- Built-in comparator for received manchester data.
- Compatible with 4 types of data transfer speeds.
- Wide supply voltage range
- Low power consumption

Application

Cordless telephone
(Low power, Digital direct modulation type)

Structure

Silicon monolithic IC

Absolute Maximum Ratings (Ta = 25°C, Vss = 0V)

• Supply voltage	VDD	VSS-0.5 to +7.0	V
• Input voltage	VI	VSS-0.5 to VDD + 0.5	V
• Output voltage	VO	VSS-0.5 to VDD + 0.5	V
• Operating temperature	Topr	-20 to +75	°C
• Storage temperature	Tstg	-55 to +150	°C

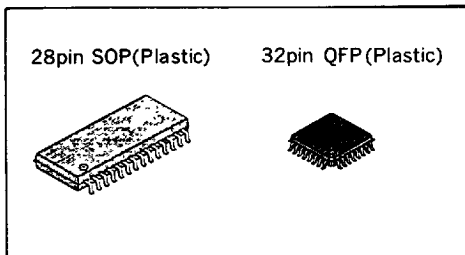
Recommended Operating Condition

• Supply voltage	VDD	3.0 to 5.0 (Typ. 3.6)	V
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Electrical Characteristics

VDD = 3.0 to 5.0V, VSS = 0V, Topr = -20 to +75°C

Item		Symbol	Min.	Typ.	Max.	Unit
Supply current (Output pin at no load)		IDD		1		mA
Input voltage		VIHC	0.7VDD			V
		VILC			0.3VDD	
Output voltage	IOH = -1mA	VOHI	VDD-0.5			V
	IOL = 2mA	VOLI			0.4	V
Input leak current		ILI	-10		10	μA
Output leak current		ILZ	-40		40	μA



Oscillation Cell Electrical Characteristics

VDD = 3.0 to 5.0V, VSS = 0V, Topr = -20 to +75°C

Item		Symbol	Min.	Typ.	Max.	Unit
Logic threshold value		LVth		VDD/2		V
Input voltage		VIH	0.7VDD			V
		VIL			0.3VDD	V
Feedback resistance	VIN = VSS, or VDD	RFB	500K	2.6M	8M	Ω
Output voltage	IOH -0.5mA	VOH	VDD/2			V
	IOL 0.5mA	VOL			VDD/2	V

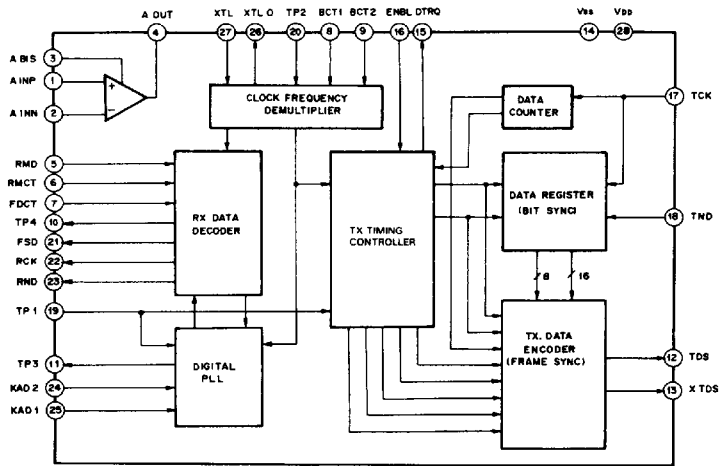
I/O Capacitance

Item		Symbol	Min.	Typ.	Max.	Unit
Input pin		CIN			9	pF
Output pin		COU			11	pF

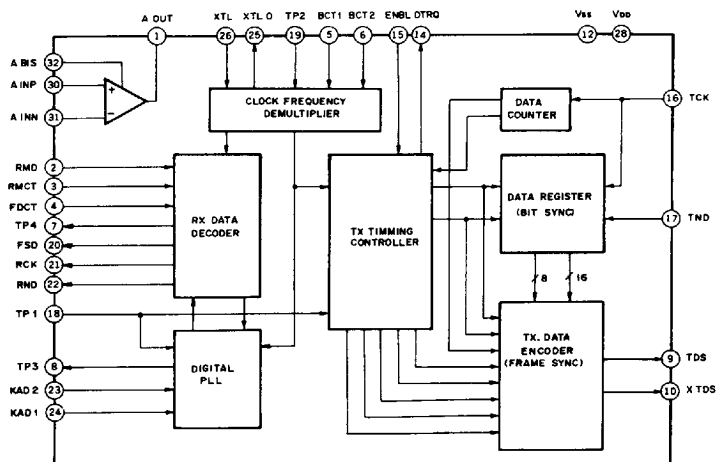
Test conditions: VDD = VI = 0V, f = 1 MHz

Block Diagram

CXD1233BM



CXD1233BQ



Pin Description

CXD1233BM

No.	Symbol	I/O	Description
1	AINP	I	Comparator non-inverted input for received manchester data.
2	AINN	I	Comparator inverted input for received manchester data.
3	ABIS	I	Comparator bias setting input for received manchester data.
4	AOUT	O	Comparator output for received manchester data.
5	RMD	I	Received manchester data input.
6	RMCT	I	Pin for the selection of inverted RMD (Normally fixed at 'L' at 'H' Data inverted)
7	FDCT	I	Pin for the selection of frame sync pattern ('L' for Hand set, 'H' for Base set)
8	BCT1	I	Data bit rate selection (BCT 1, BCT 2) Normally (H,H): Compatible with 1200bps (L,L): Compatible with 600bps (L,H): Compatible with 4800bps (H,L): Compatible with 2400bps
9	BCT2	I	
10	TP4	O	Output for test
11	TP3	O	Output for test
12	TDS	O	Transmitted manchester data output
13	XTDS	O	Inverted TDS (Pin 12)
14	Vss	—	GND pin
15	DTRQ	O	Data request output for transmission.
16	ENBL	I	Enable input (ENABLE at 'L')
17	TCK	I	Clock input synchronous with TND (pin 18)
18	TND	I	NRZ data input for transmission.
19	TP1	I	Test input (normally fixed at 'L')
20	TP2	I	Test input (normally fixed at 'L')
21	FSD	O	Frame sync detection output.
22	RCK	O	Clock output extracted from transmitted data.
23	RND	O	Transmitted NRZ data output.
24	KAD2	I	PLL logic range select input for transmitted manchester data.
25	KAD1	I	
26	XTLO	O	Crystal oscillator output (4.608MHz)
27	XTL	I	Crystal oscillator input or external clock input (4.608MH)
28	VDD	—	Supply pin

CXD1233BQ

No.	Symbol	I/O	Description
1	AOUT	O	Comparator output for received manchester data.
2	RMD	I	Received manchester data input.
3	RMCT	I	Pin for the nelection of inverted RMD (Normally fixed at 'L' at 'H' Data inverted)
4	FDCT	I	Pin for the selection of frame sync pattern ('L' for Hand set, 'H' for Base set)
5	BCT1	I	Data bit rate selection (BCT1, BCT2) Normally(H, H): Compatible with 1200bps (L, L): Compatible with 600bps (L, H): Compatible with 4800bps (H, L): Compatible with 2400bps
6	BCT2	I	
7	TP4	O	Output for test
8	TP3	O	Output for test
9	TDS	O	Transmitted manchester data output
10	XTDS	O	Inverted TDS (Pin 9)
11	N.C	—	
12	V _{SS}	—	GND pin
13	N.C	—	
14	DTRQ	O	Data request output for transmission.
15	ENBL	I	Enable input (ENABLE at 'L')
16	TCK	I	Clock input synchronous with TND (Pin 17)
17	TND	I	NRZ data input for transmission.
18	TP1	I	Test input (normally fixed at 'L')
19	TP2	I	Test input (normally fixed at 'L')
20	FSD	O	Frame sync detection output.
21	RCK	O	Clock output extracted from transmitted data.
22	RND	O	Transmitted MRZ data output.
23	KAD2	I	PLL logic range select input for transmitted manchester data.
24	KAD1	I	
25	XTLO	O	Crystal oscillator output (4.608MHz)
26	XTL	I	Crystal oscillator input or external clock input (4.608MH)
27	N.C	—	
28	V _{DD}	—	Supply pin
29	N.C	—	
30	AINP	I	Comparator non-inverted input for received manchester data.
31	AINN	I	Comparator inverted input for received manchester data.
32	ABIS	I	Comparator bias setting input for received manchester data.

Operation

Transmitted data decode

With the cordless telephone system data exchanges are done between HS (Hand Set) and BS (Base Set).

Data format is as follows:

Bit Sync	Frame Sync	ID + Error Correction Data	Control Data
12 bit or more	16 bit	37 bit (1 bit is twice sync signal 1 bit)	

Bit sync: Signal that indicates the beginning of data '01010101' that is the repetition of '0' and '1' data for 12 bit or more.

Frame sync: 16 bit signal that indicates whether the data is from BS to HS or from HS to BS.

For HS data (BS→HS) FDCT = "L"
1100010011010110

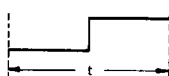
For BS data (HS→BS) FDCT = "H"
1001001100110110

ID + correction compensation data: a 37-bit manchester code.

Control code: The number of bits varies according to the type of equipments. However it should be a figure divisible by 8 when added to 37-bit. Manchester code.

Bit sync and Frame sync are NRZ data. Then the manchester code data where each bit is inverted at its middle and the latter half indicates the logic value. This bit's length is twice that of the bit sync or frame sync. The manchester code logic value "1", "0" is indicated in the Fig. below.

Logic value '1'



Logic value '0'



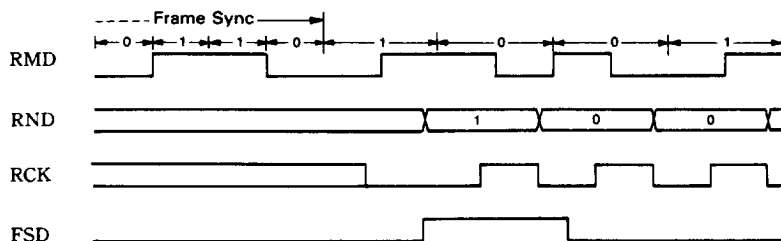
t the time for one bit of the manchester code changes according to the value of BCT 1 and BCT 2. t is compatible with the 4 types of transmission speed of data.

Bit rate

Table 1

BCT1	BCT2	Bit rate	t
0	1	4800BPS	208.3μs
1	0	2400BPS	416.7μs
1	1	1200BPS	833.3μs
0	0	600BPS	1666.7μs

To decode data input through RMD pin, clock components are extracted at D-PLL and using this clock the frame sync signal is detected. Moreover the manchester code logic value is extracted. The frame sync detection signal is output from FSD pin, decoded data is output from RND pin as NRZ. That bit clock is output from RCK pin.



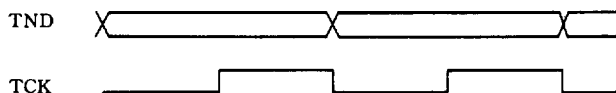
Transmission data encode

Data format in Fig. is assembled through ENBL, TCK and TND that have been sent from μ -COM, and output from TDS and XTDS. The speed of output data matches the bit rate shown in table 1. As ENBL signal is output, the bit sync signal begins to be output from TDS and XTDS. Consequently the frame sync signal depending on FDCT value, is output.

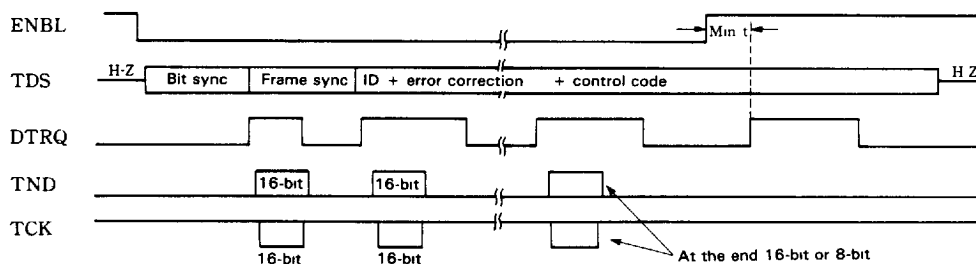
When FDCT = 'L'	'1001001100110110'	} Frame sync signal
When FDCT = 'H'	'1100010011010110'	

Simultaneously as the frame sync begins to be output, 'H' is output from DTRQ pin and requests data to μ -COM.

DTRQ becomes a clock pulse and is output. Then every time DTRQ = H is on, from μ -COM, NRZ data is sent to TND and the clock is sent the required number of times, 16-bit at a time. As data comes in a number of bits multiplied by 8, data transmitted at the end comes in either 16-bit or 8-bit. The timing of TND and TCK is shown in the Fig. below.

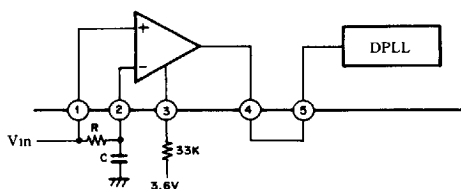


Data input at NRZ is encoded to manchester code and output from TDS and XTDS. As data and clock transmission from μ -COM to TND and TCK ends, ENBL should go back to 'H' before the next DTRQ-'H' turns on, in terms of time t (Table 1). ENBL = 'H' state is on, and as manchester code output ends, TDS and XTDS turn to H-Z (High impedance).



Transmission data timing

Operation of Built-in AMP



The built-in amplifier in CXD1233B serves to interface between the band limitation LPF (f_c : about 3kHz) and the DPLL. It can be used as a comparator to amplify the filter output level (100mVrms) up to logic amplitude. Here as DC to low pass contained in the filter output, is output by means of a primary RC filter to become the comparator comparison voltage, as a result. There is not need to rely on the DC offset of the filter output and drift, since the comparator output duty can be maintained at around a stable 50%.

When $R = 22k\Omega$, and $C = 1\mu F$, the primary RC filter cut off frequency becomes 7Hz ($-3dB$).

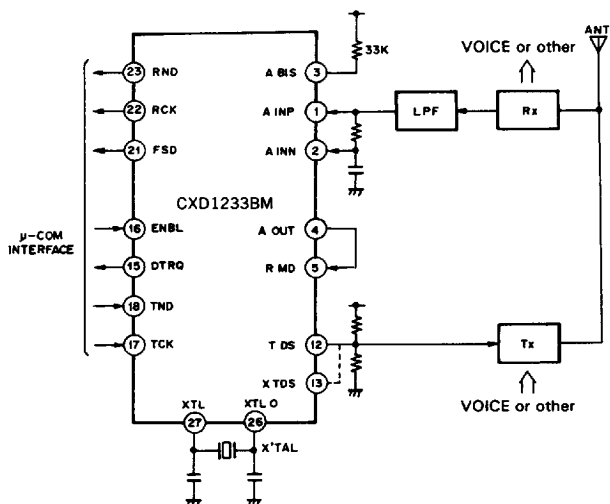
Electrical Characteristics

$T_a = 25^\circ C$, $V_{DD} = 3.6V$

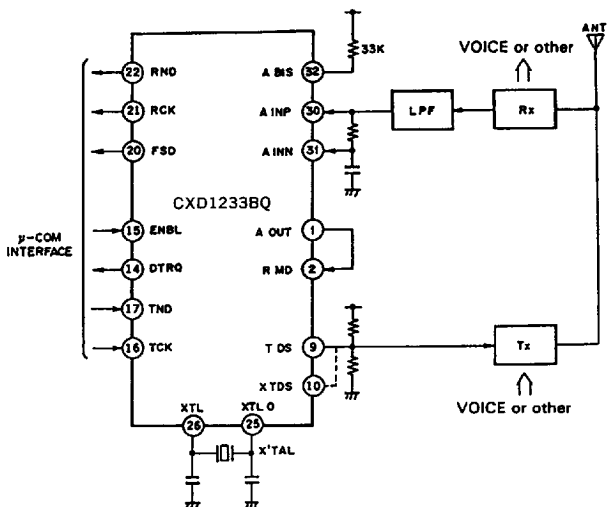
Item	Test conditions	Min.	Typ.	Max.	Unit
Offset voltage	Input conversion			50	mV
Open loop gain	DC gain	20			dB
Input level	$f = 1.2kHz$		100		mV _{rms}

Application Circuit

CXD1233BM

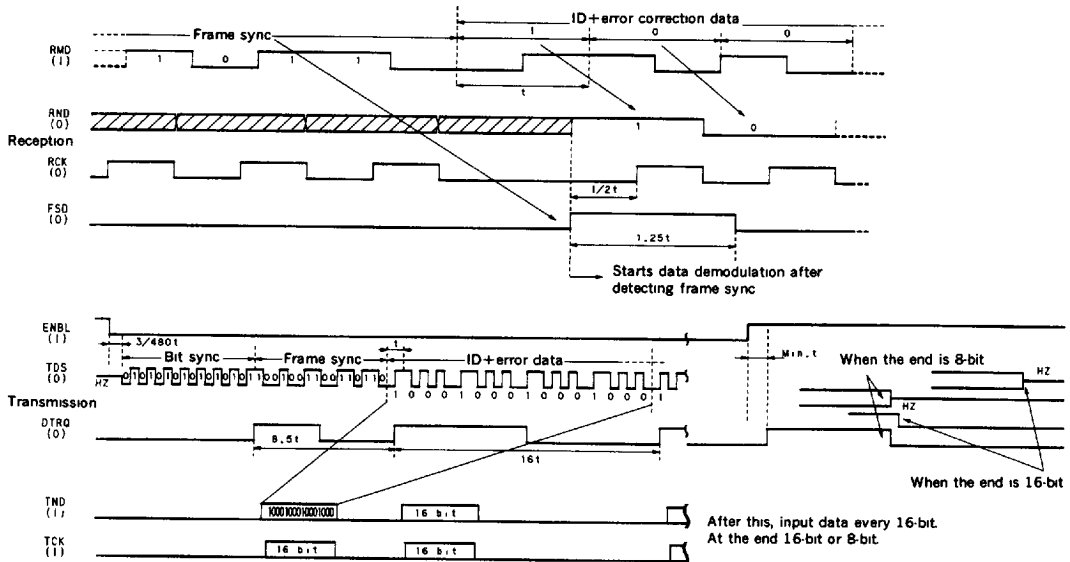


CXD1233BQ



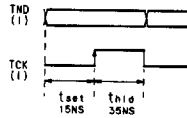
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

CXD1233BM/BQ Reception/Transmission Timing chart



Divide ID+error data into 16-bit and input them from TND as NRZ signal TCK is input clock. Inputs the first 16-bit within 8.5t. From the next 16-bit, input within 16t.

Input starts when DTRQ (data request) is high.

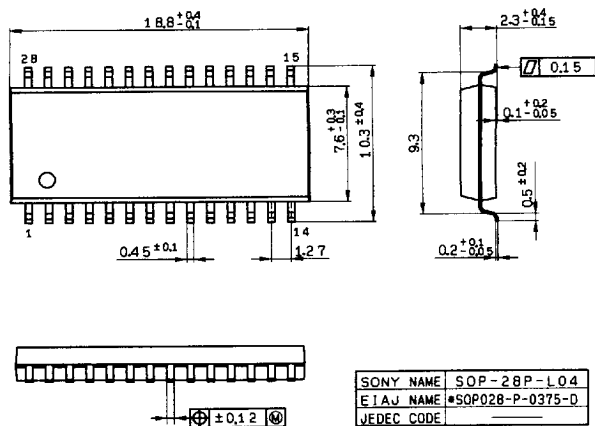


Bit rate	t (us)
4800	208.3
2400	416.7
1200	833.3
600	1666.7

Package Outline Unit: mm

CXD1233BM

28pin SOP (Plastic) 375mil 0.7g



CXD1233BQ

32pin QFP (Plastic) 0.2g

