HM67G1866 Series

65,536-words × 18-bits Synchronous Fast Static RAM Target Spec

HITACHI

ADE-203-579A(Z)
Rev. 3
Dec. 25, 1995

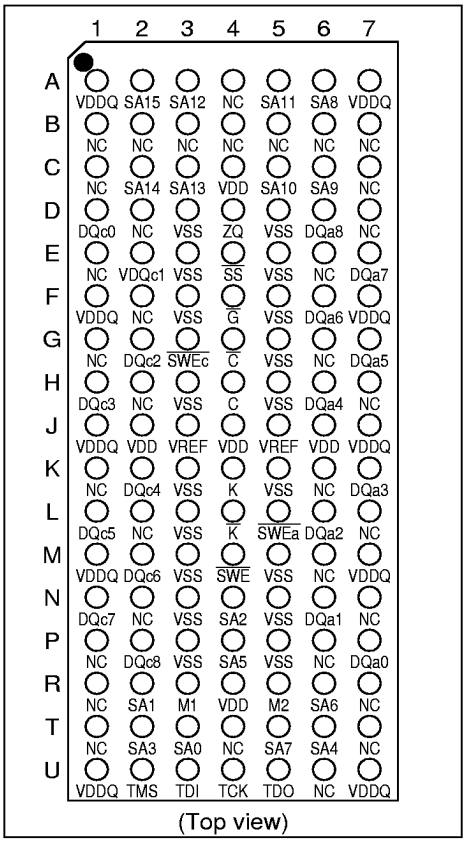
Features

- 3.2 to 3.6 V Operation
- 1.5 V HSTL Compatible Input and Output
- Synchronous Operation
- Internal self-timed Late Write
- Asynchronous/G Output Control
- Byte Write Control
  (2 byte write selects, one for each 9 bits)
- Programmable Impedance Output Drivers
- Differential Clock Inputs
- Boundary Scan

Ordering Information

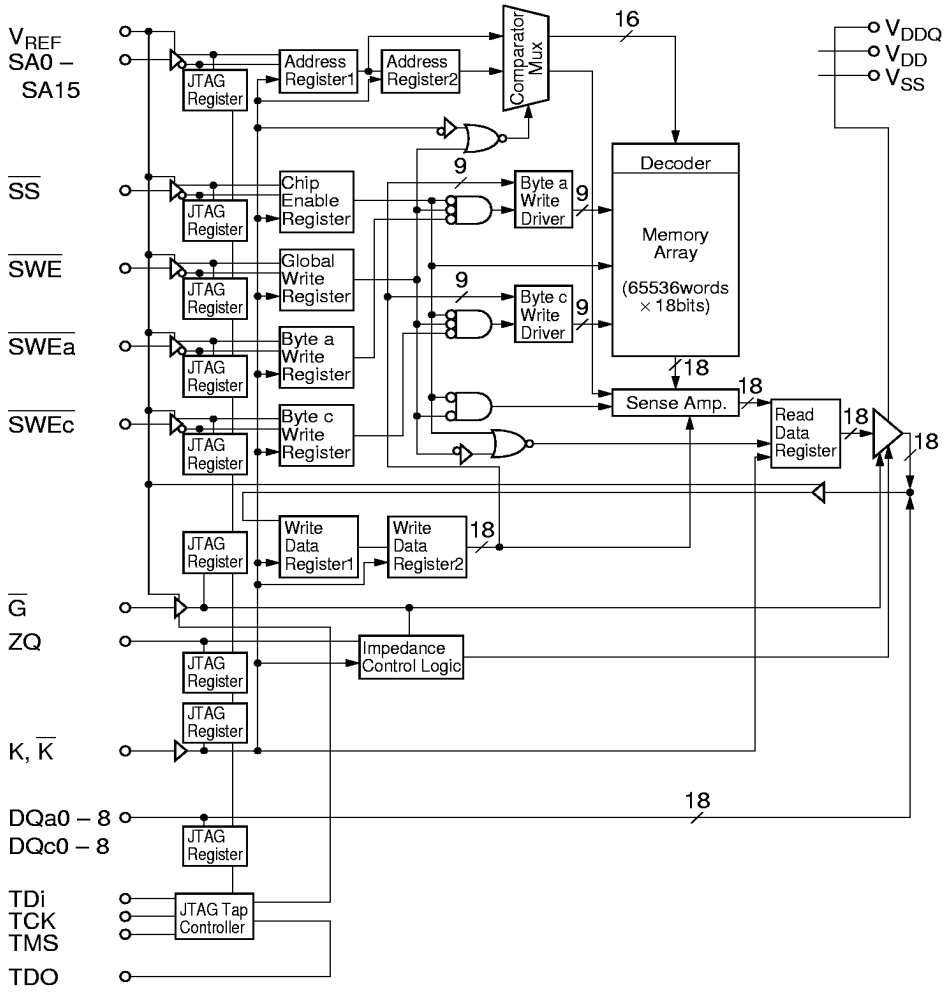
Type Number	Cycle Time	Package
HM67G1866BP-7	7 ns	119 Bump 1.27 mm 14 mm × 22 mm BGA (BP-119)

Pin Arrangement



Pin R3 and R5 are clock mode pins. For this application, Pin R3 and R5 need to connect to V_{SS} and V_{DD}, respectively. Pin G4 and H4 are output clocks. For this application, Tied to V_{DD} are recommended.

Block Diagram



Note: The functional block diagram illustrates simplified device operation. See truth table, pin descriptions and timing diagram information.

Pin Descriptions

Name	I/O Type	Descriptions	Note
V_{DD}		Power Supply	
V_{SS}		Ground	
V_{DDQ}		Output Power Supply	
K	Input	Input Clock	
$\overline{K}$	Input	Input Clock	
$\overline{SS}$	Input	Synchronous Chip Select	
$\overline{SWE}$	Input	Synchronous Write Enable	
V_{REF}	Input	I/O Reference Voltage	
SAn	Input	Synchronous Address	n = 0, 1, 2, ... 14, 15
$\overline{SWEx}$	Input	Synchronous Byte Write Enable	x = a, c
$\overline{G}$	Input	Asynchronous Output Enable	
ZQ		Output Impedance Control	1
DQxm	I/O	Synchronous Data Input/Output	x = a, c m = 0, 1, 2, ... 8
Mn	Input	Output Protocol Mode Select	2n = 1, 2
TMS	Input	Boundary Scan Test Mode Select	
TCK	Input	Boundary Scan Test Clock	
TDI	Input	Boundary Scan Test Data In	
TDO	Output	Boundary Scan Test Data Out	
NC		No Connection	

Notes: 1. ZQ is to be connected to V_{SS} via a resistance RQ where 175 Ω ≤ RQ ≤ 350 Ω, if ZQ = V_{DD} output buffer impedance will be minimum push pull output buffer mode.

2. M1 and M2 need to connect to either V_{SS} or V_{DD}, respectively. The state of the Mode control inputs must be set before power-up and must not change during device operation. Mode control inputs are not standard inputs and may not meet V_{IH} or V_{IL} specifications.

M1	M2	Protocol
V_{SS}	V_{DD}	Single Clock Register Register

Truth Table

(1) Single differential clock Mode (Register Register Mode)

SS	G	SWE	SWEa	SWEc	K	K	Operation	DQa	DQc
H	X	X	X	X	L-H	H-L	Dead (not selected)	High-Z	High-Z
L	H	H	X	X	L-H	H-L	Dead (Dummy read)	High-Z	High-Z
L	L	H	X	X	L-H	H-L	Read	Dout	Dout
L	X	L	L	L	L-H	H-L	Write	Din	Din
L	X	L	H	L	L-H	H-L	Write	High-Z	Din
L	X	L	L	H	L-H	H-L	Write	Din	High-Z

Notes: 1. X means don't care for synchronous inputs, and H or L for asynchronous inputs.
2. SWE, SS, SWEa, SWEc, SA are sampled at the rising edge of K clock.

Absolute Maximum Ratings

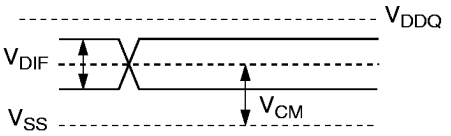
Parameter	Symbol	Value	Unit	Note
Supply voltage	V_{DD}	−0.5 to +4.6	V	1
Output Supply Voltage	V_{DDQ}	−0.5 to 1.6	V	1
Voltage on any pin	V_{IN}	−0.5 to V_{DD}+0.5 (4.6 V max)	V	1
Operating Temperature	Ta	0 to 70	°C	
Storage Temperature	Tstg (bias)	-55 to 125	°C	
Output Current per pin	Iout	±70	mA	
Power dissipation	Pd	2.2	W	

Notes: 1. All voltage are referenced to V_{SS}.
2. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted the Operation Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
3. The device is tested under the minimum transverse air flow of 2.5 meters per second for the DC and AC specifications shown in the tables.
4. Power Up Initialization
The following supply voltage application sequence is recommended: V_{SS}, V_{DD} then V_{DDQ}.

Recommended DC Operating Conditions (Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{DD}	3.2	3.3	3.6	V	
Output Supply voltage	V_{DDQ}	1.2	1.5	1.6	V	
Input voltage Logic High Level	V_{IH}	V_{REF} + 0.2	—	V_{DDQ} + 0.3	V	
Logic Low Level	V_{IL}	-0.3	—	V_{REF} - 0.2	V	
I/O Reference DC Voltage	V_{REF}(DC)	0.6	—	0.9	V	
I/O Reference AD Voltage	V_{REF}(AC)	—	—	V_{REF}(DX) X 5%	V_{PP}	
Clock input differential Voltage	VDIF	0.4			V	2
Clock input common mode voltage	VCM	0.6	—	0.9	V	2

Note: 1. Clock input common mode voltage VCM V_{REF}(AC) may not exceed 5% of V_{REF}(DC).
2. Differential input levels.



DC Characteristics (Ta = 0 to 70°C, V_{DD} = 3.2 V to 3.6 V)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Input Leakage Current	I_{LI}	-5	—	5	µA	1
Output Leakage Current	I_{LO}	-5	—	5	µA	2
V_{DD} Operating Current	I_{DD}	—	—	600	mA	3
Output Voltage	V_{OL}	0	—	0.4	V	4
	V_{OH}	0.8	—	V_{DDQ} + 0.3	V	4
ZQ pin connect Resistance	R_Q	175	250	350	Ω	
Output Current	I_{OL}	2.5×V_{DDQ} /RQ-20%	—	2.5×V_{DDQ} /RQ+20%	mA	5
	I_{OH}	2.5×V_{DDQ} /RQ-20%	—	2.5×V_{DDQ} /RQ+20%	mA	6

Note: 1. $0 \le Vin \le V_{DDQ}$
2. $0 \le VI/O \le V_{DDQ}$, Tristate I/O, $\overline{SS}$ = V_{IH} or $\overline{G}$ = V_{IH}
3. Iout = 0 mA, t_{KHKH} = 7 ns, Address increment pattern, read 50% / write 50%, V_{DD} = V_{DD} max, $\overline{SS}$ = V_{IL}
4. Minimum impedance push pull output buffer mode, I_{OH} = -2.4 mA, I_{OL} = 2.4 mA
5. Measured at V_{OL} = 1/2
6. Measured at V_{OH} = 1/2

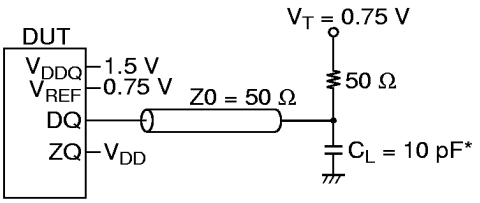
Input Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Min	Max	Unit	Pin Name	Note
Address Input Capacitance	C_{INA}	—	5	pF	SAn, $\overline{SS}$, $\overline{SWE}$, $\overline{SWEx}$	1
Clock Input Capacitance	C_{INC}	—	8	pF	K, $\overline{K}$, $\overline{G}$, C, $\overline{C}$	1
I/O Capacitance	C_{INIO}	—	8	pF	DQxm	1

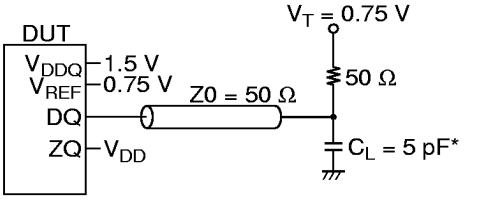
Note: 1. This value is measured by sampling and not 100% tested.

AC Test Conditions

- Temperature — 0°C ≤ Ta ≤ 70°C
- Input Reference Point for Differential Signals — Differential Cross-Over Point
- Input Reference Point for Single-Ended Signals — 0.75 V
- Input pulse levels — 0 to 1.5 V
- Clock Input pulse levels — 0 to 1.5 V
- Input Rise/Fall Time — 1.0 ns (20% to 80%)
- Clock input Rise/Fall Time — 1.0 ns (20% to 80%)
- Output timing reference — 0.75 V
- Input reference DC voltage (Vref) — 0.75 V
- Output load — See figures



Load A (t_{KHQV}, t_{GLQV})



* Including scope and jig capacitance

Load B (for t_{KHQX}, t_{KHQX2}, t_{GLQX}, t_{KHQZ}, t_{GHQZ})

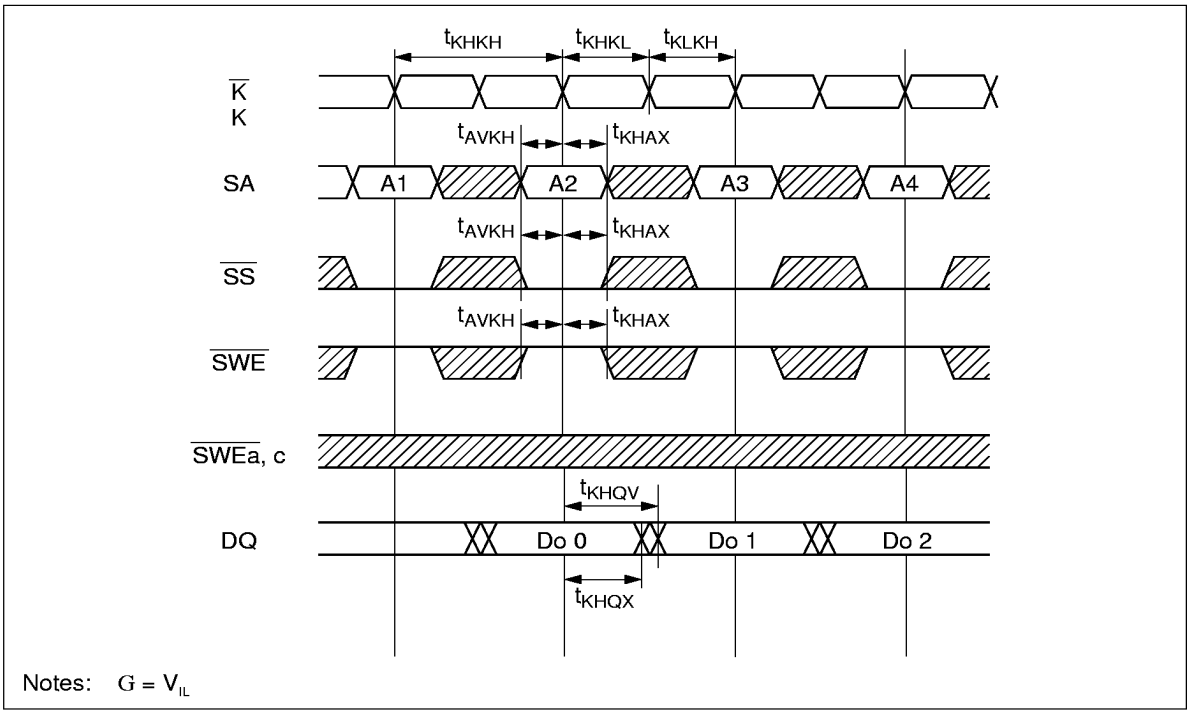
AC Characteristics (0°C ≤ Ta ≤ 70°C)

Parameter	Symbol	Min	Max	Unit	Notes
Clock Control					
Clock Cycle	t_{KHKH}	7.0	—	ns	
Clock High Width	t_{KHKL}	3.0	—	ns	
Clock Low Width	t_{KLKH}	3.0	—	ns	
Read Control					
K Clock Access	t_{KHQV}	—	4.0	ns	
Output Enable Access	t_{GLQV}	—	4.0	ns	
K High to Q Change	t_{KHQX}	0.5	—	ns	
Output Enable to Low-Z	t_{GLQX}	0.5	—	ns	1
Output Buffer Control					
K High to Low-Z	t_{KHQX2}	0.5	—	ns	1
K High to Q Hi-Z	t_{KHQZ}	0.0	4.0	ns	1
Output Enable to Hi-Z	t_{GHQZ}	0.0	4.0	ns	1
Setup Times					
Address Setup Time	t_{AVKH}	0.5	—	ns	SA, SS, SWE, SWEa, SWEc
Data Setup Time	t_{DVKH}	0.5	—	ns	
CID Update Setup	t_{GHKH}	2.0	—	ns	2
Hold Times					
Address Hold Time	t_{KHAX}	2.2	—	ns	SA, SS, SWE, SWEa, SWEc
Data Hold Time	t_{KHDX}	2.2	—	ns	
CID Update Hold	t_{KHGX}	2.0		ns	2
CID Update					
CID Update Time	t_{GHGL}	t_{KHKH}		ns	2

Notes: 1. Transition is measured ±100 mV from steady voltage with specified loading in Load B. This parameter is sampled and not 100% tested.

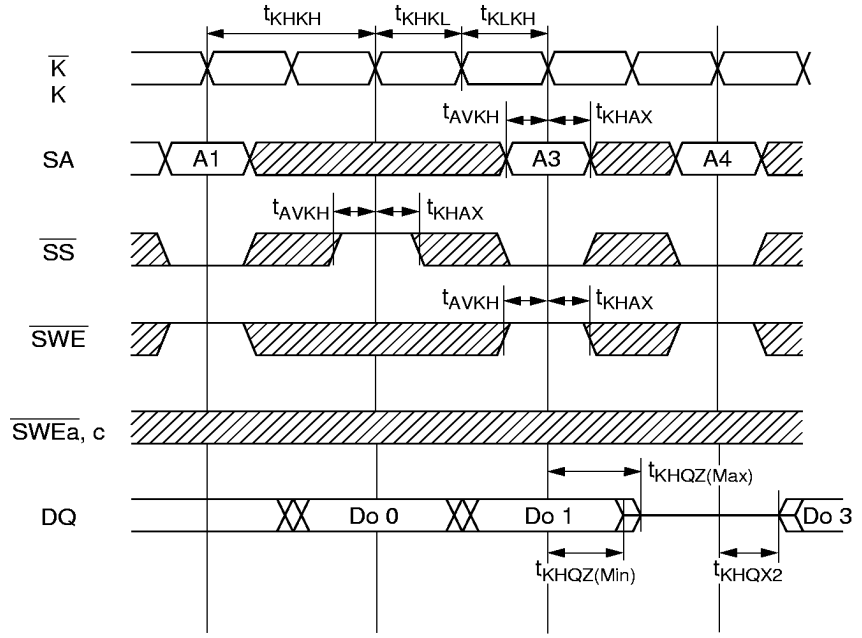
2. These specifications are required for impedance updates when G is high. At least the same number of cycles of initialization as the depth of the part are required to provide initial impedance matching.

Read Cycle 1



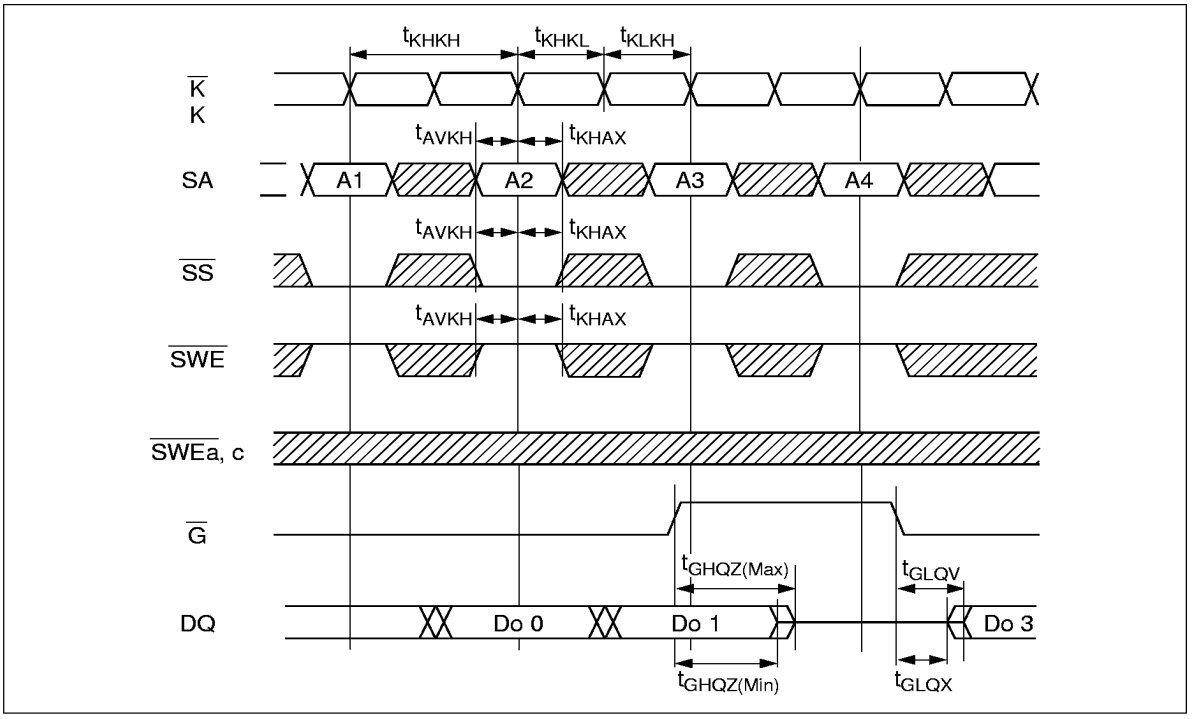
Notes: $\overline{G} = V_{IL}$

Read Cycle 2 ($\overline{SS}$ Controlled)

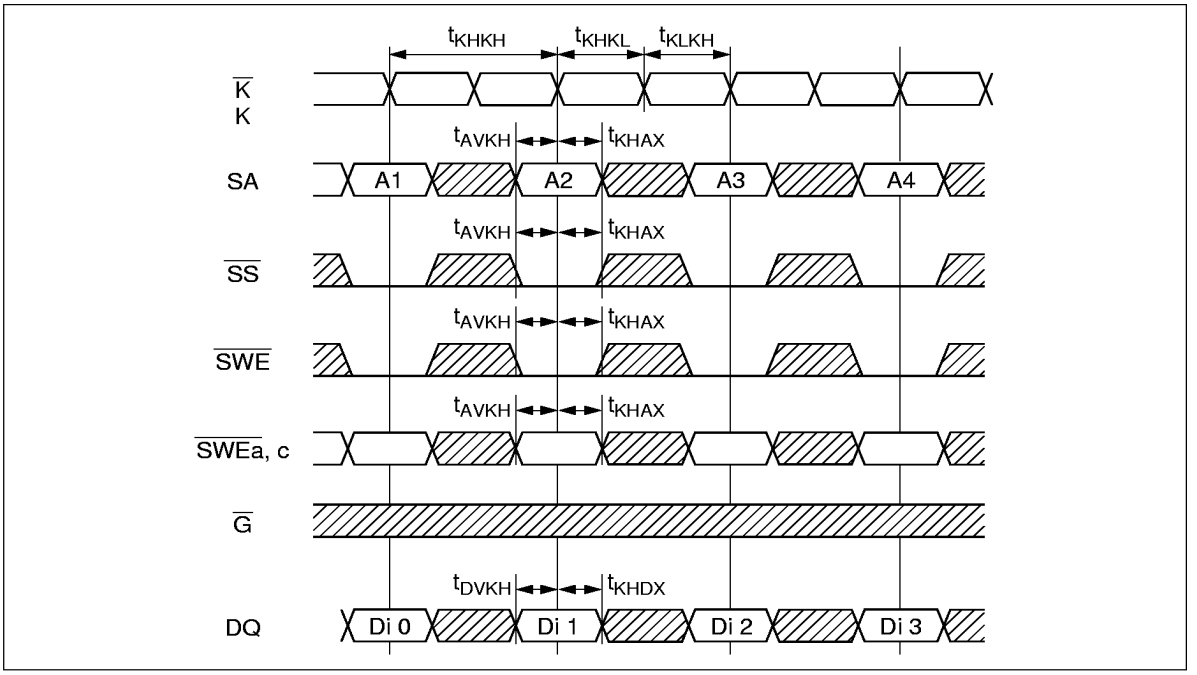


Note: $\overline{G} = V_{IL}$

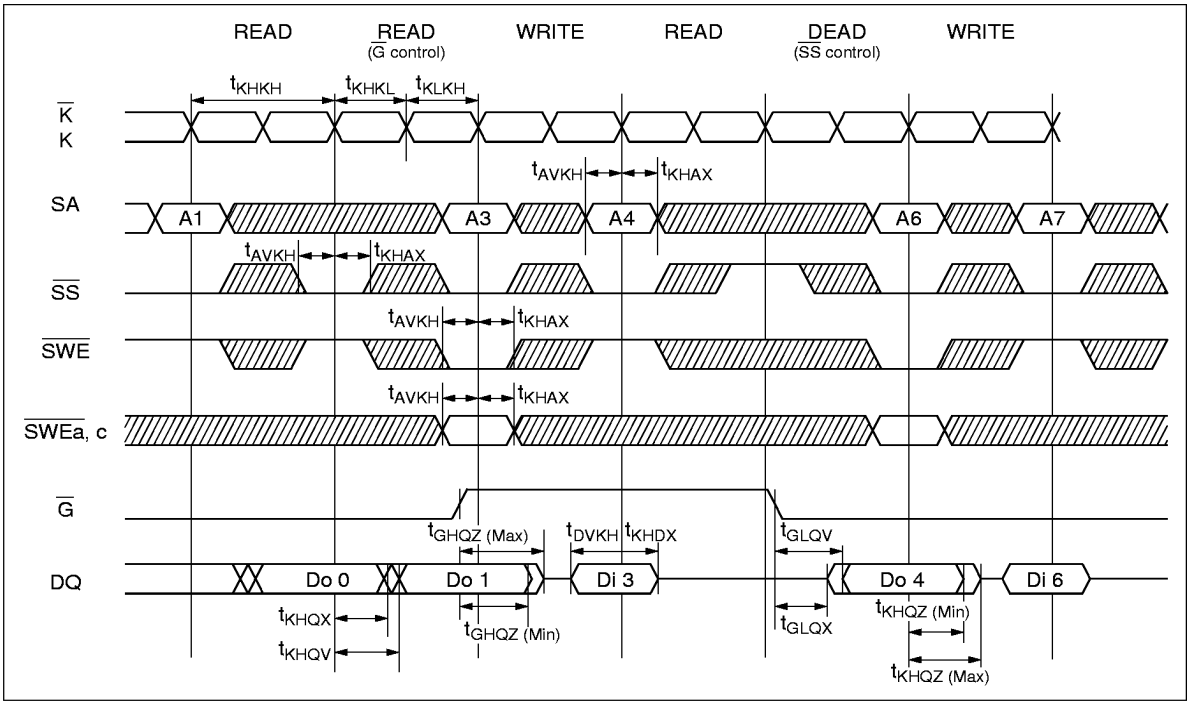
Read Cycle 3 ($\overline{G}$ Controlled)



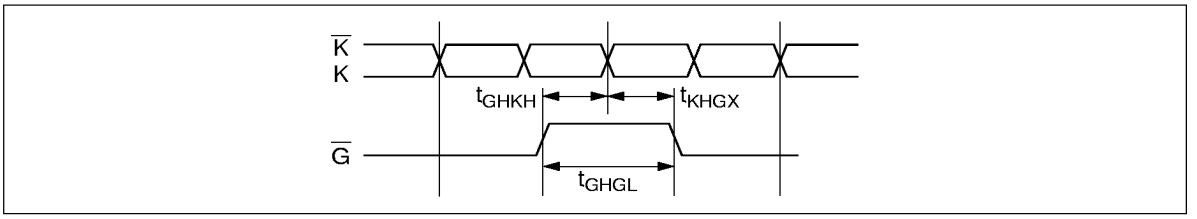
Write Cycle



Read-Write Cycle



Impedance update timing



Boundary Scan Test Access Port Operations

Overview

In order to perform the interconnect testing of the modules that include this SRAM, the serial boundary scan test access port (TAP) is designed to operate in a manner consistent with IEEE Standard 1149.1 - 1990. But does not implement all of the functions required for 1149.1 - 1990.

Test Access Port Pins

Symbol I/O	Name
TCK	Test Clock
TMS	Test Mode Select
TDI	Test Data In
TDO	Test Data Out

Note: This Device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. To disable the TAP, TCK must be connected to V_{SS}. TDO should be left unconnected.

TAP DC Operating Characteristics (Ta = 0˚C to 70˚C)

Parameter	Symbol	Min	Max	Note
Boundary scan Input High voltage	V_{IH}	2.2 V	V_{DD} + 0.3 V	
Boundary scan Input Low voltage	V_{IL}	-0.5 V	0.8 V	
Boundary scan Input Leakage Current	I_{LI}	-5µA	+5µA	1
Boundary scan Output Low voltage	V_{OL}	-0.3 V	0.4 V	2
Boundary scan Output High voltage	V_{OH}	2.4 V	V_{DD} + 0.3 V	3

Notes: 1. $0 \le Vin \le V_{DD}$
2. I_{OL} = 2 mA
3. I_{OH} = -2 mA

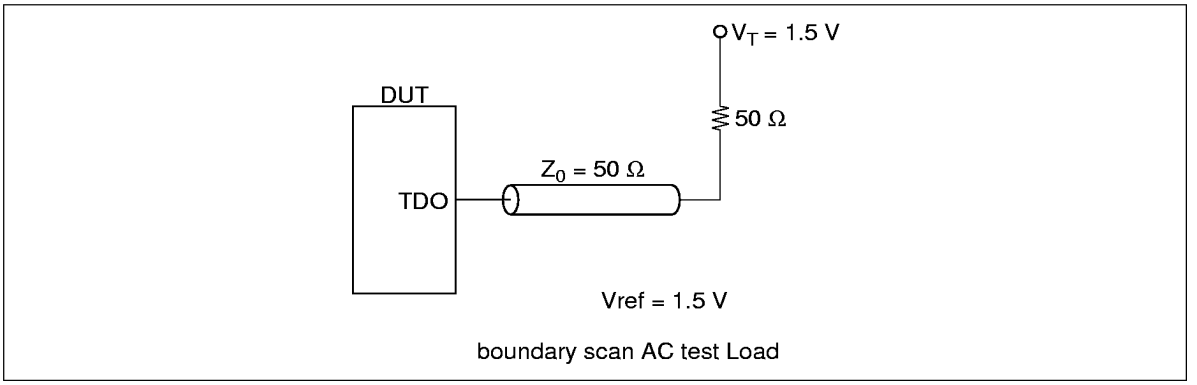
TAP AC Operating Characteristics (Ta = 0°C to 70°C)

Parameter	Symbol	Min	Max	Unit
Test Clock Cycle Time	t_{THTH}	67	—	ns
Test Clock High Pulse Width	t_{THTL}	30	—	ns
Test Clock Low Pulse Width	t_{TLTH}	30	—	ns
Test Mode Select Setup	t_{MVTH}	10	—	ns
Test Mode Select Hold	t_{THMX}	10	—	ns
Capture Setup	t_{CS}	10	—	ns
Capture Hold	t_{CH}	10	—	ns
TDI Valid to TCK High	t_{DVTH}	10	—	ns
TCK High to TDI Don't Care	t_{THDX}	10	—	ns
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns
TCK Low to TDO Valid	t_{TLQV}	—	20	ns

Notes: 1. $t_{CS} + t_{CH}$ defines the minimum pause in RAM I/O pad transitions to assure pad data capture.

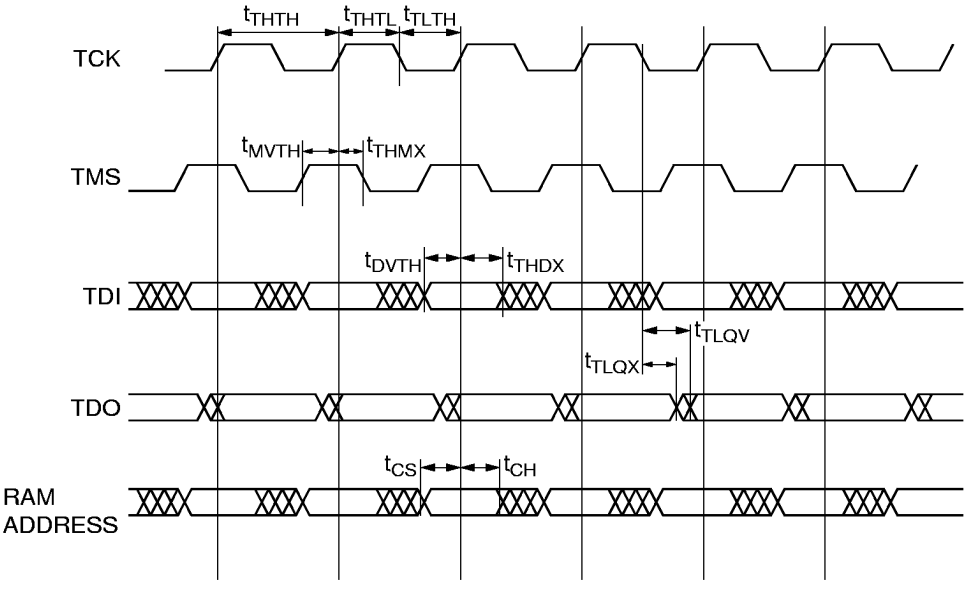
TAP AC Test Conditions

- Temperature — 0°C ≤ Ta ≤ 70°C
- Input Reference Point for Single-Ended Signals — 1.5 V
- Input pulse levels — 0 to 3.0 V
- Input Rise/Fall Time — 1.0 ns (20% to 80%)
- Output timing reference — 1.5 V
- Test load termination supply voltage (V_T) — 1.5 V
- Output Load — See boundary scan AC test load



boundary scan AC test Load

TAP Timing Diagram



TAP Timing Diagram

Test Access Port Registers

Register Name	Length	Symbol	Note
Instruction Register	3 bits	IR [0;2]	
Bypass Register	1 bits	BP	
ID Register	32 bits	ID [0;31]	
Boundary Scan Register	51 bits	BS [1;51]	

TAP Controller Instruction Set

IR2	IR1	IR0	Instruction	Operation
0	0	0	SAMPLE-Z	Tristate all data drivers and capture the pad value
0	0	1	IDCODE	
0	1	0	SAMPLE-Z	Tristate all data drivers and capture the pad value
0	1	1	BYPASS	
1	0	0	SAMPLE	
1	0	1	BYPASS	
1	1	0	BYPASS	
1	1	1	BYPASS	

Note: This Device does not perform EXTEST, INTEST or the preload portion of the PRELOAD command in IEEE 1149.1.

Boundary Scan Order

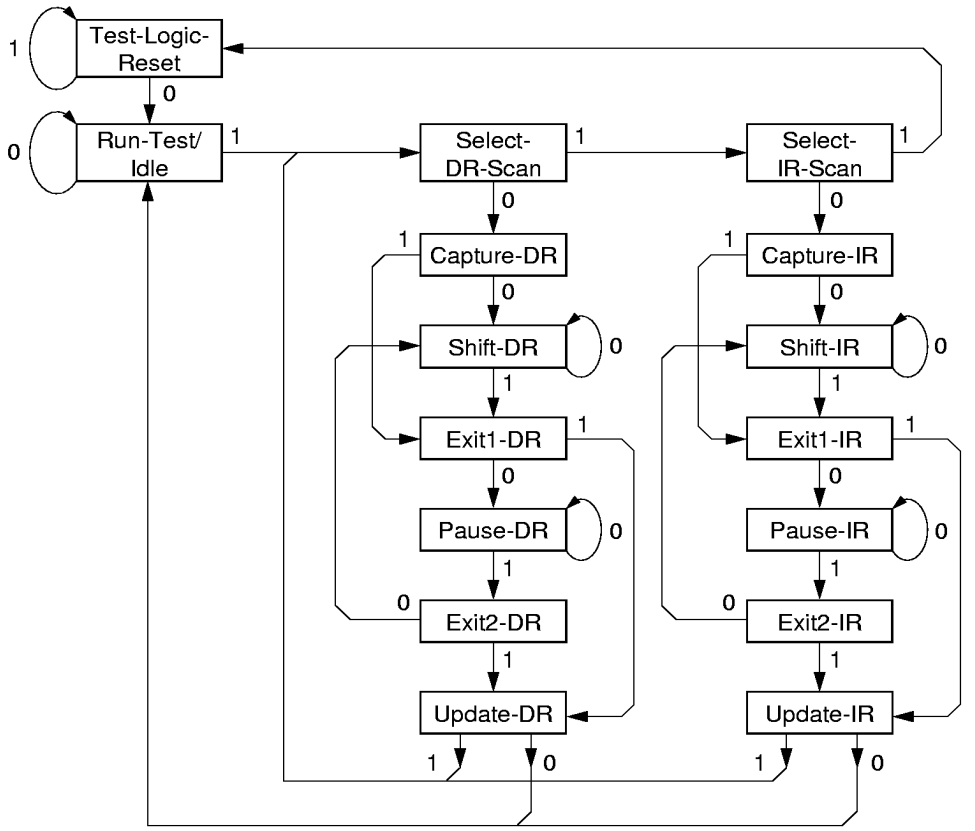
Bit #	Bump ID	Signal Name	Bit #	Bump ID	Signal Name
1	5R	M2	27	2B	NC
2	6T	SA4	28	3A	SA12
3	4P	SA5	29	3C	SA13
4	6R	SA6	30	2C	SA14
5	5T	SA7	31	2A	SA15
6	7T	NC	32	1D	DQc0
7	7P	DQa0	33	2E	DQc1
8	6N	DQa1	34	2G	DQc2
9	6L	DQa2	35	1H	DQc3
10	7K	DQa3	36	3G	SWEc
11	5L	SWEa	37	4D	ZQ
12	4L	K	38	4E	SS
13	4K	K	39	4G	C
14	4F	G	40	4H	C
15	6H	DQa4	41	4M	SWE
16	7G	DQa5	42	2K	DQc4
17	6F	DQa6	43	1L	DQc5
18	7E	DQa7	44	2M	DQc6
19	6D	DQa8	45	1N	DQc7
20	6A	SA8	46	2P	DQc8
21	6C	SA9	47	3T	SA0
22	5C	SA10	48	2R	SA1
23	5A	SA11	49	4N	SA2
24	6B	NC	50	2T	SA3
25	5B	NC	51	3R	M1
26	3B	NC			

Notes: 1. Bit#1 is the first scan bit to exit the chip.
2. NC pads listed in the TABLE are represented in the Boundary Scan Register by a Place Holder. Place Holder registers are internally connected to vdd.
3. K, K, C, C are sampled individually. In scan modes each of these differential inputs are referenced to V_{REF}.

ID register

Bit#	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	X	X	X	X	0	0	1	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
	Vendor Revision No.				4M, 16M Depth		Depth			4M, 16M Width		Width			Use in the future						Vendor ID No.											Fix

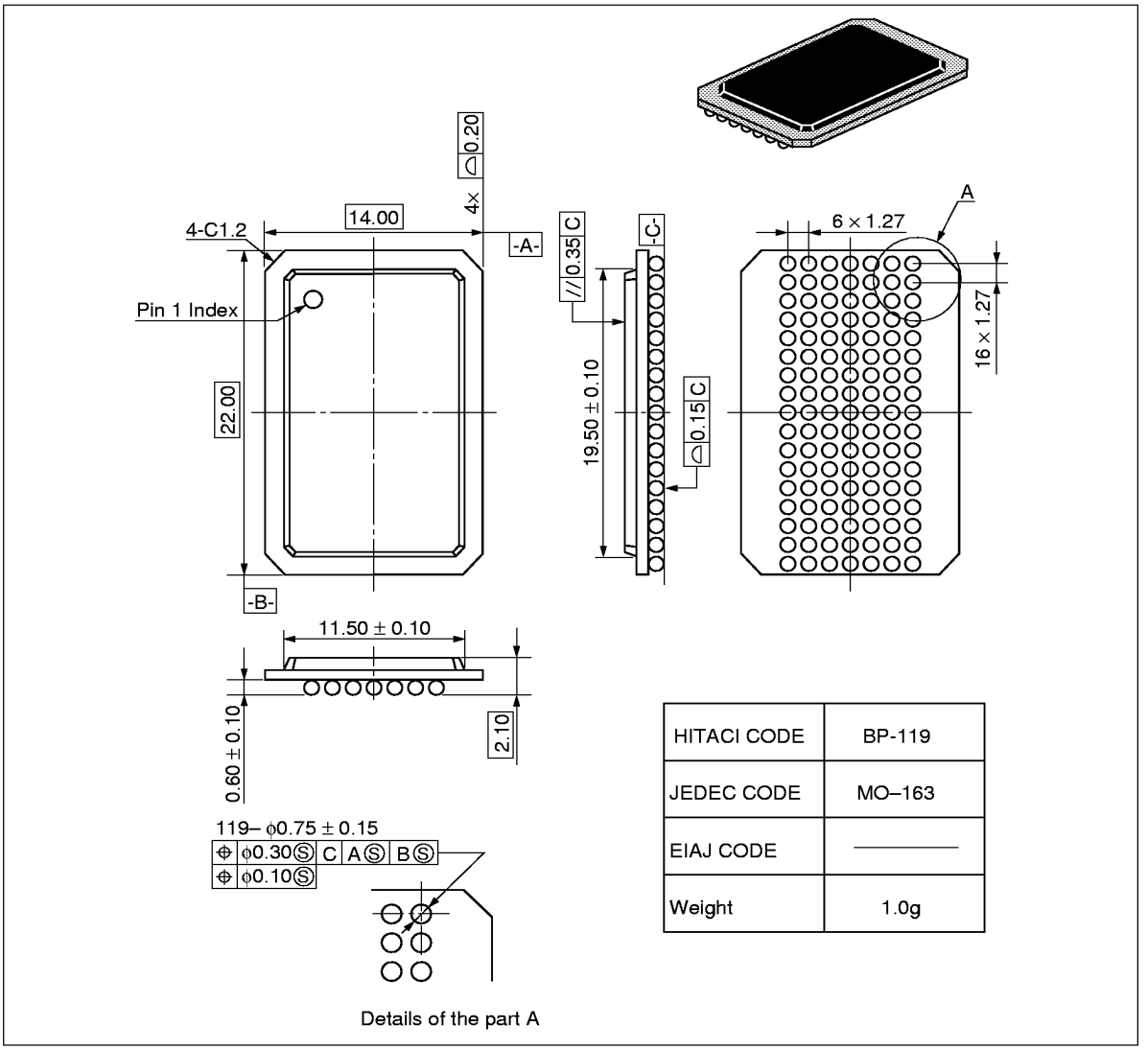
TAP Controller State Diagram



Note: The value adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.
No matter what the original state of the controller, it will enter Test-Logic-Reset when TMS is held high for at least five rising edges of TCK.

Package Outline

HM67G1886BP (BP-119) **Unit : mm**



HITACI CODE	BP-119
JEDEC CODE	MO–163
EIAJ CODE	———
Weight	1.0g