HM67S3632 Series

32,768-words × 36-bits Synchronous Fast Static RAM

HITACHI

ADE-203-446B(Z)
Preliminary
Rev. 2
Mar. 28, 1996

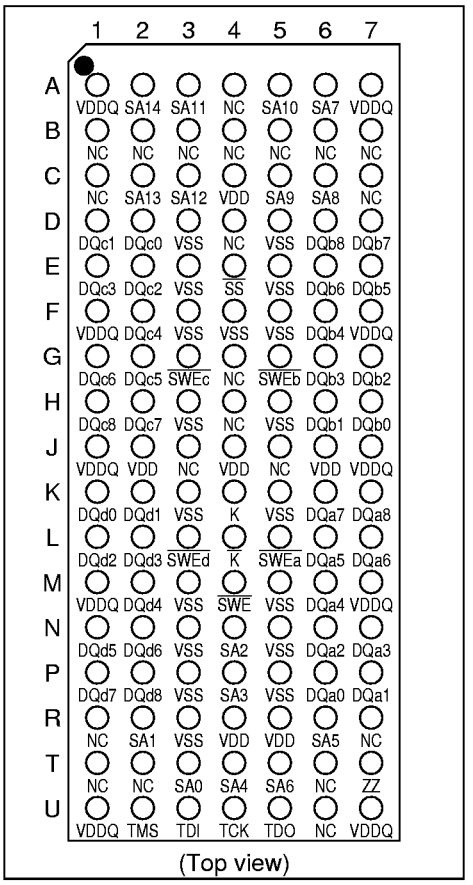
Features

- 3.3 V – 3 % + 5 % Operation
- LVCMOS Compatible Input and Output
- Synchronous Operation
- Self-timed Late Write
- Byte Write Control
- Power down mode is provided
- Differential PECL Clock Inputs
- Boundary Scan
- Single Clock Register-Register Mode

Ordering Information

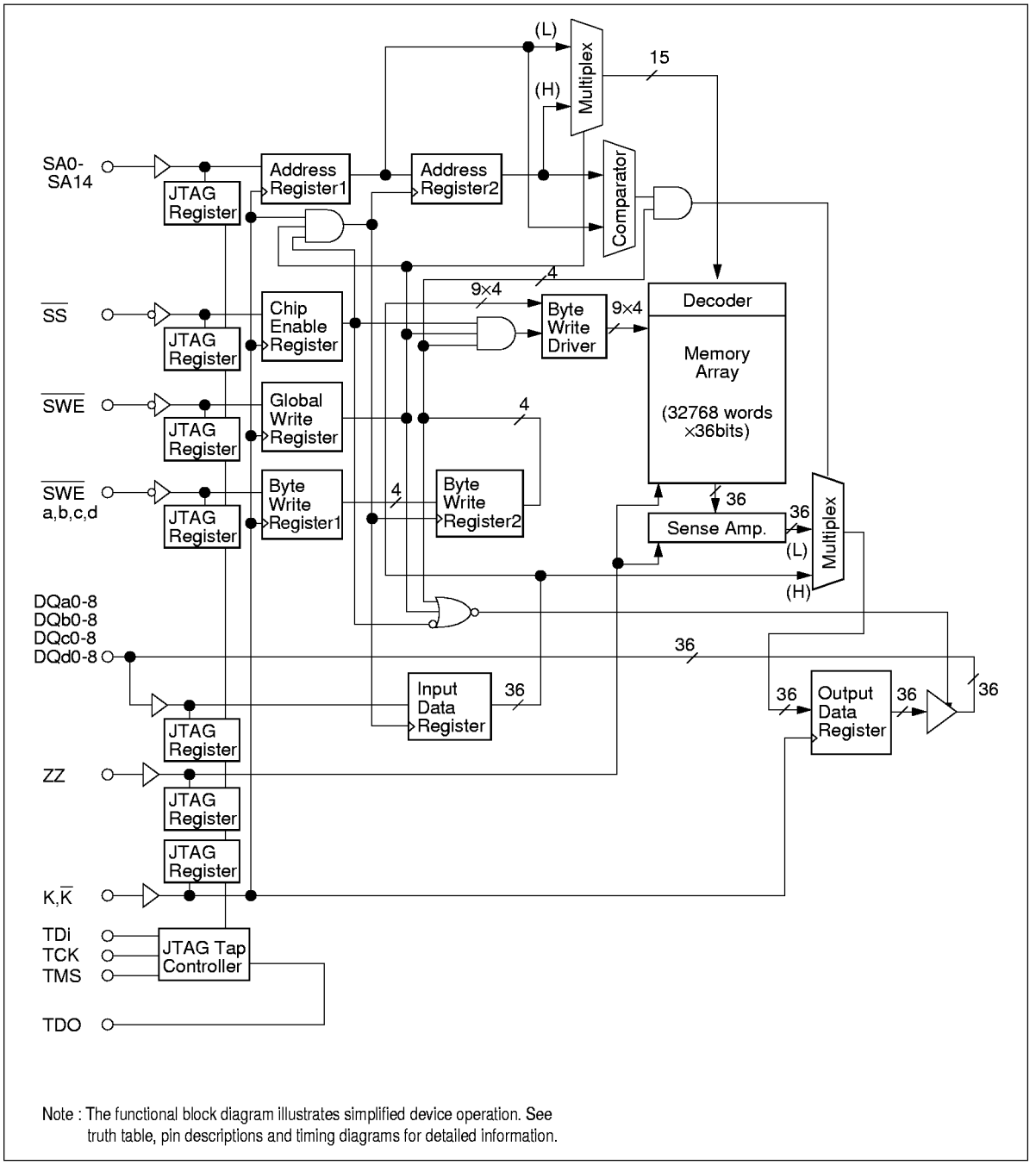
Type Number	Cycle Time	Clock Access	Package
HM67S3632BP-5	5 ns	3.0 ns	119 Bump 1.27 mm
HM67S3632BP-6	6 ns	3.5 ns	14 mm × 22 mm BGA (BP-119)
HM67S3632BP-7	7 ns	4.0 ns	

Pin Arrangement



Pin R3 and R5 are clock mode pins, For this application,
Pin R3 and R5 need to connect to Vss and V_{DD} respectively.
Pin F4 needs to connect to Vss.

Block Diagram



Note : The functional block diagram illustrates simplified device operation. See truth table, pin descriptions and timing diagrams for detailed information.

Pin Descriptions

Name	I/O Type	Descriptions	Note
V_{DD}		Power Supply	
V_{SS}		Ground	
V_{DDQ}		Output Power Supply	
K	Input	Clock	
$\overline{K}$	Input	Clock	
$\overline{SS}$	Input	Synchronous Chip Select	
$\overline{SWE}$	Input	Synchronous Write Enable	
San	Input	Synchronous Address	n = 0, 1, 2, ... 14
$\overline{SWEx}$	Input	Synchronous Byte Write Enable Select	x = a, b, c, d
ZZ	Input	Power Down Mode Select	
DQxm	I/O	Synchronous Data Input/Output	x = a, b, c, d, m = 0, 1, 2, ... 8
TMS	Input	Boundary Scan Test Mode Select	
TCK	Input	Boundary Scan Test Clock	
TDI	Input	Boundary Scan Test Data In	
TDO	Output	Boundary Scan Test Data Out	
NC		No Connection	

Truth Table

ZZ	SS	SWE	SWEx	K	Operation	DQxm
H	X	X	X	H-L	Power Down Mode	High-Z
L	H	H	X	H-L	Dead (Not selected)	High-Z
L	L	H	X	H-L	Read	Dout
L	L	L	L	H-L	Write (x)	Din (x)
L	L	L	H	H-L	Not Write (x)	High-Z (x)

Notes: 1. X means don't care for synchronous inputs, and H or L for asynchronous inputs.
2. SWE, SS, SWEa to SWEd are sampled at the rising edge of K clock.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Supply voltage	V_{DD}	–0.5 to +4.6	V	1
Output Supply Voltage	V_{DDQ}	–0.5 to V_{DD}+0.5 (4.6 V max)	V	1
Voltage on any pin	V_{IN}	–0.5 to V_{DD}+0.5 (4.6 V max)	V	1
Operating Temperature	Ta	0 to 70	°C	
Storage Temperature	Tstg	–55 to 125	°C	
Input Latchup Current	I_{LI}	200	mA	
Output Short Circuit Current	Iout	±25	mA	

Notes: 1. All voltage are referenced to V_{SS}.
2. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted the Operation Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
3. The device is tested under the minimum transverse air flow of 2.5meters per second for the DC and AC specifications shown in the tables.
4. Power Up Initialization
The following supply voltage application sequence is recommended: V_{SS}, V_{DD} then V_{DDQ}.

DC Characteristics (Ta = 0 to 70°C, V_{DD} = 3.3 V –3% + 5%)

		–5			–6 / –7				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Note**
Supply Voltage	V_{DD}	3.2	3.3	3.465	3.2	3.3	3.465	V	1
Output Supply Voltage	V_{DDQ}	3.2	3.3	3.465	3.2	3.3	3.465	V	
Input Voltage: Logic High Level	V_{IH}	0.7*V_{DD}	—	V_{DD} + 0.3	0.7*V_{DD}	—	V_{DD} + 0.3	V	
: Logic Low Level	V_{IL}	–0.5	—	0.8	–0.5	—	0.8	V	
PECL Logic Low Level	V_{IL} (PECL)	1.490	—	1.825	1.490	—	1.825	V	
PECL Logic High Level	V_{IH} (PECL)	2.135	—	2.420	2.135	—	2.420	V	
Leakage Current: Input Leakage Current	I_{LI}	–1	—	+1	–1	—	+1	µA	1
: Output Leakage Current	I_{LO}	–1	—	+1	–1	—	+1	µA	2
PECL Input Leakage Current Low	I_{IL} (PECL)	—	—	50	—	—	50	µA	
PECL Input Leakage Current High	I_{IH} (PECL)	—	—	150	—	—	150	µA	
V_{DD} Operating Current: excluding output drivers	I_{DD}	—	—	480	—	—	440	mA	3
Standby Current (Power down mode)	I_{SB}	—	—	20	—	—	20	mA	5
Output Voltage: Logic Low	V_{OL}	—	—	0.4	—	—	0.4	V	4
: Logic High	V_{OH}	2.4	—	—	2.4	—	—	V	4

Note: 1. $0 \le Vin \le V_{DD}$
2. $0 \le VI/O \le V_{DDQ}$, Tristate I/O
3. Tristate I/O, Address increment read 50% / write 50%, $V_{DD} = V_{DD}$ max, Frequency = 167 MHz (–6/–7), 200 MHz (–5)
4. I_{OH} = –2 mA or I_{OL} = 2 mA
5. All inputs (except clock) are held at either V_{SS} or V_{DD}, and ZZ is held at V_{DD}

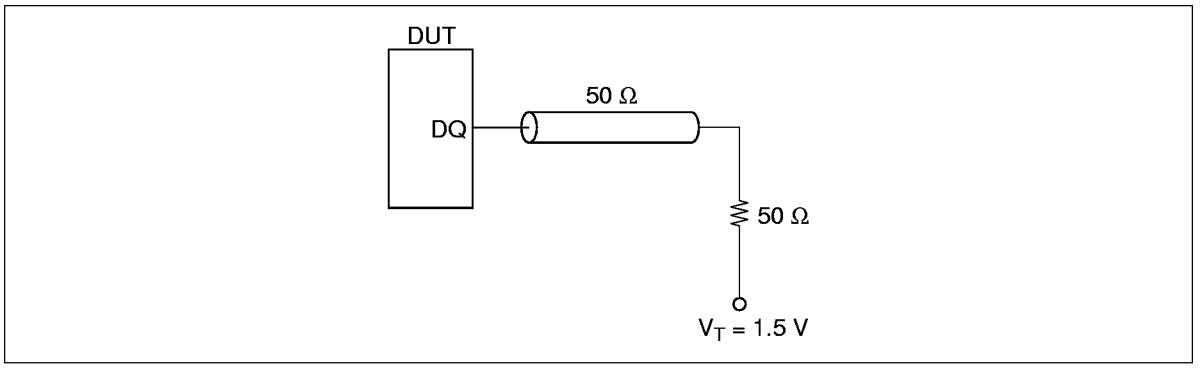
Input Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	**Symbol**	**Min**	**Max**	**Unit**	**Pin Name**	**Note**
Input Capacitance	C_{IN}	—	5	pF	SAn, SS, SWE, SWEx	1
Clock Input Capacitance	C_{INCLK}	—	8	pF	K, K	1
I/O Capacitance	C_{INIO}	—	8	pF	DQxm	1

Note: 1. This value is measured by sampling and not 100% tested.

AC Test Conditions

- Temperature : 0°C ≤ Ta ≤ 70°C
- Input Reference Point for Differential Signals : Differential Cross-Over Point
- Input Reference Levels : 2.2 V / 0.8 V
- Input pulse levels : 0 to 2.5 V
- Clock pulse levels : 1.8 to 2.1 V
- Input Rise/Fall Time : 1.0 ns (10% to 90%)
- Clock input Rise/Fall Time : 0.2 ns (10% to 90%)
- Output timing reference : 1.5V
- Output load : See figures

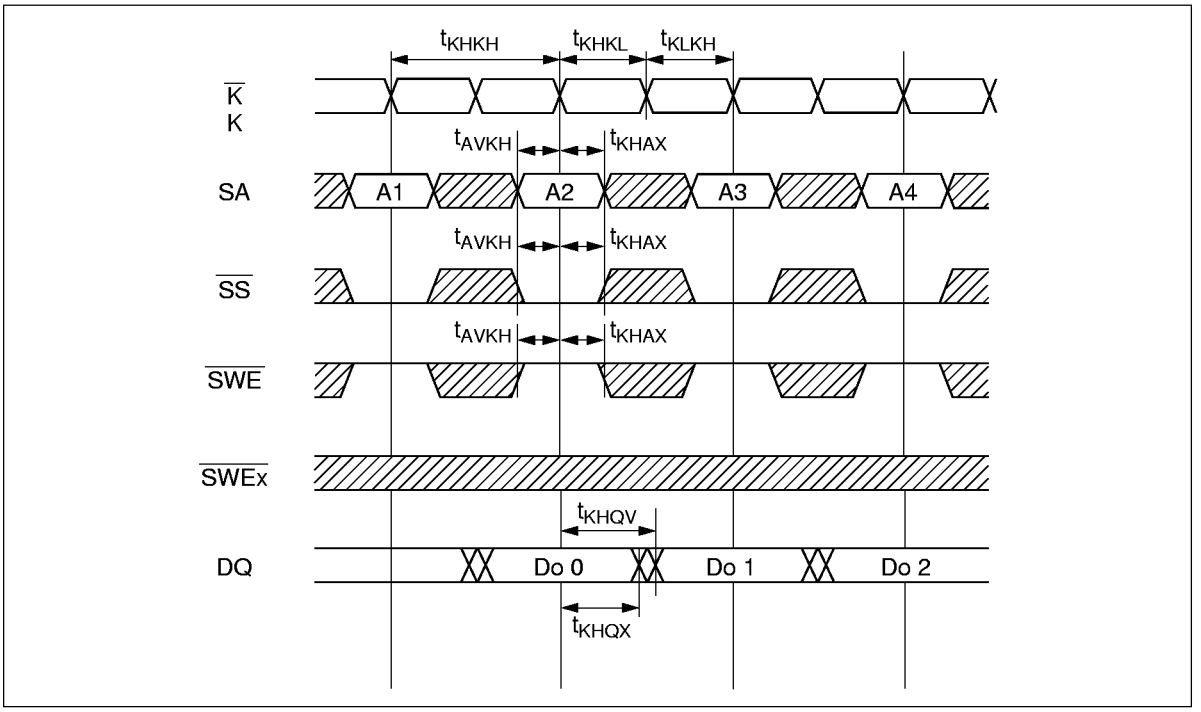


AC Characteristics (Ta = 0 to 70°C, V_{DD} = 3.3 V –3 % + 5 %)

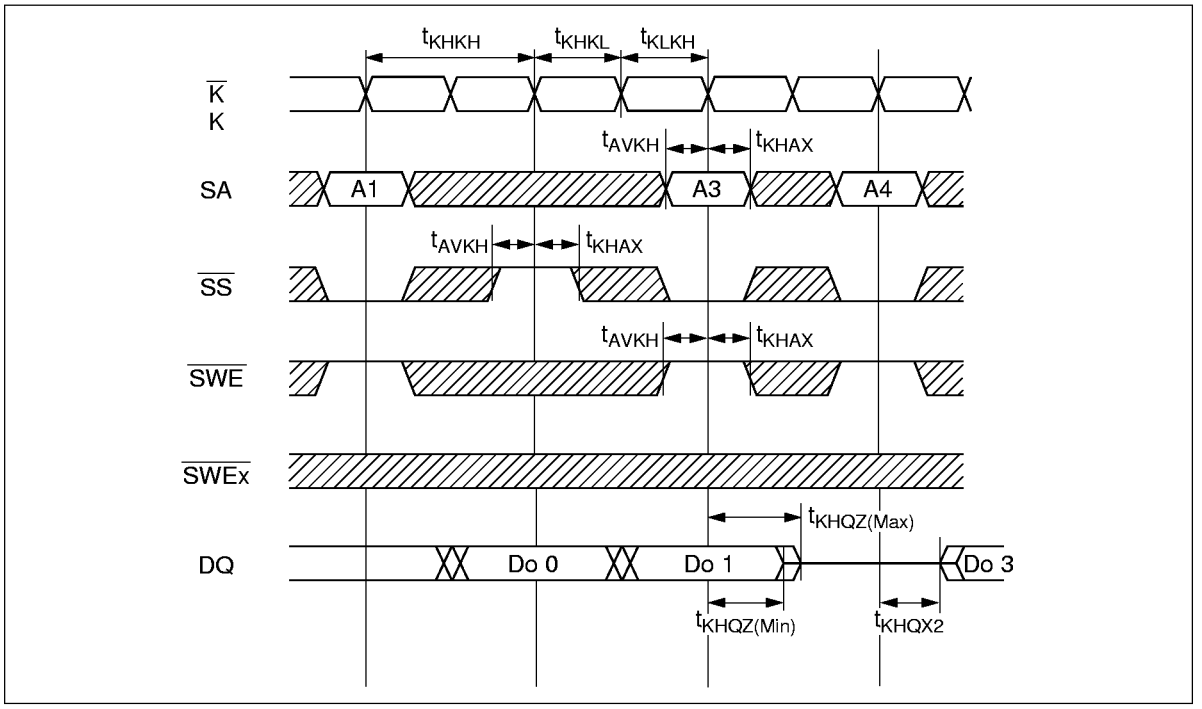
		–5		–6		–7			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Clock Control									
Clock Cycle	t_{KHKH}	5.0	—	6.0	—	7.0	—	ns	
Clock High Width	t_{KHKL}	2.0	—	2.0	—	2.0	—	ns	
Clock Low Width	t_{KLKH}	2.0	—	2.0	—	2.0	—	ns	
Read Control									
K Clock Access	t_{KHQV}	—	3.3	—	3.5	—	4.0	ns	
K High to Q Change	t_{KHQX}	0.5	—	0.5	—	0.5	—	ns	
Output Buffer Control									
K High to Low-Z	t_{KHQX2}	0.5	—	0.5	—	0.5	—	ns	1
K High to Q Hi-Z	t_{KHQZ}	0	3.5	0	4.0	0	4.0	ns	1
Setup Times									
Address Setup Time	t_{AVKH}	0.5	—	0.5	—	1.0	—	ns	SA, SS, SWE, SWEx
Data Setup Time	t_{DVKH}	0.5	—	0.5	—	1.0	—	ns	
Hold Times									
Address Hold Time	t_{KHAX}	1.0	—	1.0	—	1.0	—	ns	SA, SS, SWE, SWEx
Data Hold Time	t_{KHDX}	1.0	—	1.0	—	1.0	—	ns	

Notes: 1. Transition is measured ±200 mV from steady voltage with specified loading. This parameter is sampled and 100% tested.

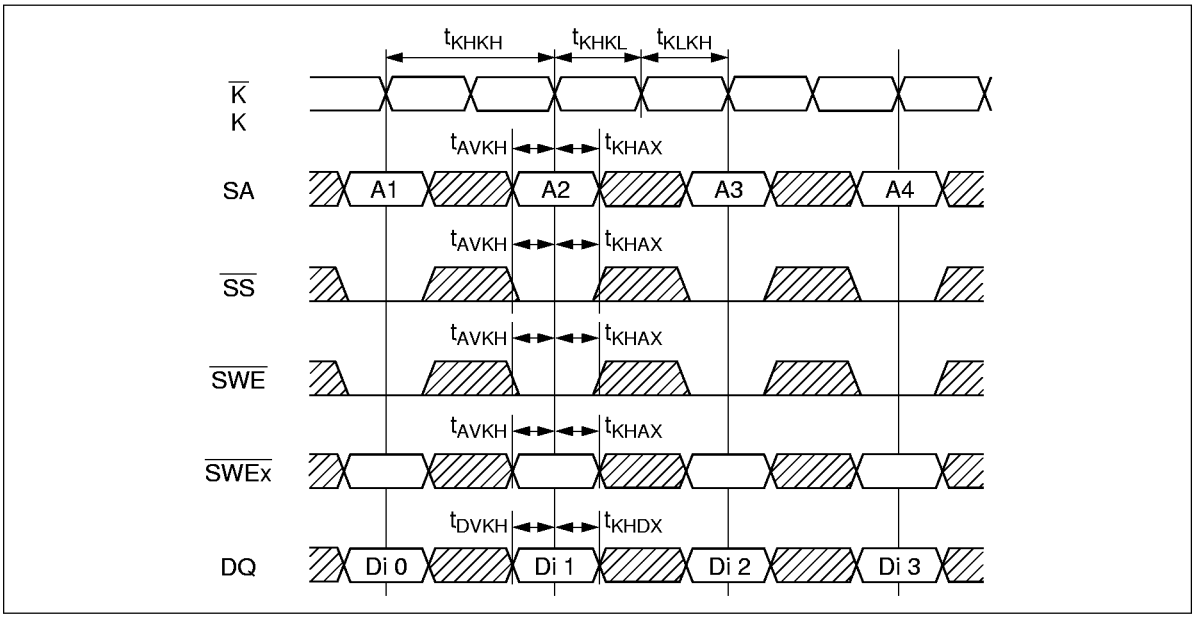
Read Cycle 1


tKHKH
tKHKL
tKLKH
K
K
tAVKH
tKHAX
SA
A1
A2
A3
A4
tAVKH
tKHAX
SS
tAVKH
tKHAX
SWE
SWEx
tKHQV
DQ
Do 0
Do 1
Do 2
tKHQX

Read Cycle 2 ($\overline{SS}$ Controlled)



Write Cycle


tKHKH
tKHKL
tKLKH
K
K
tAVKH
tKHAX
SA
A1
A2
A3
A4
SS
SWE
SWEx
tDVKH
tKHDX
DQ
Di 0
Di 1
Di 2
Di 3

Boundary Scan Test Access Port Operations

overview

In order to perform the interconnect testing of the modules that include this SRAM, the serial boundary scan test access port (TAP) is designed to operate in a manner consistent with IEEE Standard 1149.1 – 1990. But does not implement all of the functions required for 1149.1 – 1990.

Test Access Port Pins

Symbol I/O	Name
TCK	Test Clock
TMS	Test Mode Select
TDI	Test Data In
TDO	Test Data Out

Notes: This Device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. To disable the TAP, TCK must be connected to V_{SS}. TDO should be left unconnected.

TAP DC Operating Characteristics (Ta = 0°C to 70°C)

Parameter	Symbol	Min	Max	Note
Logic Input Logic High	V_{IH}	2.0 V	V_{DD} + 0.3 V	
Logic Input Logic Low	V_{IL}	–0.5 V	0.8 V	
Logic Input Leakage Current	I_{LI}	–1µA	+1µA	1
Output Logic Low	V_{OL}	—	0.4 V	2
Output Logic High	V_{OH}	2.4 V	—	3

Notes: 1. $0 \le Vin \le V_{DD}$
2. I_{OL} = 2 mA
3. I_{OH} = –2 mA

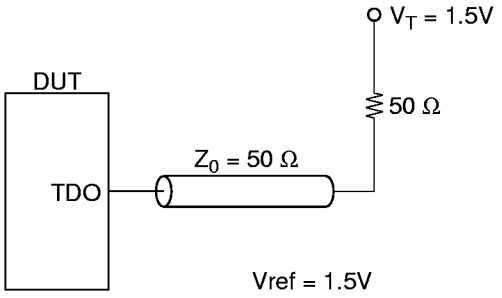
TAP AC Operating Characteristics (Ta = 0°C to 70°C)

Parameter	Symbol	Min	Max	Unit
Test Clock Cycle Time	t_{THTH}	67	—	ns
Test Clock High Pulse Width	t_{THTL}	30	—	ns
Test Clock Low Pulse Width	t_{TLTH}	30	—	ns
Test Mode Select Setup	t_{MVTH}	10	—	ns
Test Mode Select Hold	t_{THMX}	10	—	ns
Capture Setup	t_{CS}	10	—	ns
Capture Hold	t_{CH}	10	—	ns
TDI Valid to TCK High	t_{DVTH}	10	—	ns
TCK High to TDI Don't Care	t_{THDX}	10	—	ns
TCK Low to TDO Unknown	t_{TLQX}	0	—	ns
TCK Low to TDO Valid	t_{TLQV}	—	20	ns

Notes: 1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure pad data capture.

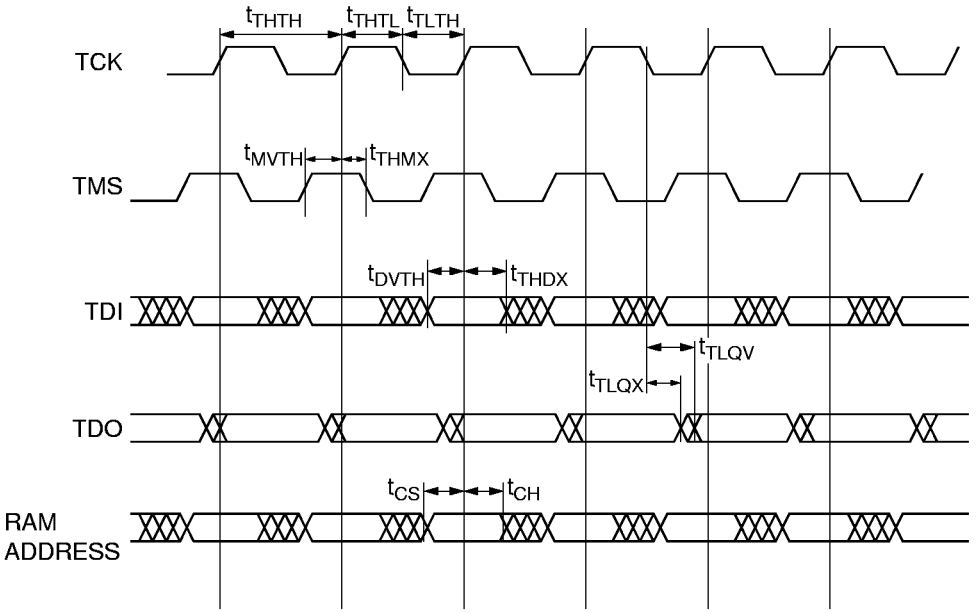
TAP AC Test Conditions

- Temperature : 0°C ≤ Ta ≤ 70°C
- Logic Input Timing Measurement Reference Level (V_{REF}) : 1.5 V
- Logic Input pulse level : 0 to 2.5 V
- Logic Input Rise/Fall Time : 1.0 ns (10% to 90%)
- Output timing measurement reference Level (V_{REF}) : 1.5 V
- Test load termination supply voltage (V_T) : 1.5 V
- Output Load : See figures



boundary scan AC test Load

TAP Timing Diagram



TAP Timing Diagram

Test Access Port Registers

Register Name	Length	Symbol	Note
Instruction Register	3 bits	IR [0;2]	
Bypass Register	1 bits	BP	
ID Register	32 bits	ID [0;31]	
Boundary Scan Register	70 bits	BS [1;70]	

TAP Controller Instruction Set

IR2	IR1	IR0	Instruction	Operation
0	0	0	SAMPLE-Z	Tristate all data drivers and capture the pad value
0	0	1	IDCODE	
0	1	0	SAMPLE-Z	Tristate all data drivers and capture the pad value
0	1	1	BYPASS	
1	0	0	SAMPLE	
1	0	1	BYPASS	
1	1	0	BYPASS	
1	1	1	BYPASS	

Note: This Device does not perform EXTEST, INTEST or the preload portion of the PRELOAD command in IEEE 1149.1.

Boundary Scan Order

Bit #	Bump ID	Signal Name	Bit #	Bump ID	Signal Name
1	5R	V_{DD}	36	3B	NC
2	4P	SA3	37	2B	NC
3	4T	SA4	38	3A	SA11
4	6R	SA5	39	3C	SA12
5	5T	SA6	40	2C	SA13
6	7T	ZZ	41	2A	SA14
7	6P	DQa0	42	2D	DQc0
8	7P	DQa1	43	1D	DQc1
9	6N	DQa2	44	2E	DQc2
10	7N	DQa3	45	1E	DQc3
11	6M	DQa4	46	2F	DQc4
12	6L	DQa5	47	2G	DQc5
13	7L	DQa6	48	1G	DQc6
14	6K	DQa7	49	2H	DQc7
15	7K	DQa8	50	1H	DQc8
16	5L	SWEa	51	3G	SWEc
17	4L	K	52	4D	NC
18	4K	K	53	4E	SS
19	4F	V_{SS}	54	4G	NC
20	5G	SWEb	55	4H	NC
21	7H	DQb0	56	4M	SWE
22	6H	DQb1	57	3L	SWEd
23	7G	DQb2	58	1K	DQd0
24	6G	DQb3	59	2K	DQd1
25	6F	DQb4	60	1L	DQd2
26	7E	DQb5	61	2L	DQd3
27	6E	DQb6	62	2M	DQd4
28	7D	DQb7	63	1N	DQd5
29	6D	DQb8	64	2N	DQd6
30	6A	SA7	65	1P	DQd7
31	6C	SA8	66	2P	DQd8
32	5C	SA9	67	3T	SA0
33	5A	SA10	68	2R	SA1
34	6B	NC	69	4N	SA2
35	5B	NC	70	3R	V_{SS}

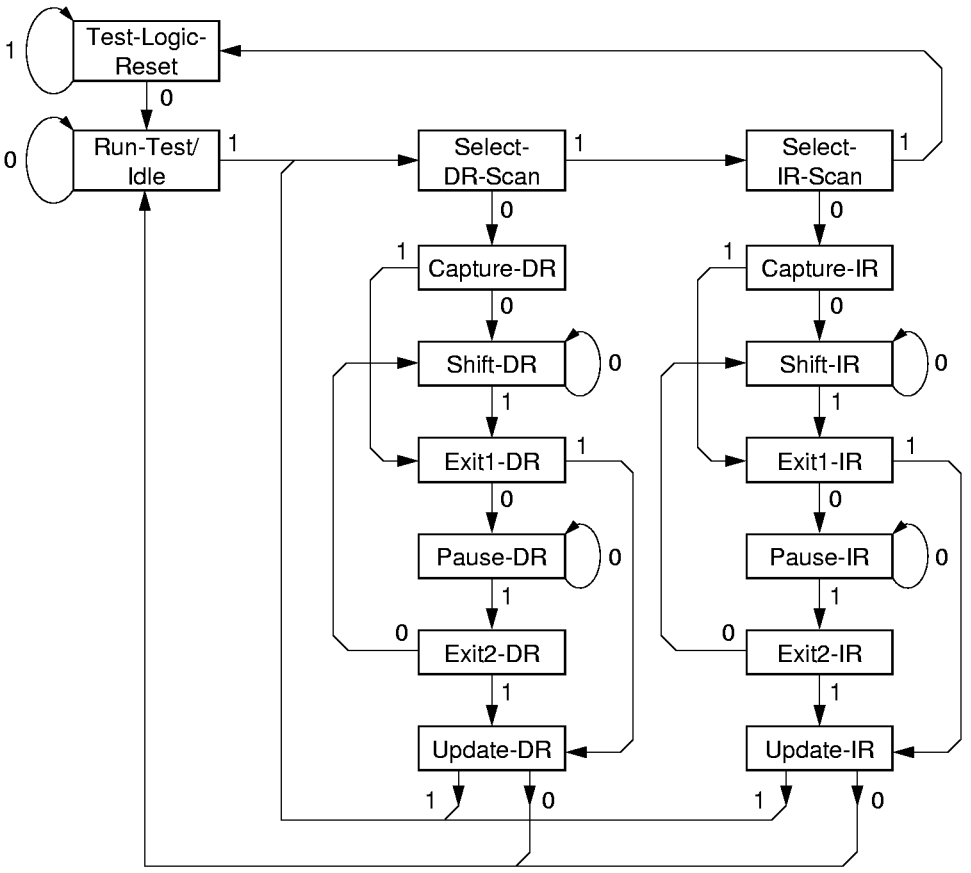
Notes: 1. NC registers are internally connected to V_{SS}.

2. The clock pins (K and $\overline{K}$) are needed as PECL differential levels. And, clock reciever generates single – end clock signal. This signal and its inverted signal are used for Boundary Scan Register input signal.

ID register

Bit#	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	X	X	X	X	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
	Vendor Revision No.				4M, 16M Depth		Depth			4M, 16M Width		Width			Use in the future						Vendor ID No.											Fix

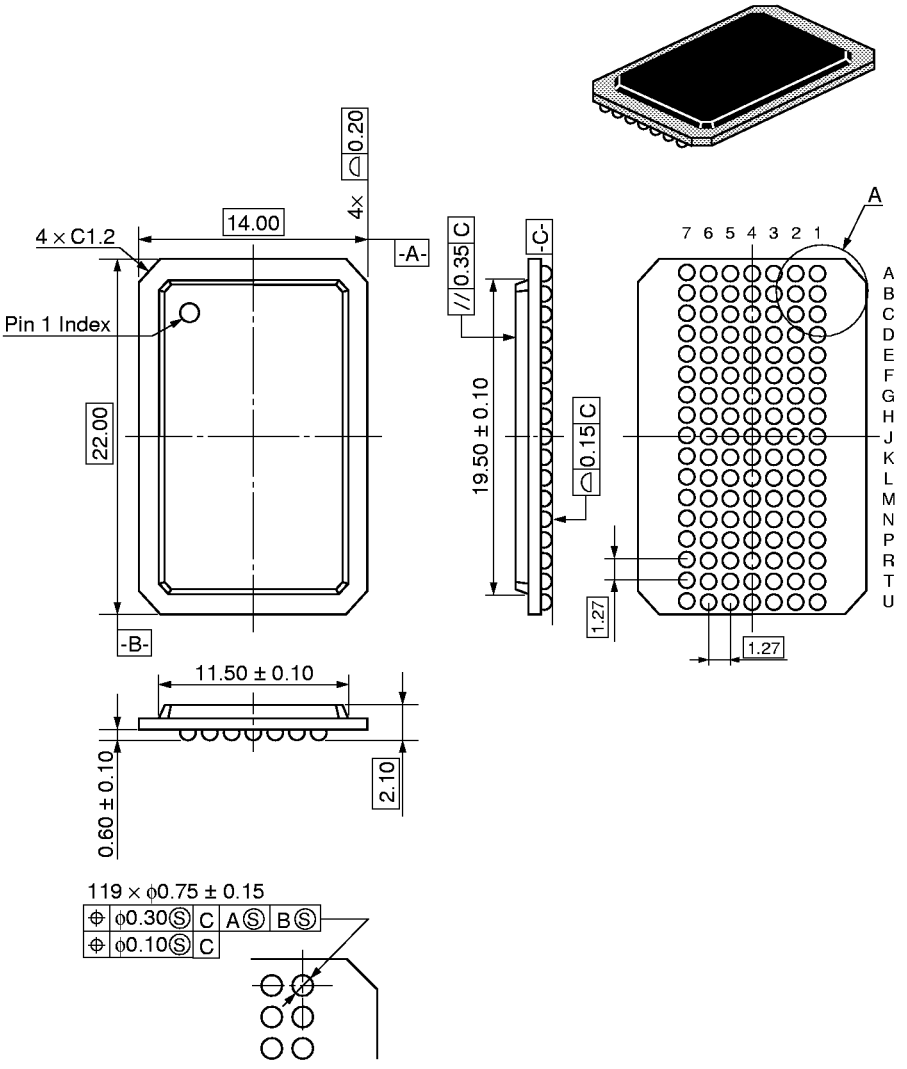
TAP Controller State Diagram



Note: The value adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.
No matter what the original state of the controller, it will enter Test-Logic-Reset when TMS is held high for at least five rising edges of TCK.

Package Outline

Unit : mm



Details of the part A

Hitachi Code	BP-119
JEDEC Code	MO-163
EIAJ Code	—
Weight	1.0 g

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