

4M x 32 SODIMM Module

Features

- 72-Pin Small Outline Dual-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	RAS Access Time	60ns	70ns
t_{CAC}	CAS Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	104ns	124ns
t_{HPC}	EDO Mode Cycle Time	25ns	30ns

- High Performance CMOS process
- Manufactured with 16Mb DRAMS (4M x 4)
- Single 3.3V $\pm$ 0.3V or 5.0V $\pm$ 0.5V Power Supply
- Optimized for use in byte-write non-parity appli-

cations.

- Low active current consumption
- All inputs & outputs are LVTTTL(3.3V) or TTL(5V) compatible
- Extended Data Out (EDO) access cycle
- Refresh Modes: RAS-Only, CBR, Hidden Refresh and Self Refresh
- 4096 refresh cycles distributed across 128ms
- 11/11 Addressing (Row/Column)
- Au contacts

Description

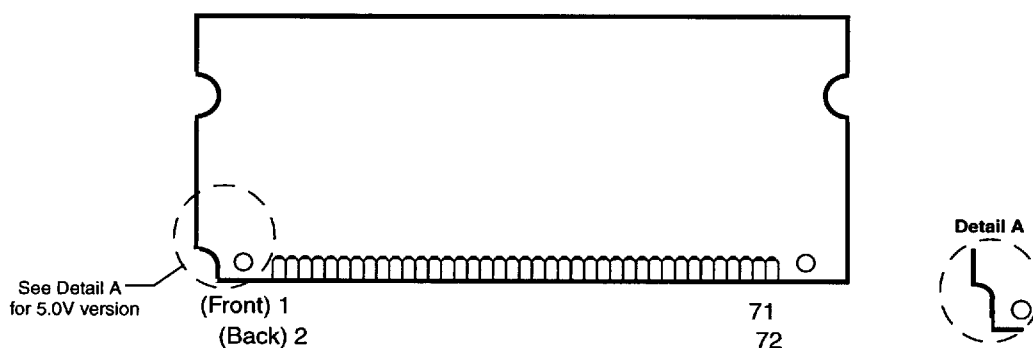
The IBM11S4325BP/M are 4MB industry standard 72-pin 4-byte small outline dual in-line memory modules (SODIMMs). The module is organized as a 4Mx32 high speed memory array that is intended for use in 16, 32 and 64 bit applications. It is manufactured with eight 4Mx4 TSOP devices, each in a 300mil package.

The use of EDO DRAMs allows for a reduction in Page Mode cycletime from 40ns (Fast Page) to 25ns (EDO, 60ns sort). The use of TSOP packages allows tight DIMM spacing (.3" on center).

This assembly is intended for use in space constrained and/or low power applications.

The IBM 72-Pin SODIMMs provide a high performance, flexible 4-byte interface in a 2.35" long footprint.

Card Outline 3.3V



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Pin Description

$\overline{\text{RAS0}}, \overline{\text{RAS2}}$	Row Address Strobe
$\overline{\text{CAS0}} - \overline{\text{CAS3}}$	Column Address Strobe
$\overline{\text{WE}}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+3.3V or +5.0V)
V_{SS}	Ground
NC	No Connect
PD1 - PD7	Presence Detects

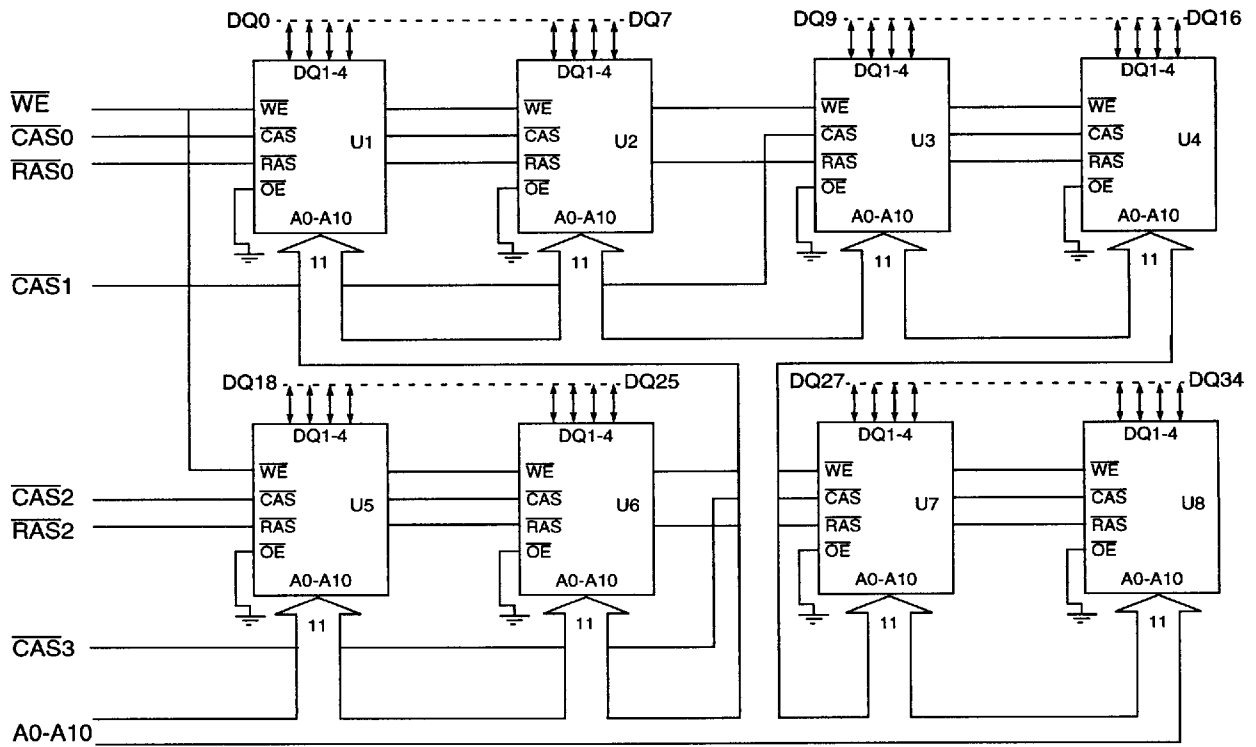
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ18	49	DQ20	61	V_{CC}
2	DQ0	14	A2	26	DQ14	38	DQ19	50	DQ21	62	DQ32
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ22	63	DQ33
4	DQ2	16	A4	28	A7	40	$\overline{\text{CAS0}}$	52	DQ23	64	DQ34
5	DQ3	17	A5	29	NC	41	$\overline{\text{CAS2}}$	53	DQ24	65	NC
6	DQ4	18	A6	30	V_{CC}	42	$\overline{\text{CAS3}}$	54	DQ25	66	PD2
7	DQ5	19	NC	31	A8	43	$\overline{\text{CAS1}}$	55	NC	67	PD3
8	DQ6	20	NC	32	A9	44	$\overline{\text{RAS0}}$	56	DQ27	68	PD4
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ28	69	PD5
10	V_{CC}	22	DQ10	34	$\overline{\text{RAS2}}$	46	NC	58	DQ29	70	PD6
11	PD1	23	DQ11	35	DQ16	47	$\overline{\text{WE}}$	59	DQ31	71	PD7
12	A0	24	DQ12	36	NC	48	NC	60	DQ30	72	V_{SS}

Ordering Information

Part Number	Organization	Speed	Dimensions	Power	DRAM Die Revision	Notes
IBM11S4325BPB-60	4M x 32	60ns	2.35" x 1" x .1496"	3.3V	D	
IBM11S4325BPB-70	4M x 32	70ns	2.35" x 1" x .1496"	3.3V	D	
IBM11S4325BMB-60	4M x 32	60ns	2.35" x 1" x .1496"	5.0V	D	
IBM11S4325BMB-70	4M x 32	70ns	2.35" x 1" x .1496"	5.0V	D	

Block Diagram



Truth Table

Function		$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	Row Address	Column Address	All DQ bits
Standby		H	H→X	X	X	X	High Impedance
Read		L	L	H	Row	Col	Valid Data Out
Early-Write		L	L	L	Row	Col	Valid Data In
EDO Mode - Read: 1st Cycle		L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles		L	H→L	H	N/A	Col	Valid Data Out
EDO Mode - Write: 1st Cycle		L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles		L	H→L	H→L	N/A	Col	Valid Data In
$\overline{\text{RAS}}$ -Only Refresh		L	H	X	Row	N/A	High Impedance
$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh		H→L	L	H	X	N/A	High Impedance
Hidden Refresh	Read	L→H→L	L	H	Row	Col	Data Out
	Write	L→H→L	L	L	Row	Col	Data In
Self Refresh		H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	NC	NC
PD2	V _{SS}	V _{SS}
PD3	V _{SS}	V _{SS}
PD4	NC	NC
PD5	NC	V _{SS}
PD6	NC	NC
PD7	V _{SS}	V _{SS}
1. NC= OPEN, V _{SS} = GND		

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units	Notes
		3.3 Volt	5.0 Volt		
V_{CC}	Power Supply Voltage	-0.5 to + 4.6	-1.0 to + 7.0	V	1
V_{IN}	Input Voltage	-0.5 to min ($V_{CC} + 0.5$, 4.6)	-0.5 to min ($V_{CC} + 0.5$, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min ($V_{CC} + 0.5$, 4.6)	-0.5 to min ($V_{CC} + 0.5$, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +150	-55 to +150	°C	1
P_D	Power Dissipation	3.6	5.5	W	1
I_{OUT}	Short Circuit Output Current	50	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions ($T_A = 0$ to 70°C)

Symbol	Parameter	3.3 Volt			5.0 Volt			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
V_{CC}	Supply Voltage	3.0	3.3	3.6	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.0	—	$V_{CC} + 0.5$	2.4	—	$V_{CC} + 0.5$	V	1, 2
V_{IL}	Input Low Voltage	-0.5	—	0.8	-0.5	—	0.8	V	1, 2

1. All voltages referenced to V_{SS} .
2. V_{IH} may overshoot to $V_{CC} + 1.2\text{V}$ for pulse widths of $\leq 4.0\text{ns}$ with 3.3 Volt, or $V_{CC} + 2.0\text{V}$ for pulse widths of $\leq 4.0\text{ns}$ (or $V_{CC} + 1.0\text{V}$ for $\leq 8.0\text{ns}$) with 5.0 Volt. Additionally, V_{IL} may undershoot to -2.0V for pulse widths $\leq 4.0\text{ns}$ (or -1.0V for $\leq 8.0\text{ns}$). Pulse widths measured at 50% points with amplitude measured peak to DC reference.

Capacitance ($T_A = 0$ to $+70^{\circ}\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ or $5.0\text{V} \pm 0.5\text{V}$)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	38	pF	
C_{I2}	Input Capacitance ($\overline{\text{RAS}}0$)	24	pF	
C_{I3}	Input Capacitance ($\overline{\text{RAS}}2$)	24	pF	
C_{I4}	Input Capacitance ($\overline{\text{CAS}}$)	14	pF	
C_{I5}	Input Capacitance ($\overline{\text{WE}}$)	40	pF	
C_{VO}	Output Capacitance (DQ0-DQ34)	15	pF	

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DC Electrical Characteristics ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3$ 0.3V or 5.0 0.5V)

Symbol	Parameter		3.3 Volt		5.0 Volt		Units	Notes
			Min	Max	Min	Max		
I_{CC1}	Operating Current Average Power Supply Operating Current (RAS, CAS, Address Cycling: $t_{RC} = t_{RC \min}$)	-60	—	1000	—	1000	mA	1, 2, 3
		-70	—	880	—	880		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current (RAS = CAS $\geq V_{IH}$)		—	8	—	8	mA	
I_{CC3}	RAS Only Refresh Current Average Power Supply Current, RAS Only Mode (RAS Cycling, CAS $\geq V_{IH}$; $t_{RC} = t_{RC \min}$)	-60	—	1000	—	1000	mA	1, 3
		-70	—	880	—	880		
I_{CC4}	EDO Mode Current Average Power Supply Current, EDO Mode (RAS = V_{IL} , CAS, Address Cycling: $t_{HPC} = t_{HPC \min}$)	-60	—	920	—	920	mA	1, 2, 3
		-70	—	800	—	800		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current (RAS = CAS = $V_{CC} - 0.2V$)		—	1600	—	1600	μA	
I_{CC6}	CAS Before RAS Refresh Current Average Power Supply Current, CAS Before RAS Mode (RAS, CAS, Cycling: $t_{RC} = t_{RC \min}$)	-60	—	1000	—	1000	mA	1, 3
		-70	—	880	—	880		
I_{CC7}	Self Refresh Current Average Power Supply Current during Self Refresh CBR cycle with RAS $\geq t_{RASS}$ (min); CAS held low; WE = $V_{CC} - 0.2V$; Addresses and $D_{IN} = V_{CC} - 0.2V$ or $0.2V$.	-60	—	1600	—	2400	μA	
		-70	—	1600	—	2400		
I_{IL}	Input Leakage Current Input Leakage Current, any input ($0.0 \leq V_{IN} \leq (V_{CC} + 0.3V)$) All Other Pins Not Under Test = 0V	RAS	-40	+40	-40	+40	μA	
		CAS	-20	+20	-20	+20		
		All others	-80	+80	-80	+80		
I_{OL}	Output Leakage Current (D_{OUT} is disabled, $0.0 \leq V_{OUT} \leq V_{CC}$)		-10	+10	-10	+10	μA	
V_{OH}	Output High Level Output "H" Level Voltage ($I_{OUT} = -2.5mA$ for 3.3V, or $I_{OUT} = -5mA$ for 5.0V)		2.4	V_{CC}	2.4	V_{CC}	V	
V_{OL}	Output Low Level Output "L" Level Voltage ($I_{OUT} = +2.1mA$ for 3.3V, or $I_{OUT} = +4.2mA$ for 5.0V)		0.0	0.4	0.0	0.4	V	

1. I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1} , I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while RAS = V_{IL} . In the case of I_{CC4} , it can be changed once or less when CAS = V_{IH} .

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3V 0.3V or 5.0V 0.5V)

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{\text{RAS}}$ only refresh cycles before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles instead of 8 $\overline{\text{RAS}}$ only refresh cycles is required.
2. AC measurements assume t_T=2ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. When both $\overline{\text{CAS0}}$ & $\overline{\text{CAS1}}$ or $\overline{\text{CAS2}}$ & $\overline{\text{CAS3}}$ go low at the same time, all 16 bits of data are read/written into the device. $\overline{\text{CAS0}}$ & $\overline{\text{CAS1}}$ or $\overline{\text{CAS2}}$ & $\overline{\text{CAS3}}$ (CAS's to the same DRAM) cannot be staggered within the same read/write cycle.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t _{RC}	Random Read or Write Cycle Time	104	—	124	—	ns	
t _{RP}	$\overline{\text{RAS}}$ Precharge Time	40	—	50	—	ns	
t _{CP}	$\overline{\text{CAS}}$ Precharge Time	10	—	10	—	ns	
t _{RAS}	$\overline{\text{RAS}}$ Pulse Width	60	10K	70	10K	ns	
t _{CAS}	$\overline{\text{CAS}}$ Pulse Width	10	10K	12	10K	ns	
t _{ASR}	Row Address Setup Time	0	—	0	—	ns	
t _{RAH}	Row Address Hold Time	10	—	10	—	ns	
t _{ASC}	Column Address Setup Time	0	—	0	—	ns	
t _{CAH}	Column Address Hold Time	10	—	12	—	ns	
t _{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	14	45	14	50	ns	1
t _{RAD}	$\overline{\text{RAS}}$ to Column Address Delay Time	12	30	12	35	ns	2
t _{RSH}	$\overline{\text{RAS}}$ Hold Time	10	—	12	—	ns	
t _{CSH}	$\overline{\text{CAS}}$ Hold Time	50	—	55	—	ns	
t _{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	5	—	5	—	ns	
t _{DZC}	$\overline{\text{CAS}}$ Delay Time from D _{IN}	0	—	0	—	ns	
t _T	Transition Time (Rise and Fall)	2	30	2	30	ns	3

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. AC measurements assume t_T = 2ns.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	10	—	12	—	ns	
t_{WP}	Write Command Pulse Width	10	—	12	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	10	—	12	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	10	—	12	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	1
t_{DH}	D_{IN} Hold Time	10	—	12	—	ns	1

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	—	15	—	20	ns	4

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC} , t_{CAC} , t_{CPA} , t_{AA} .
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Extended Data Out Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
t_{HCAS}	CAS Pulse Width (EDO Mode)	10	10K	12	10K	ns	
t_{HPC}	EDO Mode Cycle Time (Read/Write)	25	—	30	—	ns	
t_{DOH}	Data-out Hold Time from $\overline{CAS}$	5	—	5	—	ns	
t_{WHZ}	Output buffer Turn-Off Delay from $\overline{WE}$	0	10	0	15	ns	
t_{WPZ}	$\overline{WE}$ Pulse Width to Output Disable at CAS High	10	—	10	—	ns	
t_{CPRH}	RAS Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1
t_{RASP}	EDO Mode RAS Pulse Width	60	125K	70	125K	ns	

1. Measured with the specified current load and 100pF at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.

Refresh Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time (CAS before RAS Refresh Cycle)	10	—	10	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time (CAS before RAS Refresh Cycle)	5	—	5	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time (CAS before RAS Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time (CAS before RAS Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	RAS Precharge to $\overline{CAS}$ Hold Time	5	—	5	—	ns	
t_{REF}	Refresh Period	—	128	—	128	ms	1

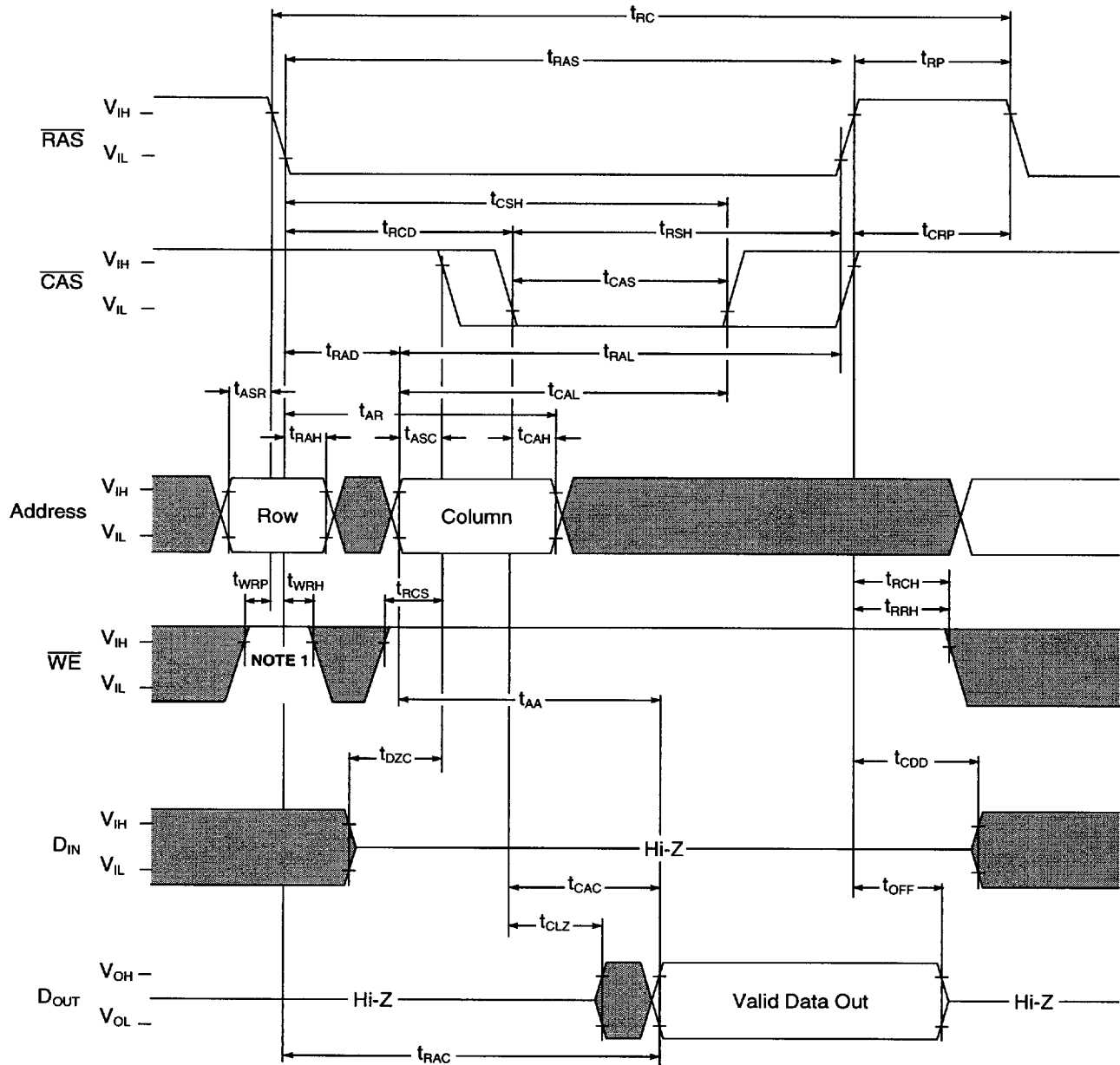
1. 40962 refreshes are required every 128ms.

Self Refresh Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RASS}	RAS Pulse Width During Self Refresh Cycle	100	—	100	—	μs	1
t_{RPS}	RAS Precharge Time During Self Refresh Cycle	104	—	124	—	ns	1
t_{CHS}	CAS Hold Time During Self Refresh Cycle	-50	—	-50	—	ns	1

1. When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation: If row addresses are being refreshed in a EVENLY DISTRIBUTED manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh. If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.

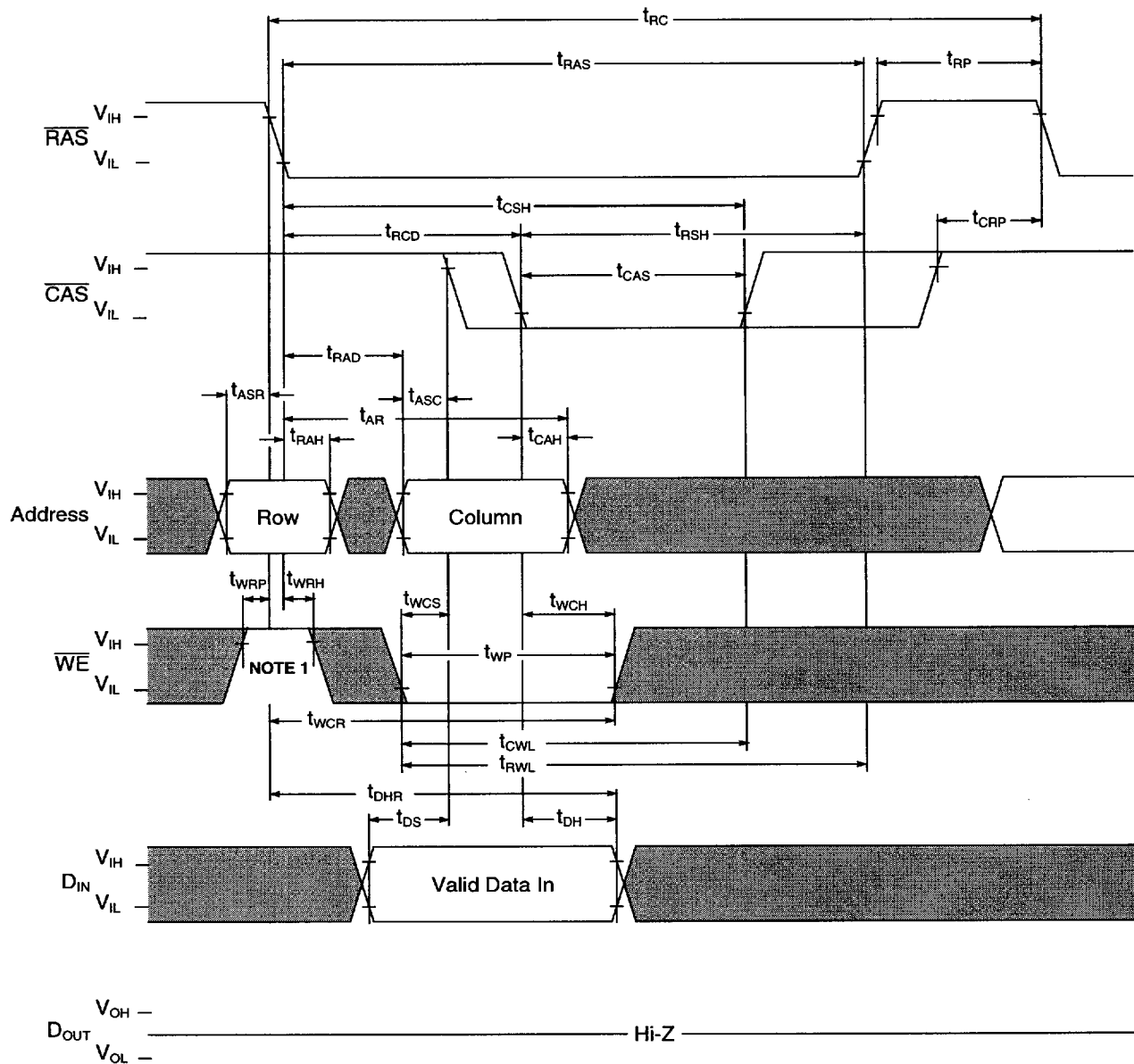
Read



■ : "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

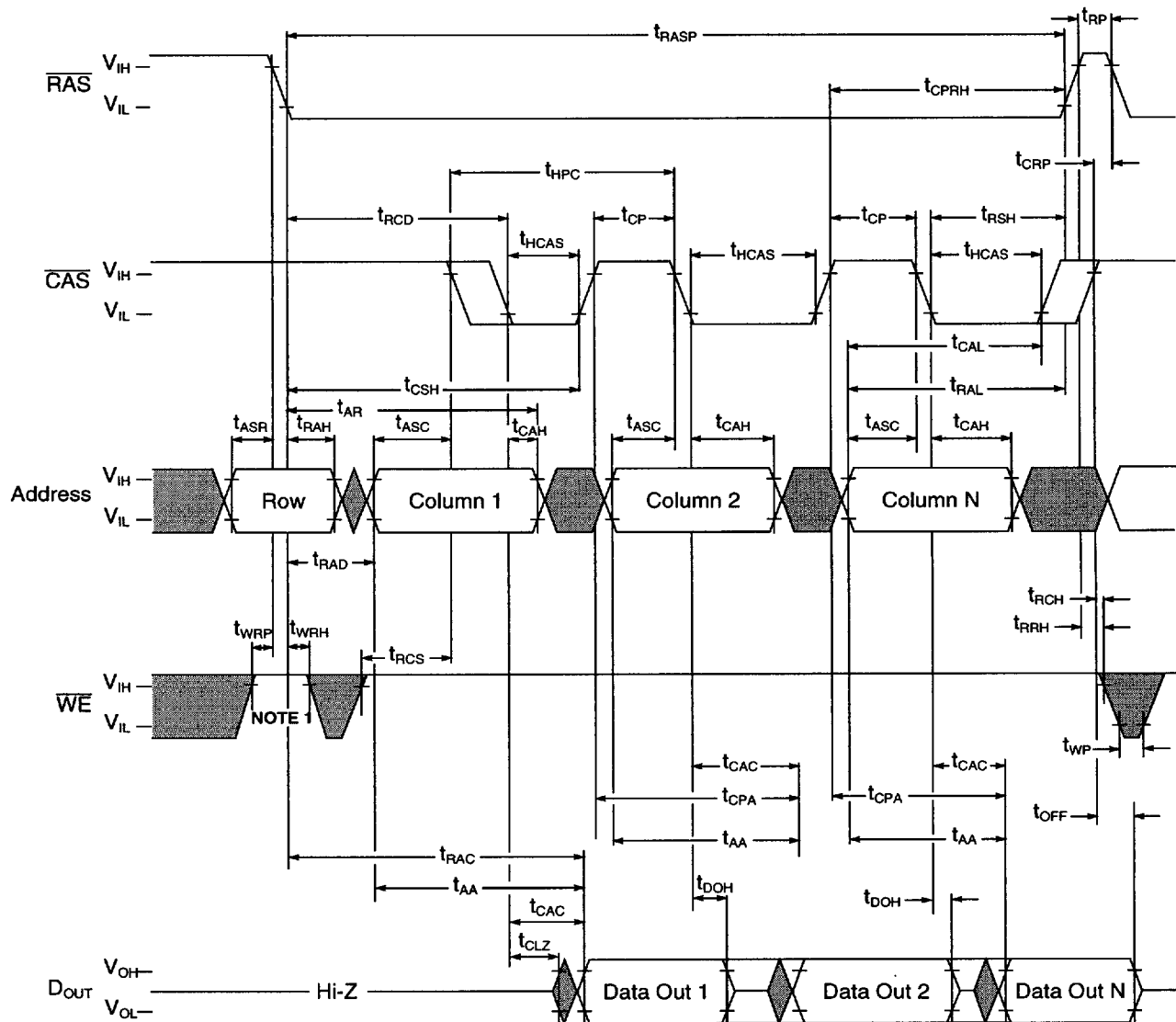
Write Cycle (Early Write)



■ : "H" or "L"

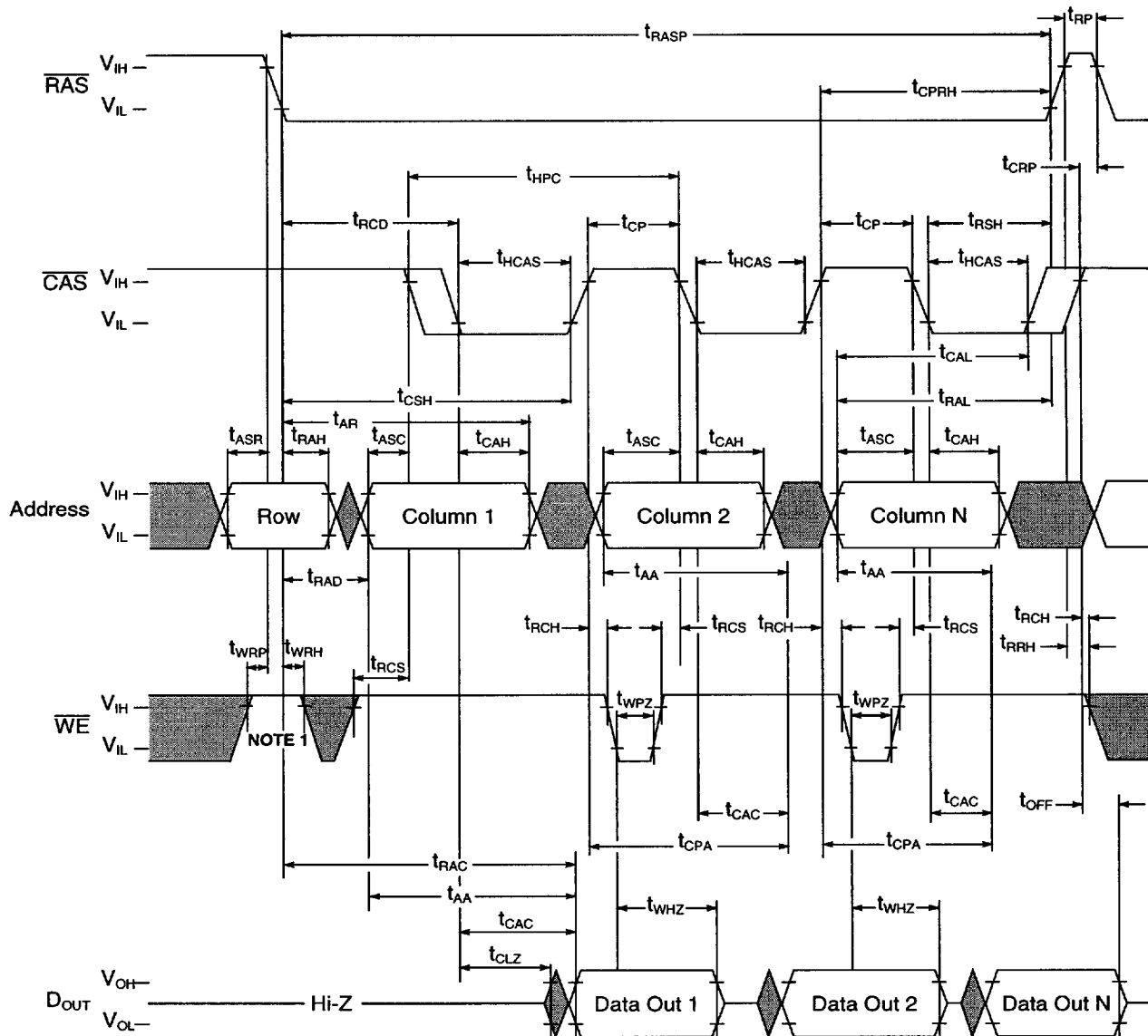
NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

Extended Data Out Mode Read Cycle



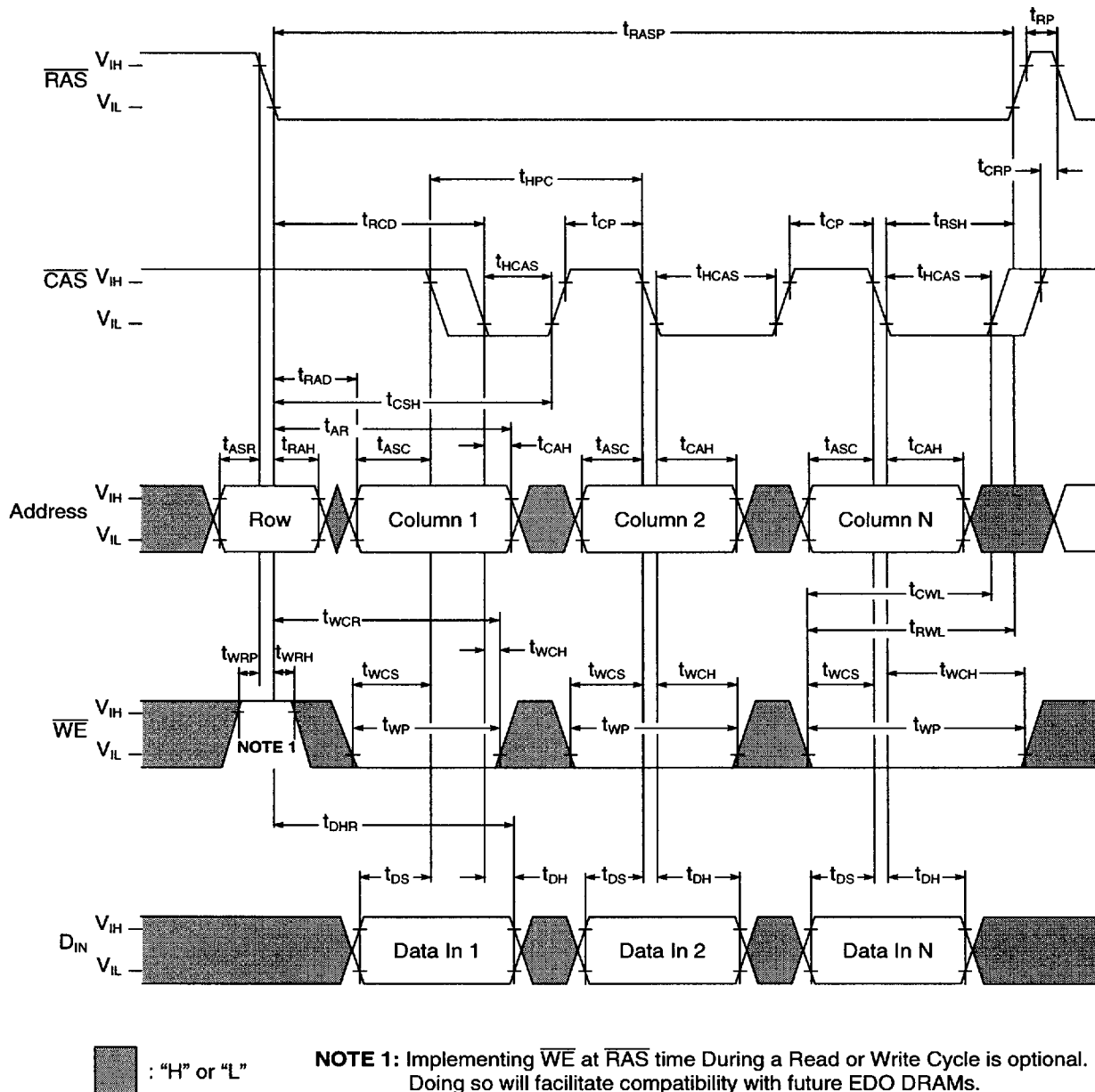
: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

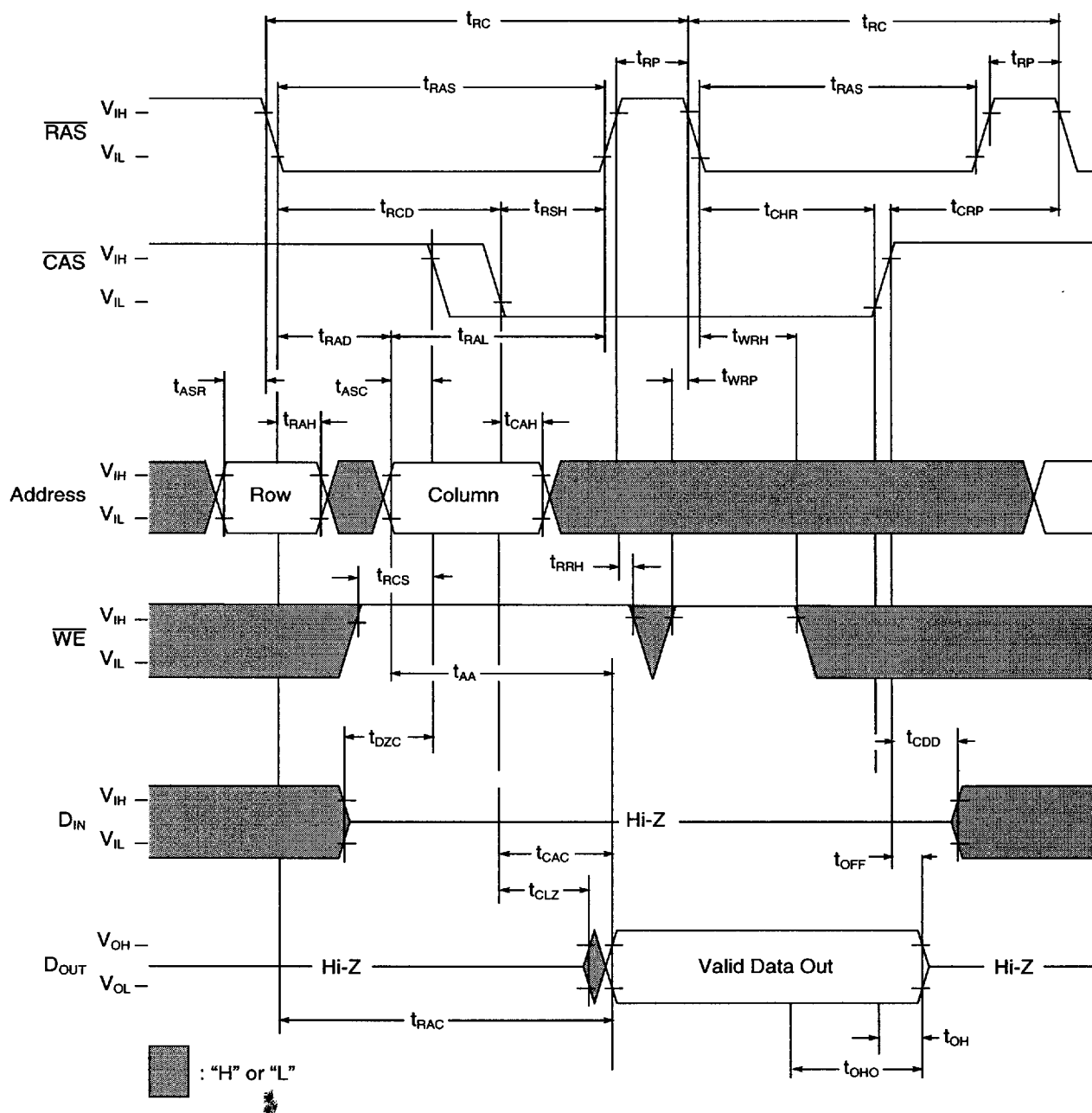


NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional
Doing so will facilitate compatibility with future EDO DRAMs.

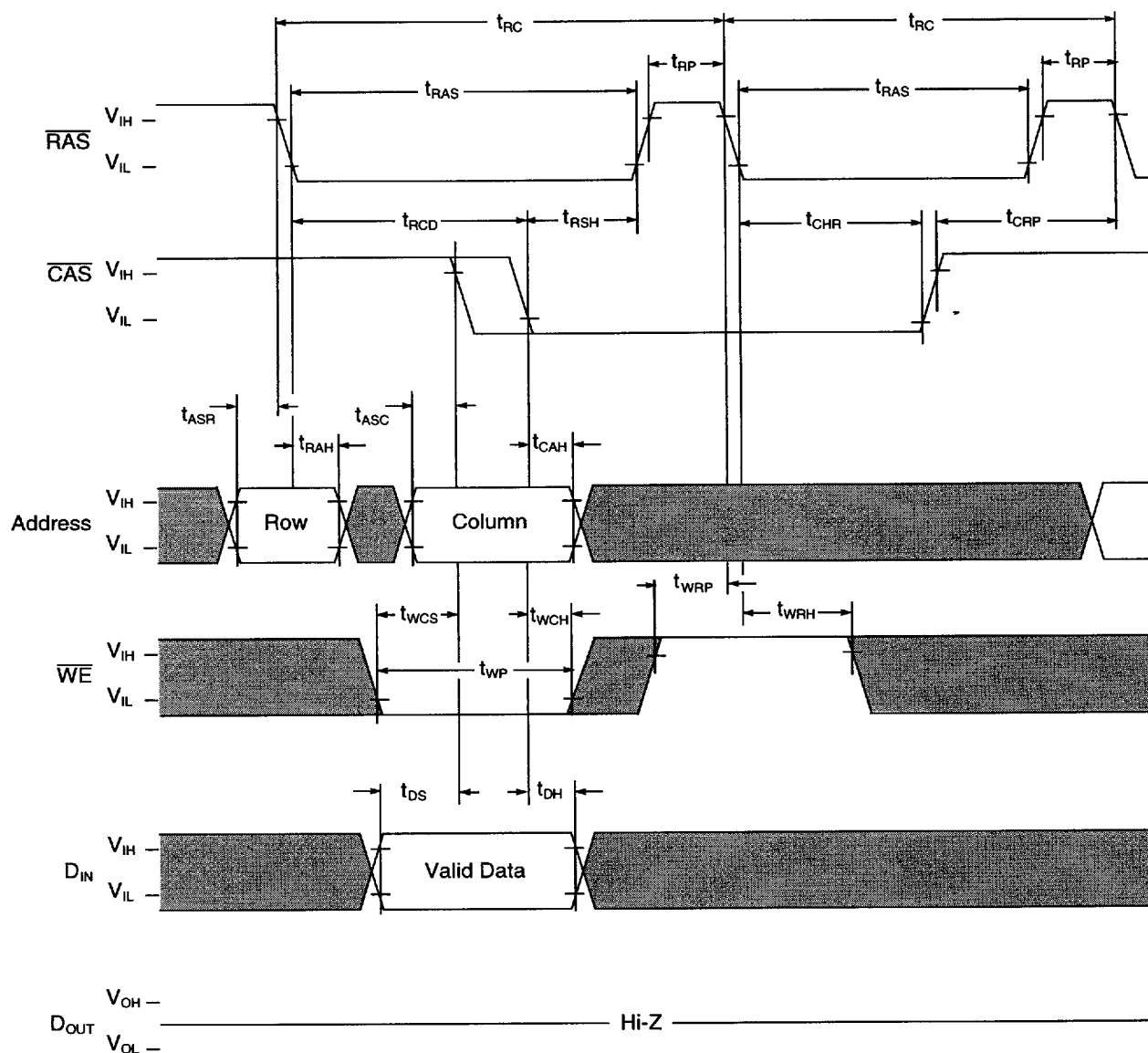
Extended Data Out Mode Write Cycle



Hidden Refresh Cycle (Read)

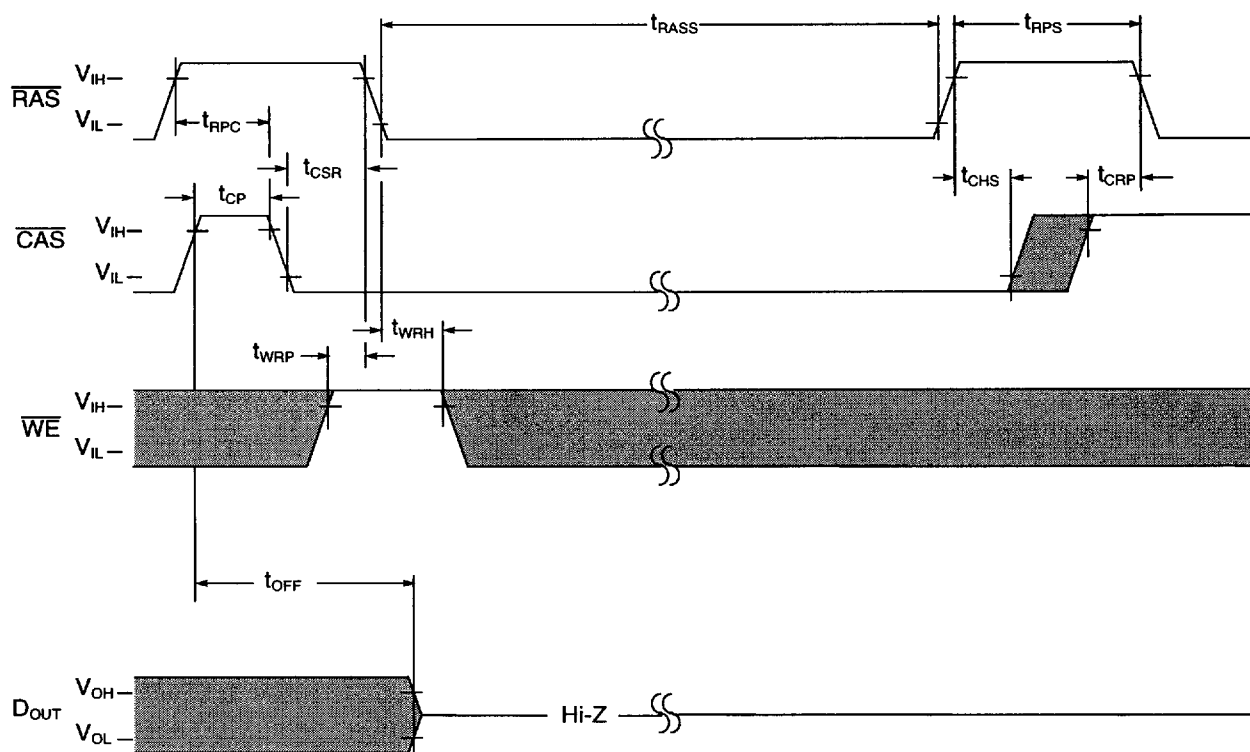


Hidden Refresh Cycle (Write)



: "H" or "L"

Self Refresh Cycle (Sleep Mode)

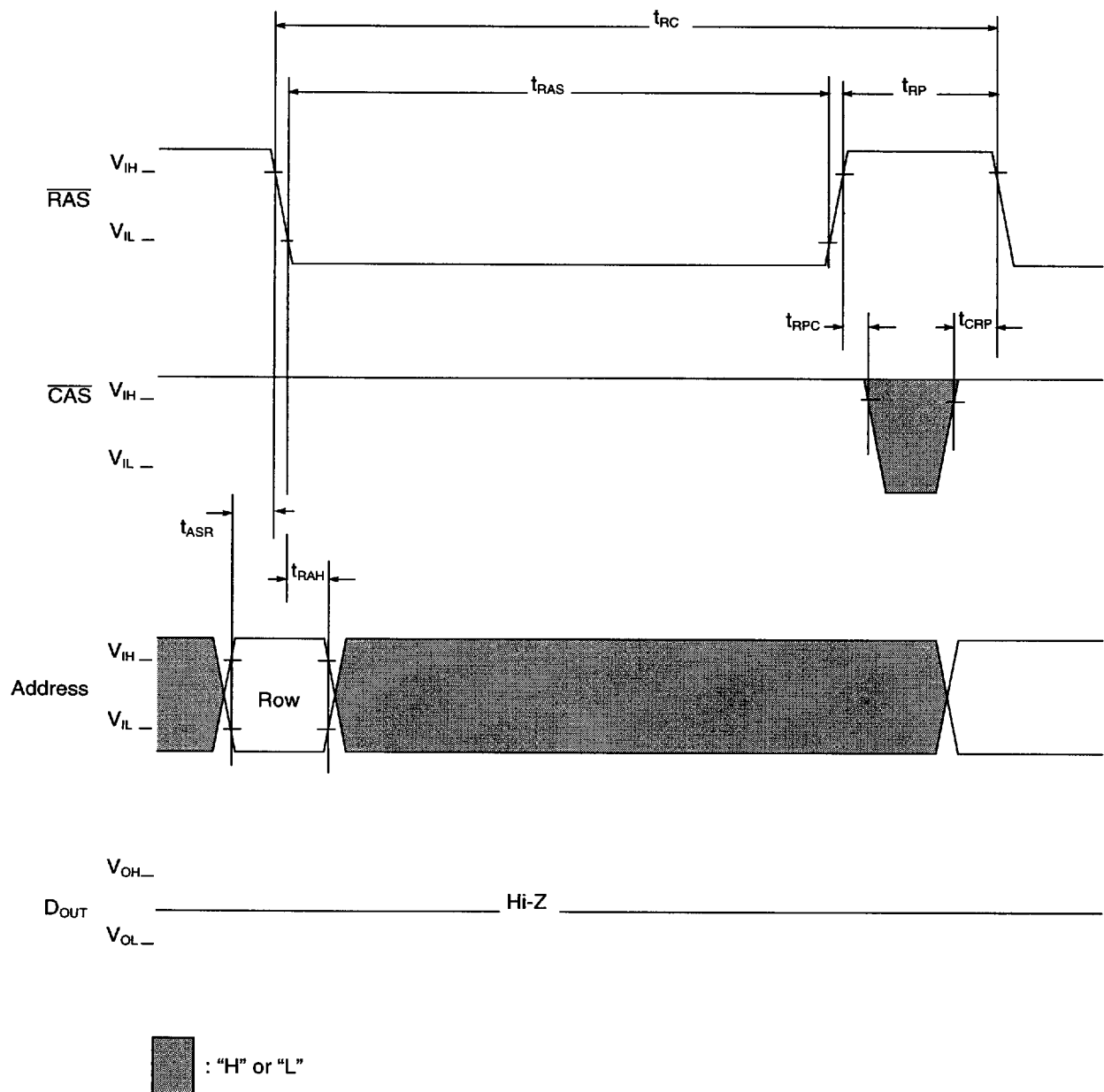


■ : "H" or "L"

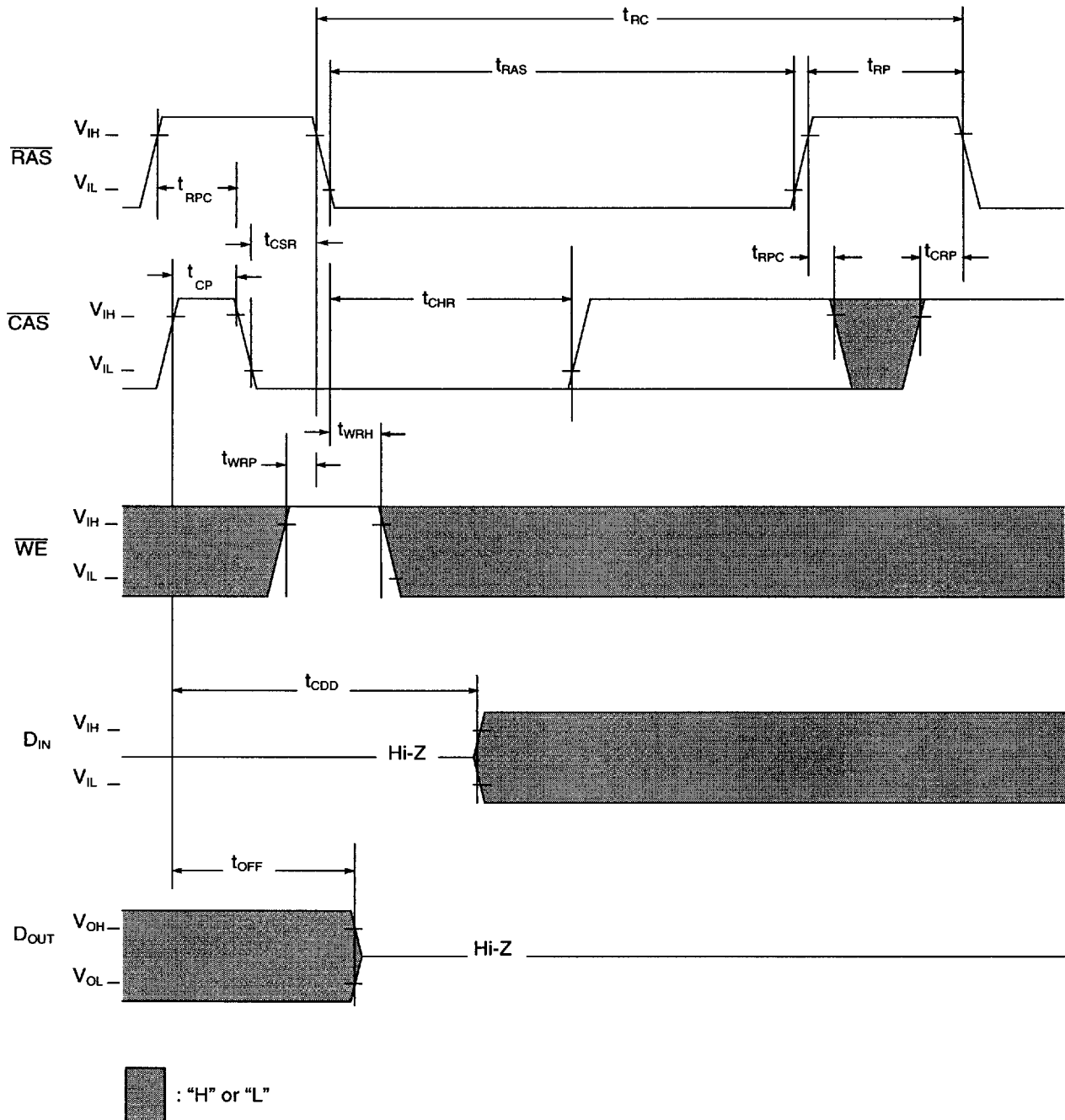
NOTE: Address is "H" or "L"

Once t_{RASS} (min) is provided and RAS remains low, the DRAM will be in Self Refresh, commonly known as "Sleep Mode."

RAS Only Refresh Cycle

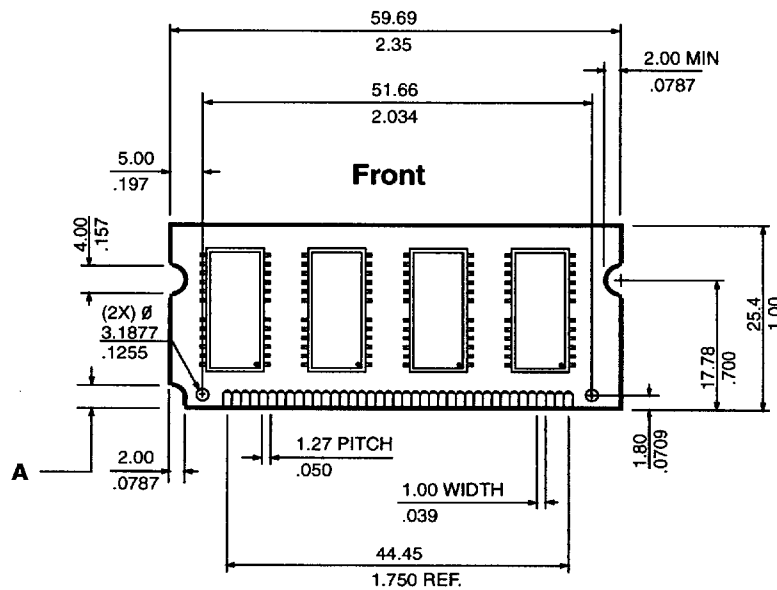


Note: $\overline{\text{WE}}$, D_{IN} are "H" or "L"

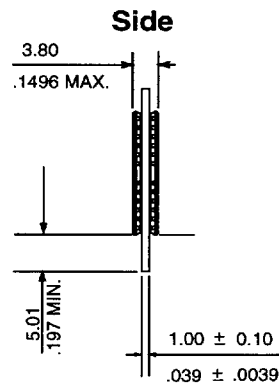
CAS Before RAS Refresh Cycle

Note: Addresses are "H" or "L"

Layout Drawing



$$\mathbf{A} = \begin{array}{c|c} 3.3\text{V} & 5.0\text{V} \\ \hline 3.175 & 6.35 \\ \hline .125 & .246 \end{array}$$



Note: All dimensions are typical unless otherwise stated.

$$\frac{\text{Millimeters}}{\text{Inches}}$$

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4M x 32 SODIMM Module

Revision Log

Rev	Contents of Modification
8/95	Initial release of 4Mx32 EDO specification using 4Mx4 with 11/11 Addressed DRAMs.