Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS 10-BIT MEMORY LATCHES

IDT54/74FBT2841A
IDT54/74FBT2841B

FEATURES:

- 25Ω output resistors reduce overshoot and undershoot when driving MOS RAMs
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Low power in all three states
- ± 10% power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

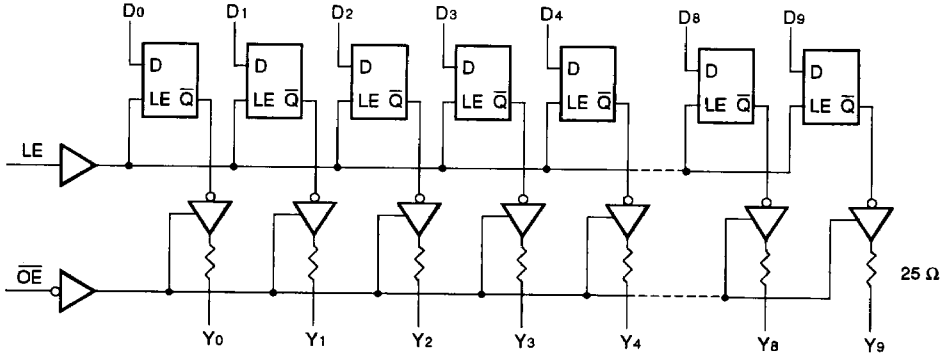
DESCRIPTION:

The FBT series of BiCMOS Memory Drivers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT2841 series are 3-state, 10-bit latches where each output is terminated with a 25Ω series resistor.

The FBT series of memory line drivers are ideal for use in designs needed to drive large capacitive loads with low static (DC) current loading. They are also designed for rail-to-rail output switching. This higher output level in the high state will result in a significant reduction in overall system power dissipation.

FUNCTIONAL BLOCK DIAGRAM



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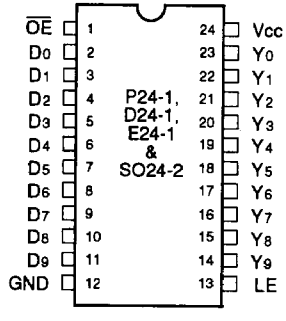
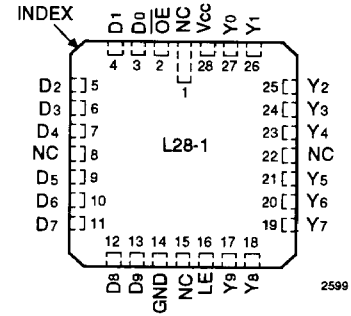
PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



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LCC
TOP VIEW

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PIN DESCRIPTION

Name	I/O	Description
$D_0 - D_9$	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
$Y_0 - Y_9$	O	The 3-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_I are in the high-impedance (off) state.

2599 tbl 05

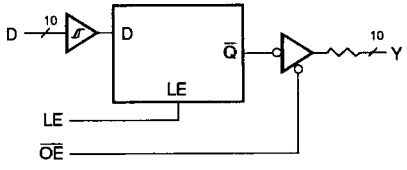
FUNCTION TABLE[1]

Inputs			Internal	Outputs	
$\overline{OE}$	LE	D_I	Q_I	Y_I	Function
H	X	X	X	Z	High Z
H	H	L	L	Z	High Z
H	H	H	H	Z	High Z
H	L	X	NC	Z	Latched (High Z)
L	H	L	L	L	Transparent
L	H	H	H	H	Transparent
L	L	X	NC	NC	Latched

NOTE: 2599 tbl 06

1. H = HIGH, L = LOW, X = Don't Care, NC = No Change, Z = High Impedance

LOGIC SYMBOL



2599 drw 03

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Military	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}[3]	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2599 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
2. Inputs and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2599 tbl 02

1. This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V		—	—	–10	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_O = 2.7V	—	—	50	µA
I_{OZL}	Output Current		V_O = 0.5V	—	—	–50	
I_I	Input HIGH Current	V_{CC} = Max., V_{CC} (Max.)		—	—	100	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		–35	—	—	mA
I_{ODL}	Output Drive Current	V_{CC} = Min., V_O = 2.25V		50	—	—	mA
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–75	—	–225	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –300µA[4]	V_{HC}	V_{CC}	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –1mA	2.7	3.8	—	
			I_{OH} = –8mA	2.4	3.3	—	
			I_{OH} = –12mA	2.0	3.2	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 300µA[4]	—	GND	V_{LC}	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 1mA	—	0.1	0.5	
			I_{OL} = 12mA	—	0.35	0.8	
V_H	Input Hysteresis	—		—	200	—	mV
I_{CCH} I_{CCZ} I_{CCL}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.2	1.5	mA

2599 tbl 03

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This condition is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND One Input Toggling LE = V_{CC} 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.3	0.4	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_i = 10MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.2	5.5	mA
		$\overline{OE}$ = GND, LE = V_{CC} One Bit Toggling	V_{IN} = 3.4V V_{IN} = GND	—	3.5	6.5	
		V_{CC} = Max., Outputs Open f_i = 2.5MHz, 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	7.7	11.5[5]	
		$\overline{OE}$ = GND, LE = V_{CC} Ten Bits Toggling	V_{IN} = 3.4V V_{IN} = GND	—	10.2	21.5[5]	

NOTES:
2599 tbl 04

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			54/74FBT2841A				54/74FBT2841B				
			Com'l.		Mil.		Com'l.		Mil.		
Symbol	Parameter	Condition[1]	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay D_i to Y_i (LE = HIGH)	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	10.0	1.5	6.5	1.5	7.5	ns
t_{SU}	Data to LE Set-up Time		2.5	—	2.5	—	2.5	—	2.5	—	ns
t_H	Data to LE Hold Time		2.5	—	3.0	—	2.5	—	2.5	—	ns
t_{PLH} t_{PHL}	Propagation Delay LE to Y_i		1.5	12.0	1.5	13.0	1.5	8.0	1.5	10.5	ns
t_W	LE Pulse Width[3] HIGH		4.0	—	5.0	—	4.0	—	4.0	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_i		1.5	11.5	1.5	13.0	1.5	8.0	1.5	8.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Y_i		1.5	8.0	1.5	10.0	1.5	7.0	1.5	7.5	ns

NOTES:
2599 tbl 07

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. These parameters are guaranteed, but not tested.