P33PCT374A/B
OCTAL D FLIP-FLOPS WITH 3-STATE OUTPUTS

ADVANCE INFORMATION

T-46-07-11

FEATURES

- 3.3V ± 0.2V Power Supply
- Center Power and Ground Pins
- Function, Speed and Drive Compatible with the Fastest Bipolar Logic
- "A" and "B" Versions for High Performance
- CMOS for Low Power Consumption
- Edge Triggered D Type Inputs
- 250 MHz Typical Toggle Rate
- Buffered Positive Edge Triggered Clock
- Inputs and Outputs Interface with TTL Logic Levels
- Input Clamp Diode to Limit Bus Reflections
- Low Ground Bounce

DESCRIPTION

The P33PCT374A/B are high-speed low power octal D-type flip-flops featuring separate D-type inputs for each flip-flop. Both devices have 3-state outputs for bus oriented applications. A buffered clock (CP) and output enable ($\overline{OE}$) are common to all flip-flops. The eight flip-flops contained in the 'PCT374A/B will store the state of their individual D inputs that meet the setup and hold time requirements on the low-to-high clock (CP) transition. When $\overline{OE}$ is LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs will be in the high impedance state. The state of output enable does not affect the state of the flip-flops.

The P33PCT374A/B is manufactured with PACE III Technology™ which is Performance Advanced CMOS Engineered with two-level metal and epitaxial substrates to use 0.4 micron effective channel lengths giving 250 picosecond loaded* internal gate delays. The nominal supply voltage is reduced from the conventional 5.0V to 3.3V, thus reducing output swings dramatically. This, together with the (lower inductance) center power and ground pins, and the extra power and extra ground pins, significantly reduces noise and ground bounce that would otherwise occur for very high speed circuitry.

The P33PCT374A/B is available in 24-pin 300 mil DIP and SOIC, providing excellent board level densities.

*For a fan-in/fan-out of 4 at 85°C junction temperature and 3.3V supply.

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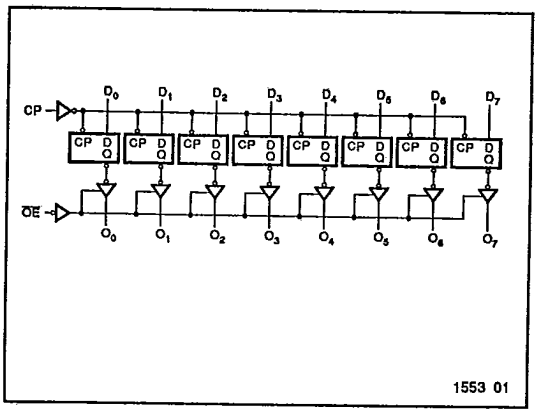
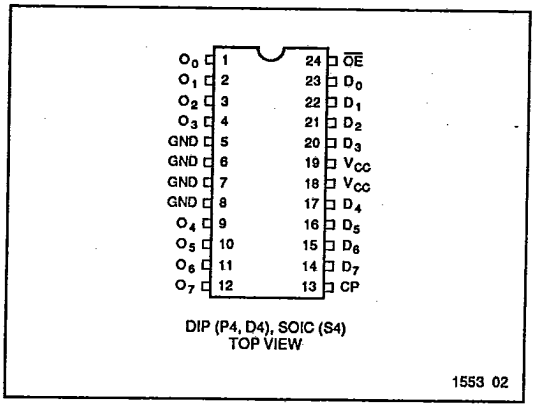
LOGIC DIAGRAM P33PCT374A/B



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–55 to +125	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +5.0	V
I_{IN}	Input Current	–30 to +5.0	mA

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Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	100	mA
V_{IN}	Input Voltage	–0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	–0.5 to V_{CC} + 0.5	V

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Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Commercial	0°C	+70°C

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Supply Voltage (V_{CC})	Min	Max
Commercial	+3.1V	+3.5V

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0		V_{CC} + 0.5	V		
V_{IL}	Input LOW Voltage		–0.5		0.8	V		
V_H	Hysteresis[4]			.35		V		All inputs
V_{CD}	Input Clamp Diode Voltage				–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V	V_{CC} – 0.2			V		I_{OH} = –32µA
		Commercial (CMOS)	V_{CC} – 0.2			V	MIN	I_{OH} = –300µA
		Commercial (TTL)	2.7			V	MIN	I_{OH} = –15mA
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V			0.2	V		I_{OL} = 300µA
		Commercial (CMOS)			0.2	V	MIN	I_{OL} = 300µA
		Commercial (TTL)			0.5	V	MIN	I_{OL} = 48mA
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current				–5	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3]				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current[3]				–5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Voltage Applied				10	µA	MAX	V_{OUT} = V_{CC}
I_{OZL}	Off State I_{OUT} LOW-Level Voltage Applied				–10	µA	MAX	V_{OUT} = GND
I_{OZH}	Off State I_{OUT} HIGH-Level Voltage Applied[3]				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Voltage Applied[3]				–10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60			mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All Inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs

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Notes:

1. Typical limits are at V_{cc} = 3.3V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.
4. Only for clock input.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
I_{CCQT}	Quiescent Power Supply Current (TTL Inputs)		2.0	mA	V_{CC} = MAX, $V_{IN} = V_{CC} - 0.3V$[2], f = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]		0.25	mA/ mHz	V_{CC} = MAX, One Bit Toggling, 50% Duty Cycle, $\overline{OE}$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$, Outputs Open
I_{CC}	Total Power Supply Current[5]		4.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OE}$ = GND and $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
			6.0	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 5MHz, $\overline{OE}$ = GND and $V_{IN} = V_{CC} - 0.3V$[2], or V_{IN} = GND
			7.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND and $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
			16.8[4]	mA	V_{CC} = MAX, f_0 = 10MHz, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND and $V_{IN} = V_{CC} - 0.3V$[2] or V_{IN} = GND

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Notes:
1. Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
2. Per TTL driven input ($V_{IN} = V_{CC} - 0.3V$); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_{CC} = I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQT} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$

I_{CCQT} = Power Supply Current for a TTL High Input ($V_{IN} = V_{CC} - 0.3V$)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_1 = Input Frequency
N_1 = Number of Inputs at f_1
All currents are in milliamps and all frequencies are in megahertz.

TRUTH TABLE

Inputs			Outputs
D_n	CP	$\overline{OE}$	O_n
H	⌐	L	H
L	⌐	L	L
X	X	H	Z

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H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
⌐ = LOW-to-HIGH clock transition
Z = HIGH Impedance

AC CHARACTERISTICS

Symbol	Parameter	P33PCT374A			P33PCT374B			Units	Fig. No.
		T_A = +25°C V_{CC} = +3.3V	COM'L		T_A = +25°C V_{CC} = +3.3V	COM'L			
		Typ.	Min.[1]	Max.	Typ.	Min.[1]	Max.		
t_{PLH} t_{PHL}	Propagation Delay Clock to Output	4.5	1.5	6.5	3.4	1.5	4.9	ns	1 5
t_{PZH} t_{PZL}	Output Enable Time	5.5	1.5	6.5	4.1	1.5	4.9	ns	1 7 8
t_{PHZ} t_{PLZ}	Output Disable Time	4.0	1.5	5.5	3.0	1.5	4.1		

Note: AC Characteristics guaranteed with C_L = 50pF as shown in Figure 1.

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AC OPERATING REQUIREMENTS

Symbol	Parameter	P33PCT374A			P33PCT374B			Units	Fig. No.
		T_A = +25°C V_{CC} = +3.3V	COM'L		T_A = +25°C V_{CC} = +3.3V	COM'L			
		Typ.	Min.[1]	Max.	Typ.	Min.[1]	Max.		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to CP	0.8	2.0		0.8	1.5		ns	4
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to CP	0.6	1.0		0.6	0.8		ns	4
$t_w(H)$ $t_w(L)$	Clock Pulse Width[2], HIGH or LOW	2.0	6.0		2.0	4.5		ns	5

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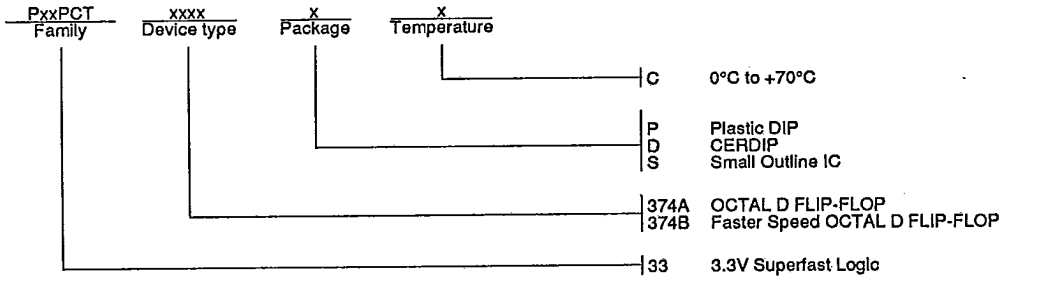
Notes:
1. Minimum limits are guaranteed but not tested on Propagation Delays.
2. With one data channel toggling, $t_w(L) = t_w(H) = 2.0$ns and $t_r = t_f = 1.0$ns.

ORDERING INFORMATION



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