![SGS-THOMSON MICROELECTRONICS logo] SGS-THOMSON MICROELECTRONICS
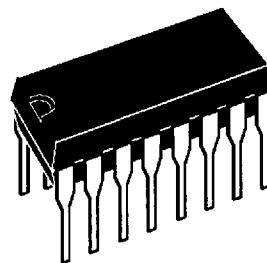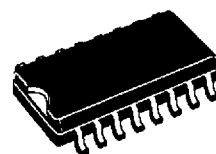
ST6203B

8-BIT HCMOS MCU

- 3.0 to 6.0V Supply Operating Range
- 8 MHz Maximum Clock Frequency
- -40 to +85°C Operating Temperature Range
- Run, Wait and Stop Modes
- 4 Interrupt Vectors
- Look-up Table capability in ROM
- Data ROM: User selectable size (in program ROM)
- Data RAM: 64 bytes
- ROM read-out Protection
- 9 I/O pins, fully programmable as:
  - Input with pull-up resistor
  - Input without pull-up resistor
  - Input with interrupt generation
  - Open-drain or push-pull output
- 3 I/O lines can sink up to 20mA to drive LEDs or TRIACs directly
- 8-bit Timer/Counter with 7-bit programmable prescaler
- Digital Watchdog
- Oscillator Safe Guard
- On-chip Clock oscillator can be driven by Quartz crystal, Ceramic resonator or RC network
- Power-on Reset
- One external Non-Maskable Interrupt
- ST626x-EMU2 Emulation and Development System (connects to an MS-DOS PC via a parallel port).

PDIP16

PSO16

(See end of Datasheet for Ordering Information)

DEVICE SUMMARY

DEVICE	ROM (Bytes)	I/O Pins
ST6203B	1036	9

1 GENERAL DESCRIPTION

1.1 INTRODUCTION

The ST6203B microcontroller is a member of the 8-bit HCMOS ST62xx family of devices, which is targeted at low to medium complexity applications. All ST62xx devices are based on a building block approach: a common core is surrounded by a number of on-chip peripherals.

The ST6203B features the following peripherals: a Timer comprising an 8-bit counter equipped with a 7-bit software programmable prescaler and a Digital Watchdog timer.

The ST6203B features a choice of Quartz, Ceramic or RC oscillators, an Oscillator Safe Guard cir-

cuit, Read-out Protection against unauthorised copying of program code, and an External STOP Mode Control option to enlarge the range of power consumption versus reliability trade-offs.

These devices are well suited for automotive, appliance and industrial applications. The user programmable part for program development is the ST62E01, which is a pin compatible device with 2Kbytes of EPROM. Care must be taken to only use the memory available on the ST6203B when using the ST62E20 for evaluation or development.

Figure 3. Block Diagram
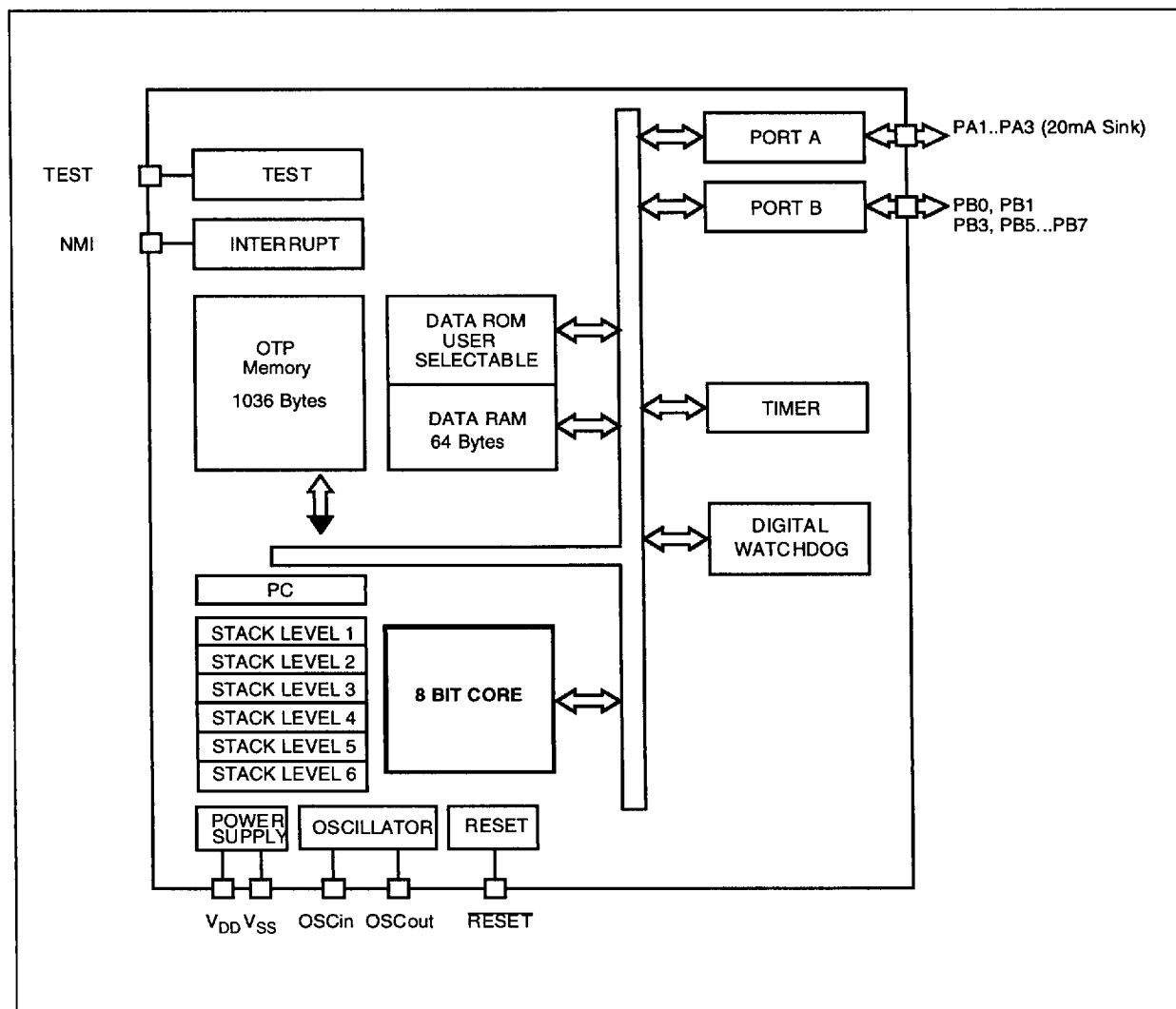
1.2 PIN DESCRIPTION

V_{DD} and V_{SS}. Power is supplied to the MCU via these two pins. V_{DD} is the power connection and V_{SS} is the ground connection.

OSCin and OSCout. These pins are internally connected to the on-chip oscillator circuit. When the QUARTZ/CERAMIC RESONATOR Mask Option is selected, a quartz crystal, a ceramic resonator or an external clock signal can be connected between these two pins. When the RC OSCILLATOR Mask Option is selected, a resistor must be connected between the OSCout pin and ground. The OSCin pin is the input pin, the OSCout pin is the output pin.

**RESET.** The active-low RESET pin is used to restart the microcontroller.

TEST. The TEST pin must be held at V_{SS} for normal operation (an internal 100KΩ pull-down resistor selects normal operating mode if the TEST pin is not connected externally).

NMI. The NMI pin provides the capability for asynchronous interruption, by applying an external non maskable interrupt to the MCU. The NMI is falling edge sensitive. A ROM mask option makes available an on-chip pull-up on the NMI pin.

PA1-PA3. These 3 lines are organized as one I/O port (A). Each line may be configured under software control as inputs with or without internal pull-up resistors, interrupt generating inputs with pull-up resistors, open-drain or push-pull outputs. **PA1-PA3** can also sink 20mA for direct LED driving.

PB0, PB1, PB3, PB5-PB7. These 6 lines are organized as one I/O port (B). Each line may be configured under software control as inputs with or without internal pull-up resistors, interrupt generating inputs with pull-up resistors, open-drain or push-pull outputs.

Figure 4. ST6203B Pin Configuration
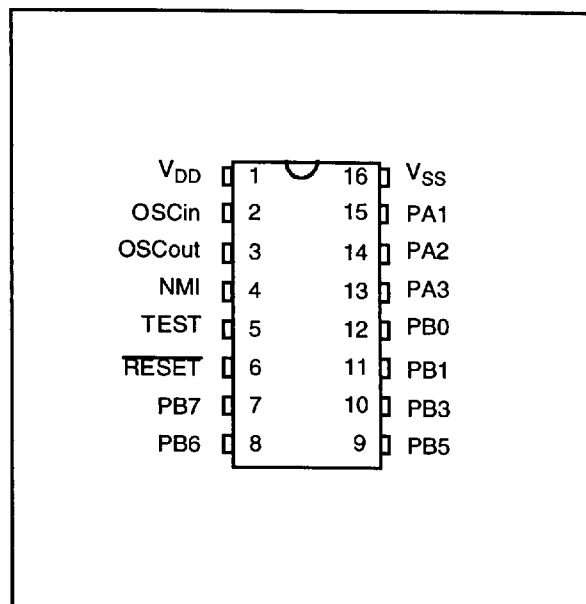
1.3 MEMORY MAP

1.3.1 Introduction

The MCU operates in three separate memory spaces: Program space, Data space, and Stack space. Operation in these three memory spaces is described in the following paragraphs.

Briefly, Program space contains user program code in ROM and user vectors; Data space contains user data in RAM and in ROM, and Stack space accommodates six levels of stack for subroutine and interrupt service routine nesting.

Figure 5. Memory Addressing Diagram

7929237 0079992 2T2
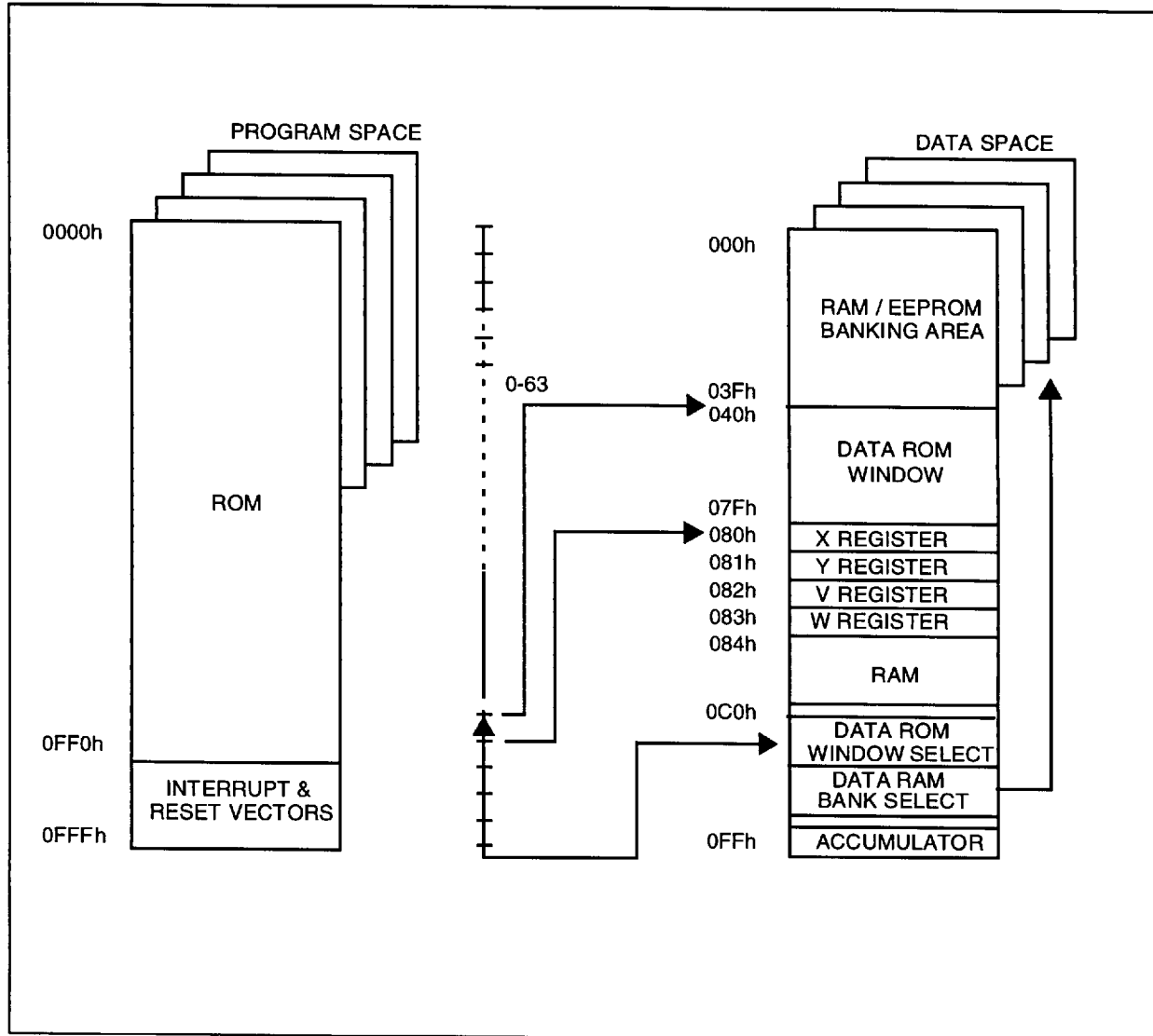
MEMORY MAP (Cont'd)

1.3.2 Program Space

Program Space is physically implemented in ROM memory. It comprises the instructions to be executed, the data required for immediate addressing mode instructions, the reserved factory test area and the user vectors. Program Space is addressed via the 12-bit Program Counter register (PC register)

1.3.2.1 ROM Protection

The ST6203B Program Space can be protected against external readout of ROM contents when the READOUT PROTECTION mask option is chosen. This option allows the user to blow a dedicated fuse on the silicon, by applying a high voltage at V_{PP} (see detailed information in the "Electrical Specification").

Note: Once the Readout Protection fuse is blown, it is no longer possible, even for SGS-THOMSON, to gain access to the ROM contents. Returned parts with a blown fuse can therefore not be accepted.

Figure 6. ST6203B ROM Memory Map
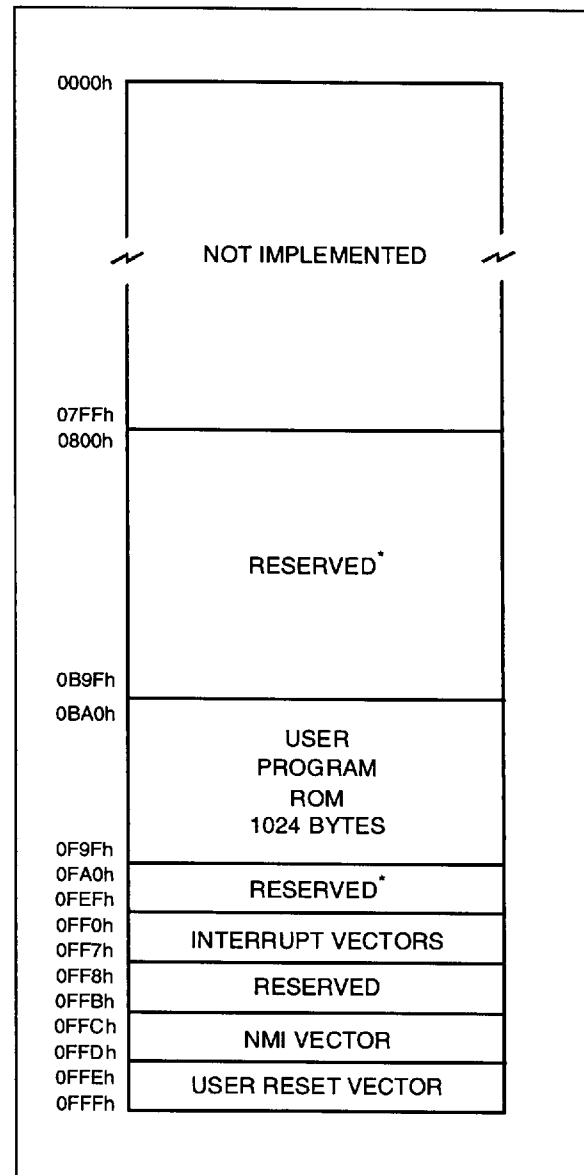
(*) Reserved areas should be filled with 0FFh

MEMORY MAP (Cont'd)

1.3.3 Data Space

Data Space accommodates all the data necessary for processing the user program. This space comprises the RAM resource, the processor core and peripheral registers, as well as read-only data such as constants and look-up tables in ROM.

1.3.3.1 Data ROM

All read-only data is physically stored in ROM memory, which also accommodates the Program Space. The ROM memory consequently contains the program code to be executed, as well as the constants and look-up tables required by the application.

The Data Space locations in which the different constants and look-up tables are addressed by the processor core may be thought of as a 64-byte window through which it is possible to access the read-only data stored in ROM.

1.3.3.2 Data RAM

In ST6203B devices, the data space includes 60 bytes of RAM, the accumulator (A), the indirect registers (X), (Y), the short direct registers (V), (W), the I/O port registers, the peripheral data and control registers, the interrupt option register and the Data ROM Window register (DRW register).

1.3.4 Stack Space

Stack space consists of six 12-bit registers which are used to stack subroutine and interrupt return addresses, as well as the current program counter contents.

Table 1. ST6203B Data Memory Space

NOT IMPLEMENTED	000h 03Fh
DATA ROM WINDOW 64 BYTES	040h 07Fh
X REGISTER	080h
Y REGISTER	081h
V REGISTER	082h
W REGISTER	083h
DATA RAM 60 BYTES	084h 0BFh
PORT A DATA REGISTER	0C0h
PORT B DATA REGISTER	0C1h
RESERVED	0C2h
RESERVED	0C3h
PORT A DIRECTION REGISTER	0C4h
PORT B DIRECTION REGISTER	0C5h
RESERVED	0C6h
RESERVED	0C7h
INTERRUPT OPTION REGISTER	0C8h*
DATA ROM WINDOW REGISTER	0C9h*
RESERVED	0CAh 0CBh
PORT A OPTION REGISTER	0CCh
PORT B OPTION REGISTER	0CDh
RESERVED	0CEh
RESERVED	0CFh
RESERVED	0D0h
OSCILLATOR CONTROL REGISTER	0D1h
TIMER PSC REGISTER	0D2h
TIMER DATA REGISTER	0D3h
TIMER TSCR REGISTER	0D4h
RESERVED	0D5h 0D7h
WATCHDOG REGISTER	0D8h
RESERVED	0D9h 0FEh
ACCUMULATOR	0FFh

* WRITE ONLY REGISTER

7929237 0079994 075

MEMORY MAP (Cont'd)

1.3.5 Data Window Register (DWR)

The Data ROM window is located from address
0040h to address 007Fh in Data space. It allows di-
rect reading of 64 consecutive bytes located any-
where in ROM memory, between address 0000h
and 1FFFh (top memory address depends on the
specific device). All the ROM memory can there-
fore be used to store either instructions or read-
only data. Indeed, the window can be moved in
steps of 64 bytes along the ROM memory by writing
the appropriate code in the Write-only Data Win-
dow register (DWR register, location 00C9h).

The DWR register can be addressed like any RAM
location in the Data Space at address 00C9h, it is
however a write-only register and cannot be ac-
cessed using single-bit operations. This register is
used to move the 64-byte read-only data window
(from address 40h to address 7Fh of the Data
space) up and down the ROM memory of the
MCU in steps of 64 bytes. The effective address of
the byte to be read as data in ROM memory is ob-
tained by concatenating the 6 least significant bits
of the register address given in the instruction (as
least significant bits) and the content of the DWR
register (as most significant bits, seeFigure 7). So
when addressing location 0040h of the Data
Space, with 0 loaded in the DWR register, the
physical location addressed in ROM is 00h. The
DWR register is not cleared on reset, therefore it
must be written to prior to the first access to the
Data ROM window area.

Data Window Register (DWR)

Address: 0C9h — Write Only

| 7							0
-	-	DWR5	DWR4	DWR3	DWR2	DWR1	DWR0

Bit 7 = This bit is not used.

Bit 6-0 = **DWR6-DWR0:** *Data ROM Window Reg-
ister Bits.* These are the Data ROM Window bits
that correspond to the upper bits of the data ROM
space.

Caution: *This register is undefined on reset. Nei-
ther read nor single bit instructions may be used to
address this register.*

Note: Care is required when handling the DWR
register as it is write only. For this reason, it is not
allowed to change the DWR contents while exe-
cuting interrupt service routine, as the service rou-
tine cannot save and then restore its previous con-
tent. If it is impossible to avoid the writing of this
register in the interrupt service routine, an image
of this register must be saved in a RAM location,
and each time the program writes to the DWR it
must write also to the image register. The image
register must be written first, so if an interrupt oc-
curs between the two instructions the DWR is not
affected.

Figure 7. Data ROM Window Memory Addressing
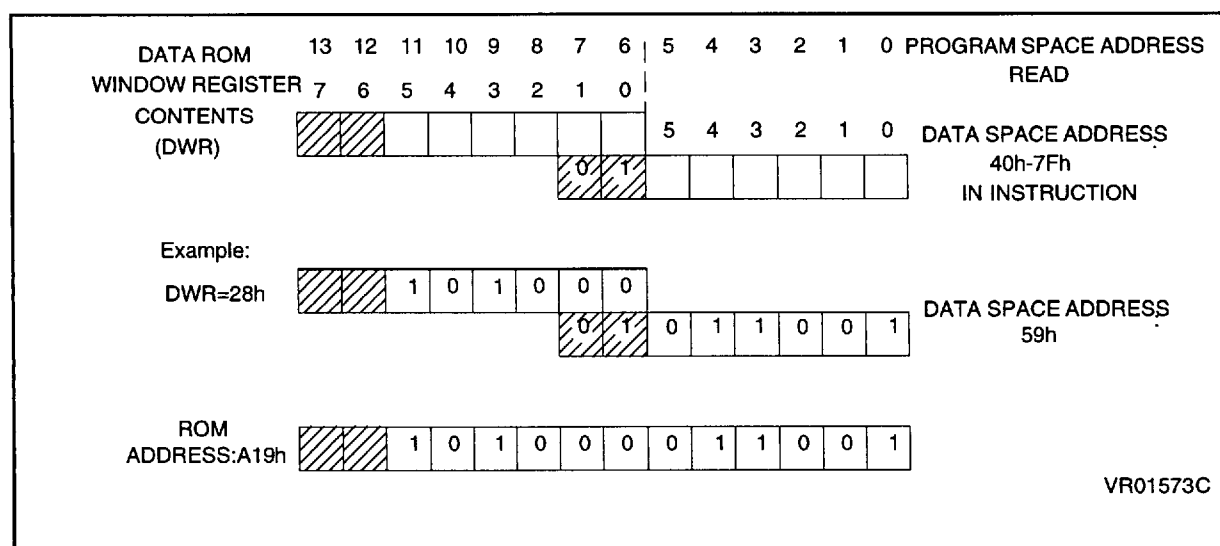
2 CENTRAL PROCESSING UNIT

2.1 INTRODUCTION

The CPU Core of ST6 devices is independent of the I/O or Memory configuration. As such, it may be thought of as an independent central processor communicating with on-chip I/O, Memory and Peripherals via internal address, data, and control buses. In-core communication is arranged as shown in Figure 8; the controller being externally linked to both the Reset and Oscillator circuits, while the core is linked to the dedicated on-chip peripherals via the serial data bus and indirectly, for interrupt purposes, through the control registers.

2.2 CPU REGISTERS

The ST6 Family CPU core features six registers and three pairs of flags available to the programmer. These are described in the following paragraphs.

Accumulator (A). The accumulator is an 8-bit general purpose register used in all arithmetic calculations, logical operations, and data manipulations. The accumulator can be addressed in Data space as a RAM location at address FFh. Thus the ST6 can manipulate the accumulator just like any other register in Data space.

Indirect Registers (X, Y). These two indirect registers are used as pointers to memory locations in Data space. They are used in the register-indirect addressing mode. These registers can be addressed in the data space as RAM locations at addresses 80h (X) and 81h (Y). They can also be accessed with the direct, short direct, or bit direct addressing modes. Accordingly, the ST6 instruction set can use the indirect registers as any other register of the data space.

Short Direct Registers (V, W). These two registers are used to save a byte in short direct addressing mode. They can be addressed in Data space as RAM locations at addresses 82h (V) and 83h (W). They can also be accessed using the direct and bit direct addressing modes. Thus, the ST6 instruction set can use the short direct registers as any other register of the data space.

Program Counter (PC). The program counter is a 12-bit register which contains the address of the next ROM location to be processed by the core. This ROM location may be an opcode, an operand, or the address of an operand. The 12-bit length allows the direct addressing of 4096 bytes in Program space.

Figure 8. ST6 Core Block Diagram

7929237 0079996 948
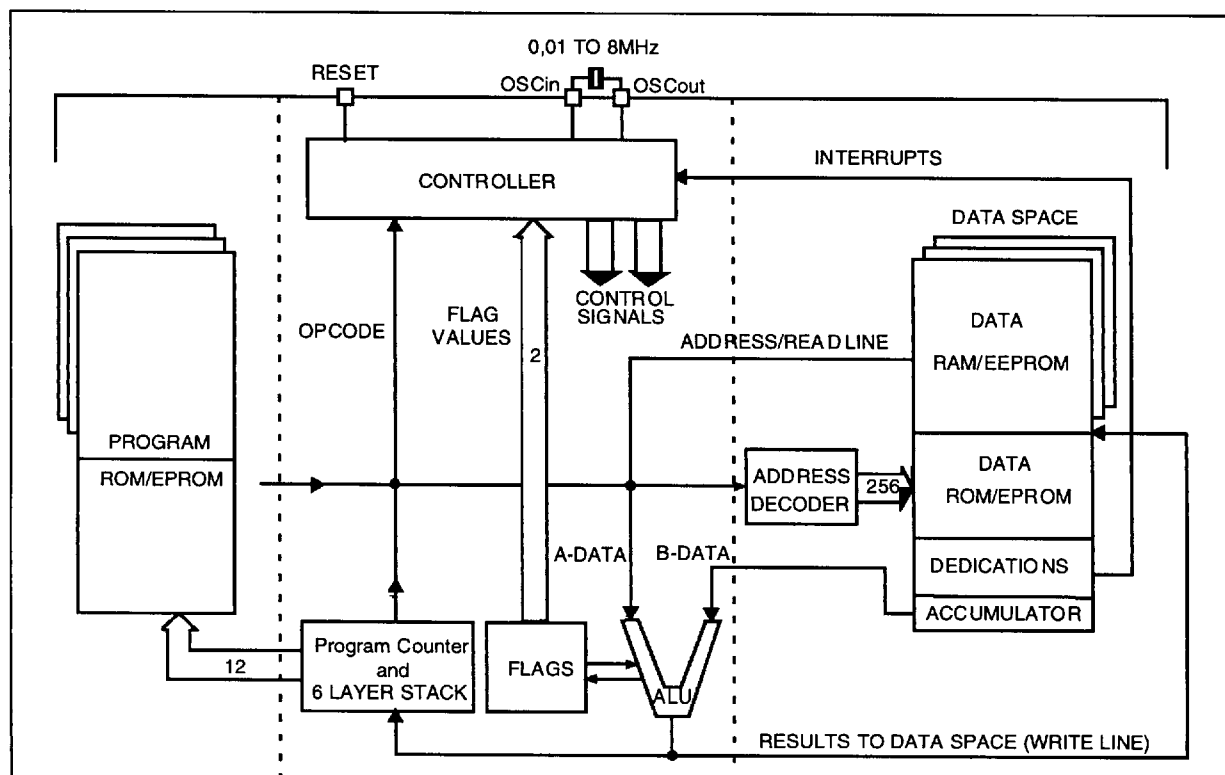
CPU REGISTERS (Cont'd)

However, if the program space contains more than 4096 bytes, the additional memory in program space can be addressed by using the Program Bank Switch register.

The PC value is incremented after reading the address of the current instruction. To execute relative jumps, the PC and the offset are shifted through the ALU, where they are added; the result is then shifted back into the PC. The program counter can be changed in the following ways:

- JP (Jump) instruction PC=Jump address

- CALL instruction PC= Call address

- Relative Branch Instruction PC= PC +/- offset

- Interrupt PC=Interrupt vector

- Reset PC= Reset vector

- RET & RETI instructions PC= Pop (stack)

- Normal instruction PC= PC + 1

Flags (C, Z). The ST6 CPU includes three pairs of flags (Carry and Zero), each pair being associated with one of the three normal modes of operation: Normal mode, Interrupt mode and Non Maskable Interrupt mode. Each pair consists of a CARRY flag and a ZERO flag. One pair (CN, ZN) is used during Normal operation, another pair is used during Interrupt mode (CI, ZI), and a third pair is used in the Non Maskable Interrupt mode (CNMI, ZNMI).

The ST6 CPU uses the pair of flags associated with the current mode: as soon as an interrupt (or a Non Maskable Interrupt) is generated, the ST6 CPU uses the Interrupt flags (resp. the NMI flags) instead of the Normal flags. When the RETI instruction is executed, the previously used set of flags is restored. It should be noted that each flag set can only be addressed in its own context (Non Maskable Interrupt, Normal Interrupt or Main routine). The flags are not cleared during context switching and thus retain their status.

The Carry flag is set when a carry or a borrow occurs during arithmetic operations; otherwise it is cleared. The Carry flag is also set to the value of the bit tested in a bit test instruction; it also participates in the rotate left instruction.

The Zero flag is set if the result of the last arithmetic or logical operation was equal to zero; otherwise it is cleared.

Switching between the three sets of flags is performed automatically when an NMI, an interrupt or a RETI instructions occurs. As the NMI mode is automatically selected after the reset of the MCU, the ST6 core uses at first the NMI flags.

Stack. The ST6 CPU includes a true LIFO hardware stack which eliminates the need for a stack pointer. The stack consists of six separate 12-bit RAM locations that do not belong to the data space RAM area. When a subroutine call (or interrupt request) occurs, the contents of each level are shifted into the next higher level, while the content of the PC is shifted into the first level (the original contents of the sixth stack level are lost). When a subroutine or interrupt return occurs (RET or RETI instructions), the first level register is shifted back into the PC and the value of each level is popped back into the previous level. Since the accumulator, in common with all other data space registers, is not stored in this stack, management of these registers should be performed within the subroutine. The stack will remain in its "deepest" position if more than 6 nested calls or interrupts are executed, and consequently the last return address will be lost. It will also remain in its highest position if the stack is empty and a RET or RETI is executed. In this case the next instruction will be executed.

Figure 9. ST6 CPU Programming Mode
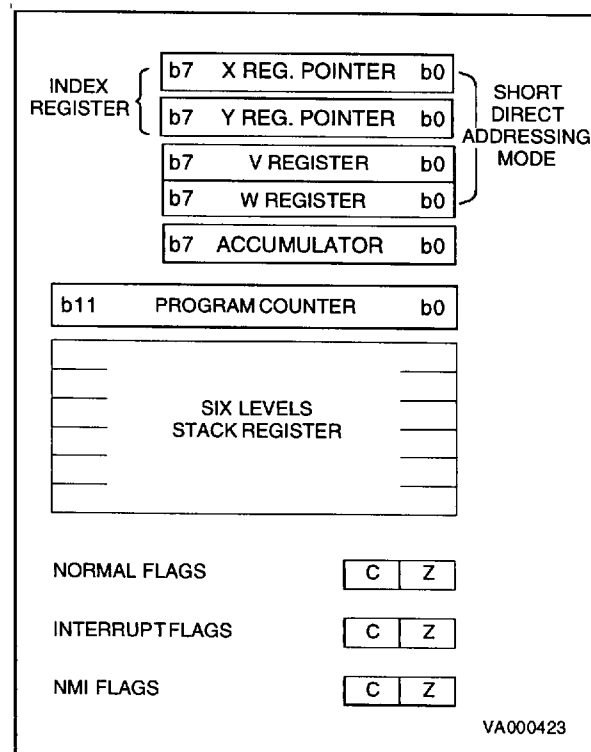
3 CLOCKS, RESET, INTERRUPTS AND POWER SAVING MODES

3.1 CLOCK SYSTEM

The MCU features a Main Oscillator which can be driven by an external clock, or used in conjunction with an AT-cut parallel resonant crystal or a suitable ceramic resonator, or with an external resistor (R_{NET}). In addition, a Low Frequency Auxiliary Oscillator (LFAO) can be switched in for security reasons, to reduce power consumption, or to offer the benefits of a back-up clock system.

The Oscillator Safeguard (OSG) option filters spikes from the oscillator lines, provides access to the LFAO to provide a backup oscillator in the event of main oscillator failure and also automatically limits the internal clock frequency (f_{INT}) as a function of V_{DD}, in order to guarantee correct operation. These functions are illustrated in Figure 11, Figure 12, Figure 13 and Figure 14.

Figure 10 illustrates various possible oscillator configurations using an external crystal or ceramic resonator, an external clock input, an external resistor (R_{NET}), or the lowest cost solution using only the LFAO. C_{L1} an C_{L2} should have a capacitance in the range 12 to 22 pF for an oscillator frequency in the 4-8 MHz range.

The internal MCU clock frequency (f_{INT}) is divided by 12 to drive the Timer and the Watchdog timer, and by 13 to drive the CPU core, as may be seen in Figure 13.

With an 8 MHz oscillator frequency, the fastest machine cycle is therefore 1.625µs.

A machine cycle is the smallest unit of time needed to execute any operation (for instance, to increment the Program Counter). An instruction may require two, four, or five machine cycles for execution.

3.1.1 Main Oscillator

The oscillator configuration may be specified by selecting the appropriate mask option. When the CRYSTAL/RESONATOR option is selected, it must be used with a quartz crystal, a ceramic resonator or an external signal provided on the OSCin pin. When the RC NETWORK option is selected, the system clock is generated by an external resistor.

The main oscillator can be turned off (when the OSG ENABLED mask option is selected) by setting the OSCOFF bit of the Oscillator Control Register (0D1h). The Low Frequency Auxiliary Oscillator is automatically started.

Figure 10. Oscillator Configurations

CRYSTAL/RESONATOR CLOCK
CRYSTAL/RESONATOR mask option

EXTERNAL CLOCK
CRYSTAL/RESONATOR mask option

RC NETWORK
RC NETWORK mask option

INTEGRATED CLOCK
CRYSTAL/RESONATOR mask option
OSG ENABLED mask option
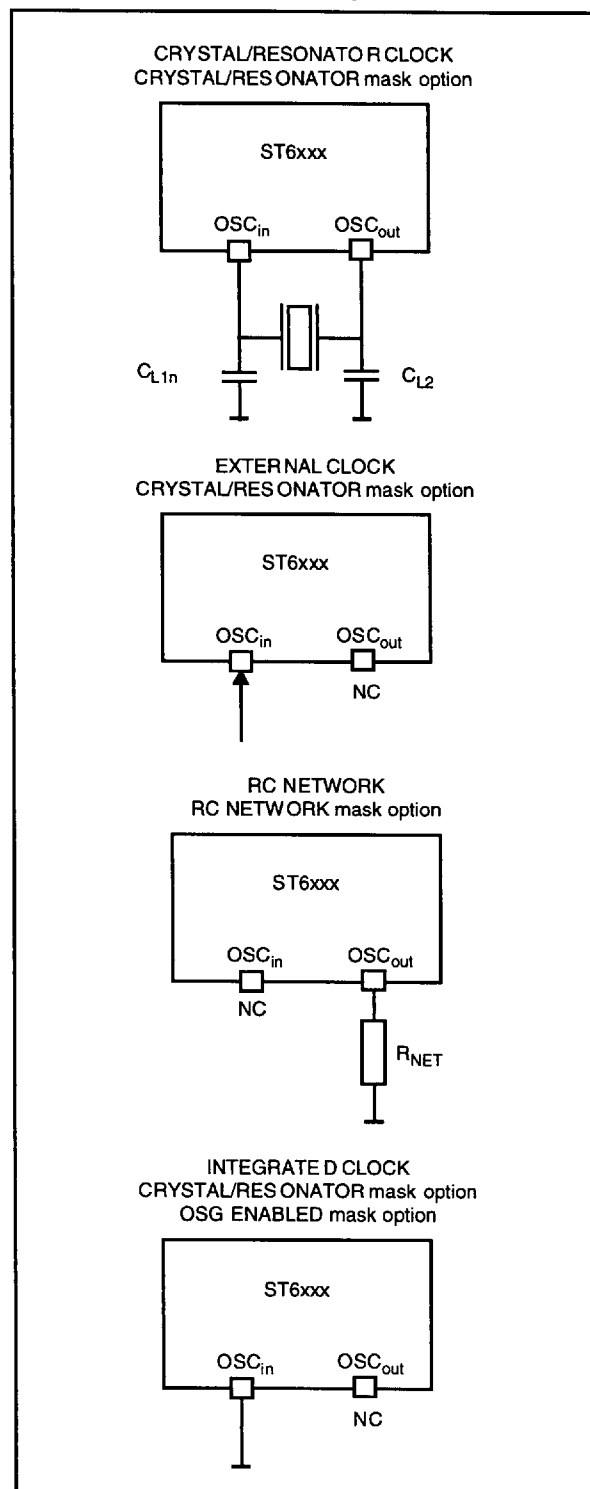
CLOCK SYSTEM (Cont'd)

Turning on the main oscillator is achieved by resetting the OSCOFF bit of the Oscillator Control Register or by resetting the MCU. Restarting the main oscillator implies a delay comprising the oscillator start up delay period plus the duration of the software instruction at f_{LFAO} clock frequency.

3.1.2 Low Frequency Auxiliary Oscillator (LFAO)

The Low Frequency Auxiliary Oscillator has three main purposes. Firstly, it can be used to reduce power consumption in non timing critical routines. Secondly, it offers a fully integrated system clock, without any external components. Lastly, it acts as a safety oscillator in case of main oscillator failure.

This oscillator is available when the OSG ENABLED mask option is selected. In this case, it automatically starts one of its periods after the first missing edge from the main oscillator, whatever the reason (main oscillator defective, no clock circuitry provided, main oscillator switched off...).

User code, normal interrupts, WAIT and STOP instructions, are processed as normal, at the reduced f_{LFAO} frequency.

At power on, the Low Frequency Auxiliary Oscillator starts faster than the Main Oscillator. It therefore feeds the on-chip counter generating the POR delay until the Main Oscillator runs.

The Low Frequency Auxiliary Oscillator is automatically switched off as soon as the main oscillator starts.

OSCR

Address: 0D1h — Read/Write

7							0
OSCR 7	OSCR 6	OSCR 5	OSCR 4	OSCR 3	OSC OFF	OSCR 1	OSCR 0

Bit 7-3, 1-0= **OSCR7-OSCR3, OSCR1-OSCR0** *ADC Control Register.* These bits are not used.

Bit 2 = **OSCOFF**. When low, this bit enables main oscillator to run. The main oscillator is switched off when OSCOFF is high.

3.1.3 Oscillator Safe Guard

The Oscillator Safe Guard (OSG) affords drastically increased operational integrity in ST62xx devices. The OSG circuit provides three basic functions: it filters spikes from the oscillator lines which would result in over frequency to the ST62 CPU; it gives access to the Low Frequency Auxiliary Oscillator (LFAO), used to ensure minimum processing in case of main oscillator failure, to offer reduced power consumption or to provide a fixed frequency low cost oscillator; finally, it automatically limits the internal clock frequency as a function of supply voltage, in order to ensure correct operation even if the power supply should drop.
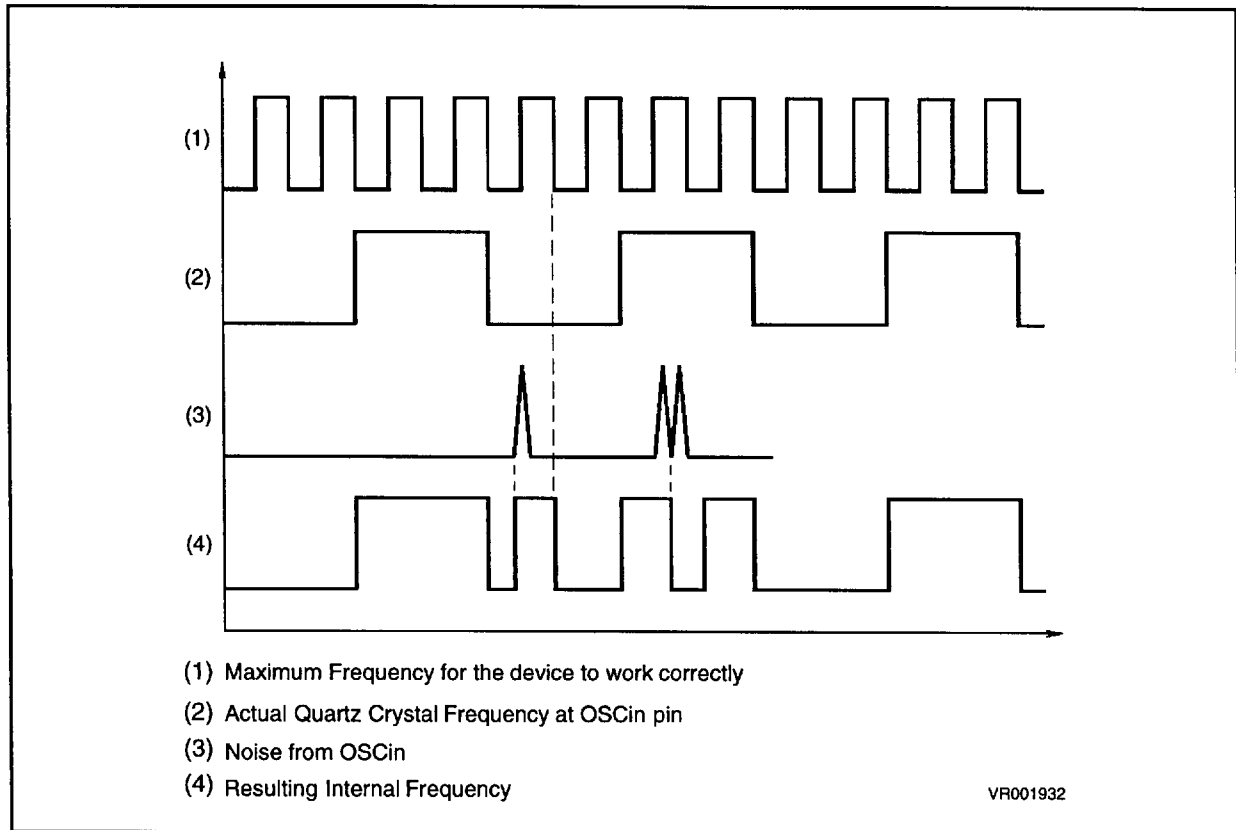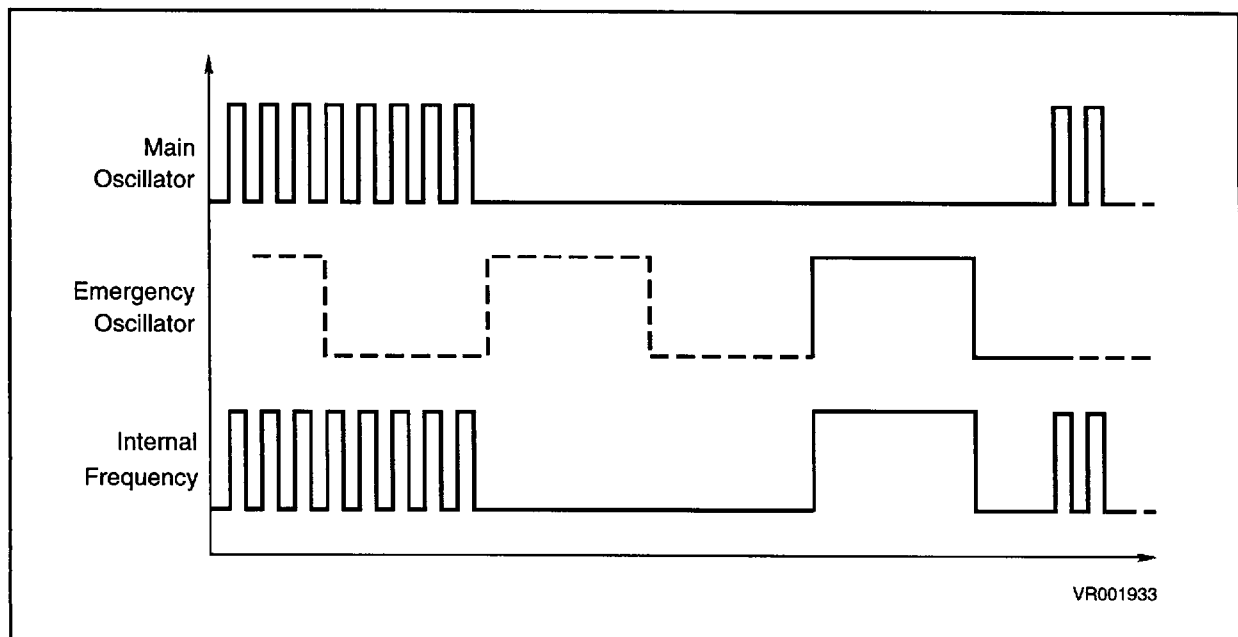
The OSG is enabled or disabled by choosing the relevant OSG mask option. It may be viewed as a filter whose cross-over frequency is device dependent.

Spikes on the oscillator lines result in an effectively increased internal clock frequency. In the absence of an OSG circuit, this may lead to an over frequency for a given power supply voltage. The OSG filters out such spikes (as illustrated in Figure 11). In all cases, when the OSG is active, the maximum internal clock frequency, f_{INT}, is limited to f_{OSG}, which is supply voltage dependent. This relationship is illustrated in Figure 14.

When the OSG is enabled, the Low Frequency Auxiliary Oscillator may be accessed. This oscillator starts operating after the first missing edge of the main oscillator (see Figure 12).

Over-frequency, at a given power supply level, is seen by the OSG as spikes; it therefore filters out some cycles in order that the internal clock frequency of the device is kept within the range the particular device can stand (depending on V_{DD}), and below f_{OSG}: the maximum authorised frequency with OSG enabled.

Note. The OSG should be used wherever possible as it provides maximum safety. Care must be taken, however, as it can increase power consumption and reduce the maximum operating frequency to f_{OSG}.

CLOCK SYSTEM (Cont'd)

Figure 11. OSG Filtering Principle

(1) Maximum Frequency for the device to work correctly

(2) Actual Quartz Crystal Frequency at OSCin pin

(3) Noise from OSCin

(4) Resulting Internal Frequency

VR001932

Figure 12. OSG Emergency Oscillator Principle

VR001933

7929237 0080000 862

CLOCK SYSTEM (Cont'd)

Figure 13. Clock Circuit Block Diagram
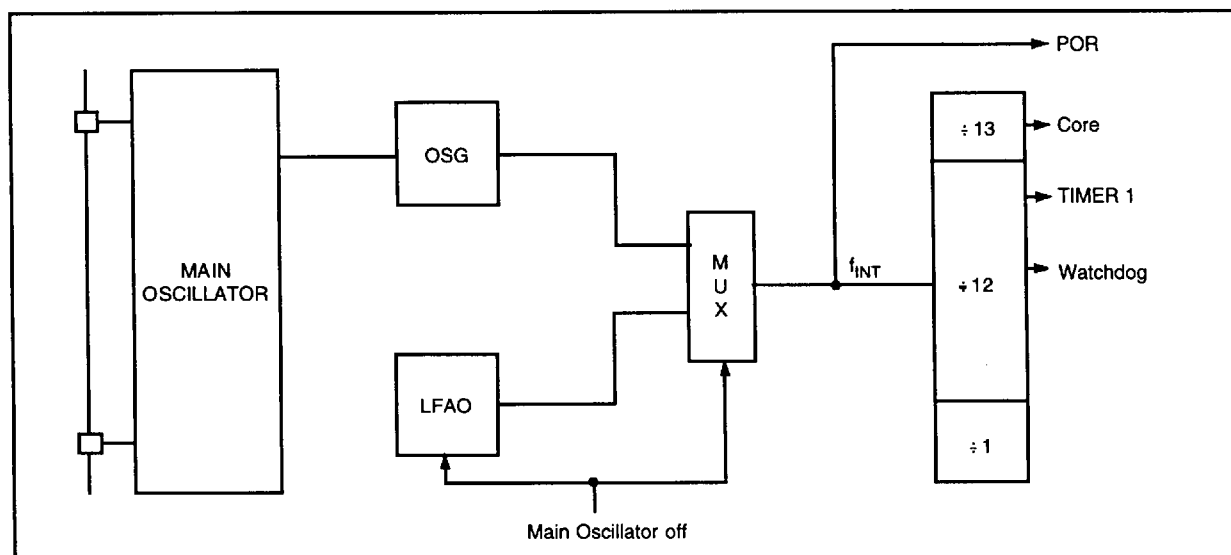
Figure 14. Maximum Operating Frequency (f_{MAX}) versus Supply Voltage (V_{DD})
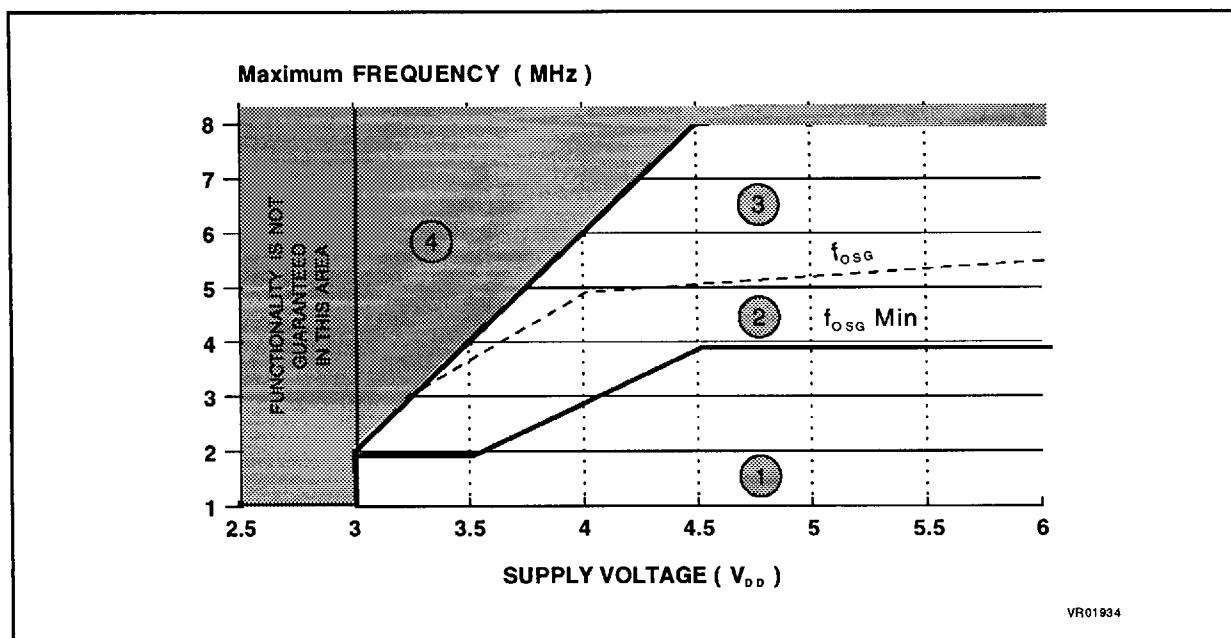
Notes:

1. In this area, operation is guaranteed at the quartz crystal frequency.

2. When the OSG is disabled, operation in this area is guaranteed at the crystal frequency. When the OSG is enabled, operation in this area is guaranteed at a frequency of at least $f_{OSG\ Min}$.

3. When the OSG is disabled, operation in this area is guaranteed at the quartz crystal frequency. When the OSG is enabled, access to this area is prevented. The internal frequency is kept a f_{OSG}.

4. When the OSG is disabled, operation in this area is not guaranteed
When the OSG is enabled, access to this area is prevented. The internal frequency is kept at f_{OSG}.

3.2 RESETS

The MCU can be reset in three ways:
- by the external Reset input being pulled low;
- by Power-on Reset;
- by the digital Watchdog peripheral timing out.

3.2.1 RESET Input

The RESET pin may be connected to a device of the application board in order to reset the MCU if required. The RESET pin may be pulled low in RUN, WAIT or STOP mode. This input can be used to reset the MCU internal state and ensure a correct start-up procedure. The pin is active low and features a Schmitt trigger input. The internal Reset signal is generated by adding a delay to the external signal. Therefore even short pulses on the RESET pin are acceptable, provided V_{DD} has completed its rising phase and that the oscillator is running correctly (normal RUN or WAIT modes). The MCU is kept in the Reset state as long as the RESET pin is held low.

If RESET activation occurs in the RUN or WAIT modes, processing of the user program is stopped (RUN mode only), the Inputs and Outputs are configured as inputs with pull-up resistors and the main Oscillator is restarted. When the level on the RESET pin then goes high, the initialization sequence is executed following expiry of the internal delay period.

If RESET pin activation occurs in the STOP mode, the oscillator starts up and all Inputs and Outputs are configured as inputs with pull-up resistors. When the level of the RESET pin then goes high, the initialization sequence is executed following expiry of the internal delay period.

3.2.2 Power-on Reset

The function of the POR circuit consists in waking up the MCU at an appropriate stage during the power-on sequence. At the beginning of this sequence, the MCU is configured in the Reset state: all I/O ports are configured as inputs with pull-up resistors and no instruction is executed. When the power supply voltage rises to a sufficient level, the oscillator starts to operate, whereupon an internal delay is initiated, in order to allow the oscillator to fully stabilize before executing the first instruction. The initialization sequence is executed immediately following the internal delay.

The internal delay is generated by an on-chip counter. The internal reset line is released 2048 internal clock cycles after release of the external reset.

Notes:

To ensure correct start-up, the user should take care that the reset signal is not released before the V_{DD} level is sufficient to allow MCU operation at the chosen frequency (see Recommended Operating Conditions).

A proper reset signal for a slow rising V_{DD} supply can generally be provided by an external RC network connected to the RESET pin.

Figure 15. Reset and Interrupt Processing

7929237 0080002 635
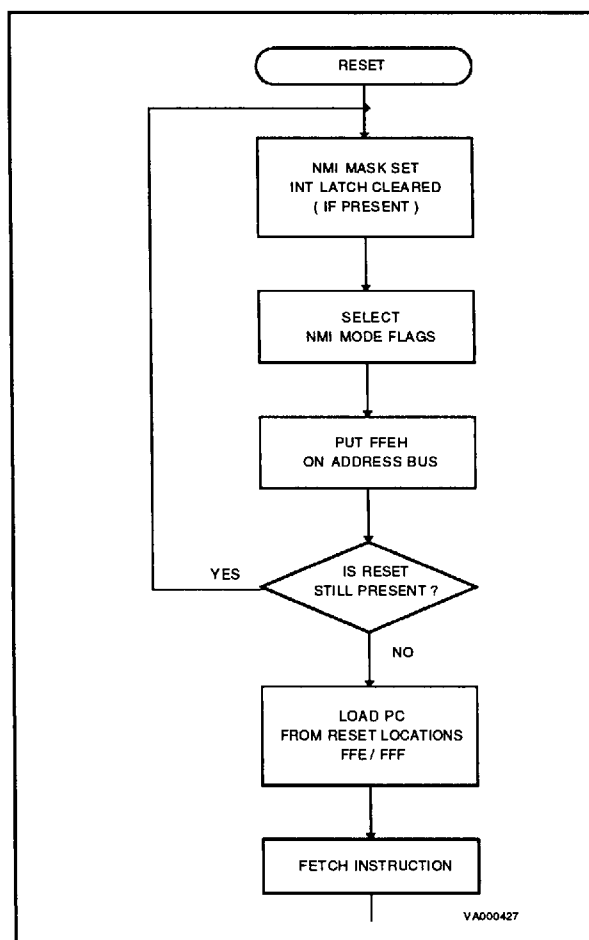
RESETS (Cont'd)

3.2.3 Watchdog Reset

The MCU provides a Watchdog timer function in order to ensure graceful recovery from software upsets. If the Watchdog register is not refreshed before an end-of-count condition is reached, the internal reset will be activated. This, amongst other things, resets the watchdog counter.

The MCU restarts just as though the Reset had been generated by the RESET pin, including the built-in stabilisation delay period.

3.2.4 Application Notes

No external resistor is required between V_{DD} and the Reset pin, thanks to the built-in pull-up device.

The POR circuit operates dynamically, in that it triggers MCU initialization on detecting the rising edge of V_{DD}. The typical threshold is in the region of 2 volts, but the actual value of the detected threshold depends on the way in which V_{DD} rises.

The POR circuit is *NOT* designed to supervise static, or slowly rising or falling V_{DD}.

3.2.5 MCU Initialization Sequence

When a reset occurs the stack is reset, the PC is loaded with the address of the Reset Vector (located in program ROM starting at address 0FFEh). A jump to the beginning of the user program must be coded at this address. Following a Reset, the Interrupt flag is automatically set, so

that the CPU is in Non Maskable Interrupt mode; this prevents the initialisation routine from being interrupted. The initialisation routine should therefore be terminated by a RETI instruction, in order to revert to normal mode and enable interrupts. If no pending interrupt is present at the end of the initialisation routine, the MCU will continue by processing the instruction immediately following the RETI instruction. If, however, a pending interrupt is present, it will be serviced.

Figure 16. Reset and Interrupt Processing
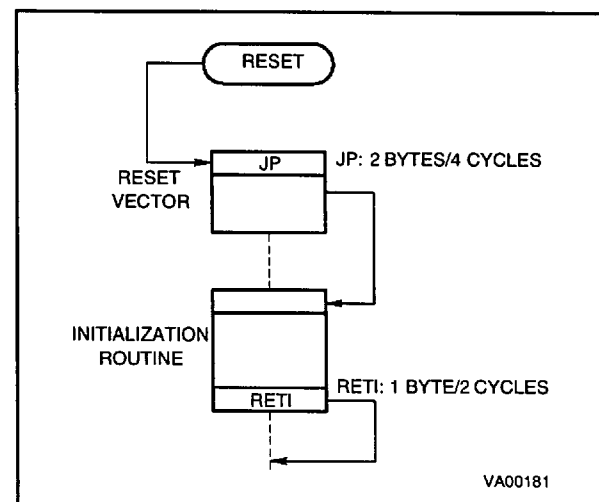
Figure 17. Reset Block Diagram
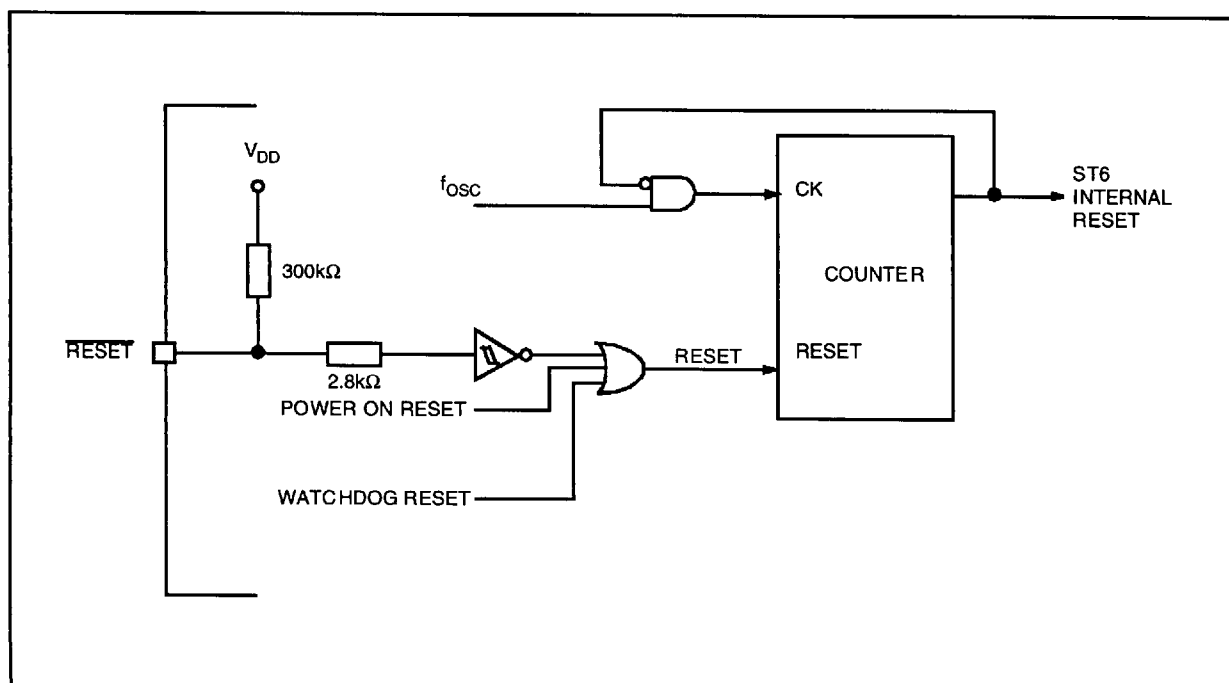
RESETS (Cont'd)

Table 2. Register Reset Status

Register	Address(es)	Status	Comment
Port Data Registers (PA, PB) Port Direction Register (PA, PB) Port Option Register (PA, PB) Interrupt Option Register Timer Status/Control	0C0h to 0C1h 0C4h to 0C5h 0CCh to 0CDh 0C8h 0D4h	00h	I/Os are Inputs with pull-up I/Os are Inputs with pull-up Interrupts disabled Timer disabled
X, Y, V, W Register Accumulator Data RAM Data ROM Window Register	080h to 083h 0FFh 084h to 0BFh 0C9h	Undefined	
Timer Counter Register Timer Prescaler Register Watchdog Counter Register	0D3h 0D2h 0D8h	FFh 7Fh FEh	Maximum count loaded
Oscillator Control Register	0D1h	40h	main oscillator on

3.3 DIGITAL WATCHDOG

The digital Watchdog consists of a reloadable downcounter timer which can be used to provide controlled recovery from software upsets.

The Watchdog circuit generates a Reset when the downcounter reaches zero. User software can prevent this reset by reloading the counter, and should therefore be written so that the counter is regularly reloaded while the user program runs correctly. In the event of a software mishap (usually caused by externally generated interference), the user program will no longer behave in its usual fashion and the timer register will thus not be reloaded periodically. Consequently the timer will decrement down to 00h and reset the MCU. In order to maximise the effectiveness of the Watchdog function, user software must be written with this concept in mind.

Watchdog behaviour is governed by two mask options, known as "WATCHDOG ACTIVATION" (i.e. HARDWARE or SOFTWARE) and "EXTERNAL STOP MODE CONTROL" (see Table 3).

In the SOFTWARE mask option, the Watchdog is disabled until bit C of the DWDR register has been set. When the Watchdog is disabled, low power Stop mode is available. Once activated, the Watchdog cannot be disabled, save by resetting the MCU.

In the HARDWARE mask option, the Watchdog is permanently enabled. Since the oscillator will run continuously, low power mode is not available. The STOP instruction is interpreted as a WAIT instruction, and the Watchdog continues to countdown.

However, when the EXTERNAL STOP MODE CONTROL mask option (available in ROM versions only) has been selected low power consumption may be achieved in Stop Mode.

Execution of the STOP instruction is then governed by a secondary function associated with the NMI pin. If a STOP instruction is encountered when the NMI pin is low, it is interpreted as WAIT, as described above. If, however, the STOP instruction is encountered when the NMI pin is high, the Watchdog counter is frozen and the CPU enters STOP mode.

When the MCU exits STOP mode (i.e. when an interrupt is generated), the Watchdog resumes its activity.

Note: when the EXTERNAL STOP MODE CONTROL mask option has been selected, port PB0 must be defined as an open-drain output, and PA2 as an input.

Table 3. Recommended Mask Option Choices

Functions Required	Recommended Mask Options
Stop Mode & Watchdog	"EXTERNAL STOP MODE" & "HARDWARE WATCHDOG"
Stop Mode	"SOFTWARE WATCHDOG"
Watchdog	"HARDWARE WATCHDOG"

DIGITAL WATCHDOG (Cont'd)

The Watchdog is associated with a Data space register (Digital WatchDog Register, DWDR, location 0D8h) which is described in greater detail in Section 3.3.1. This register is set to 0FEh on Reset: bit C is cleared to "0", which disables the Watchdog; the timer downcounter bits, T0 to T5, and the SR bit are all set to "1", thus selecting the longest Watchdog timer period. This time period can be set to the user's requirements by setting the appropriate value for bits T0 to T5 in the DWDR register. The SR bit must be set to "1", since it is this bit which generates the Reset signal when it changes to "0"; clearing this bit would generate an immediate Reset.

It should be noted that the order of the bits in the DWDR register is inverted with respect to the associated bits in the down counter: bit 7 of the DWDR register corresponds, in fact, to T0 and bit 2 to T5. The user should bear in mind the fact that these bits are inverted and shifted with respect to the physical counter bits when writing to this register. The relationship between the DWDR register bits and the physical implementation of the Watchdog timer downcounter is illustrated inFigure 18.

Only the 6 most significant bits may be used to define the time period, since it is bit 6 which triggers the Reset when it changes to "0". This offers the user a choice of 64 timed periods ranging from 3,072 to 196,608 clock cycles (with an oscillator frequency of 8MHz, this is equivalent to timer periods ranging from 384μs to 24.576ms).

Figure 18. Watchdog Counter Control
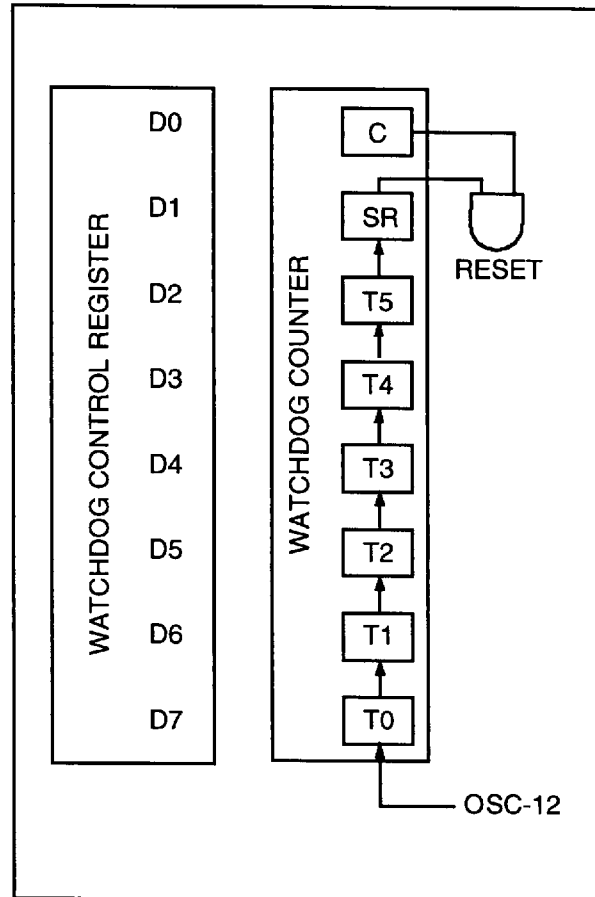
DIGITAL WATCHDOG (Cont'd)

3.3.1 Digital Watchdog Register (DWDR)

Address: 0D8h — Read/Write

Reset status: 1111 1110b

7							0
T0	T1	T2	T3	T4	T5	SR	C

Bit 0 = C: *Watchdog Control bit*

If the hardware option is selected, this bit is forced high and the user cannot change it (the Watchdog is always active). When the software option is selected, the Watchdog function is activated by setting bit C to 1, and cannot then be disabled (save by resetting the MCU).

When C is kept low the counter can be used as a 7-bit timer.

This bit is cleared to "0" on Reset.

Bit 1 = SR: *Software Reset bit*

This bit triggers a Reset when cleared.

When C = "0" (Watchdog disabled) it is the MSB of the 7-bit timer.

This bit is set to "1" on Reset.

Bits 2-7 = T5-T0: *Downcounter bits*

It should be noted that the register bits are reversed and shifted with respect to the physical counter: bit-7 (T0) is the LSB of the Watchdog downcounter and bit-2 (T5) is the MSB.

These bits are set to "1" on Reset.

3.3.2 Application Notes

The Watchdog plays an important supporting role in the high noise immunity of ST62xx devices, and should be used wherever possible. Watchdog related options should be selected on the basis of a trade-off between application security and STOP mode availability.

When STOP mode is not required, hardware activation without EXTERNAL STOP MODE CONTROL should be preferred, as it provides maximum security, especially during power-on.

When STOP mode is required, hardware activation and EXTERNAL STOP MODE CONTROL should be chosen. NMI should be high by default, to allow STOP mode to be entered when the MCU is idle.

The NMI pin can be connected to PB0 (seeFigure 19) to allow its state to be controlled by software. PB0 can then be used to keep NMI low while Watchdog protection is required, or to avoid noise or key bounce. When no more processing is required, PB0 is released and the device placed in STOP mode for lowest power consumption.

When software activation is selected and the Watchdog is not activated, the downcounter may be used as a simple 7-bit timer (remember that the bits are in reverse order).

The software activation option should be chosen only when the Watchdog counter is to be used as a timer. To ensure the Watchdog has not been unexpectedly activated, the following instructions should be executed within the first 27 instructions:

```
jrr 0, WD, #+3
ldi WD, 0FDH
```

DIGITAL WATCHDOG (Cont'd)

These instructions test the C bit and Reset the MCU (i.e. disable the Watchdog) if the bit is set (i.e. if the Watchdog is active), thus disabling the Watchdog.

In all modes, a minimum of 28 instructions are executed after activation, before the Watchdog can generate a Reset. Consequently, user software should load the watchdog counter within the first 27 instructions following Watchdog activation (software mode), or within the first 27 instructions executed following a Reset (hardware activation).

It should be noted that when the GEN bit is low (interrupts disabled), the NMI interrupt is active but cannot cause a wake up from STOP/WAIT modes.

Figure 19. A typical circuit making use of the EXERNAL STOP MODE CONTROL feature

VR02002
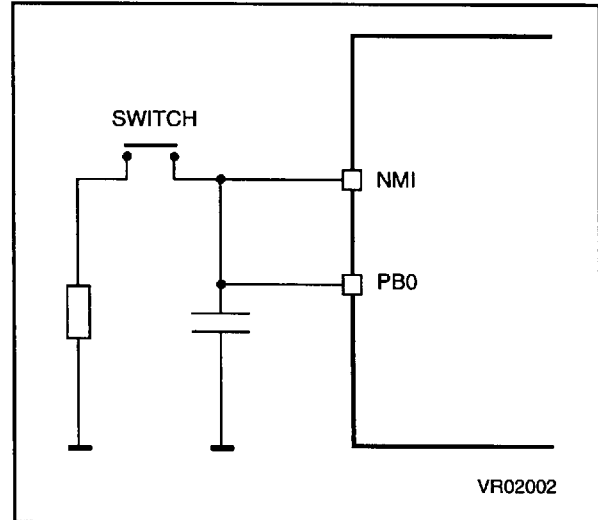
Figure 20. Digital Watchdog Block Diagram

VA00010

7929237 0080008 053
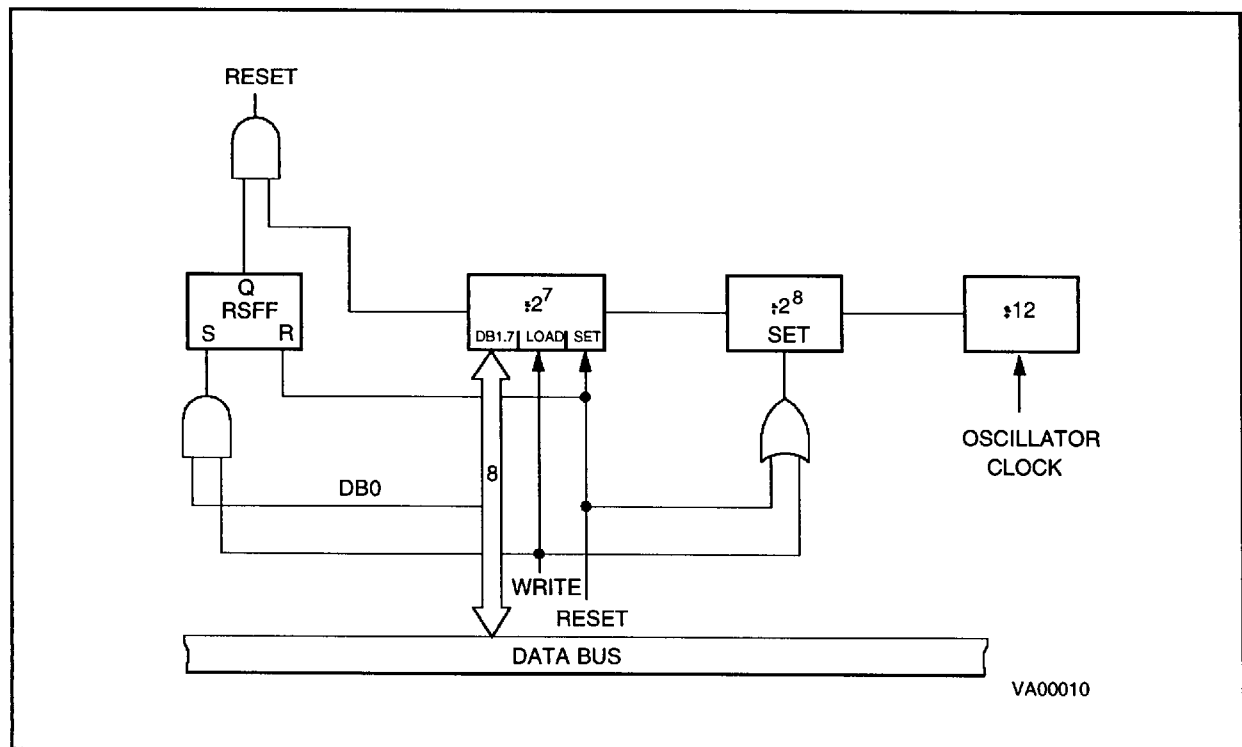
3.4 INTERRUPTS

The CPU can manage four Maskable Interrupt sources, in addition to a Non Maskable Interrupt source (top priority interrupt). Each source is associated with a specific Interrupt Vector which contains a Jump instruction to the associated interrupt service routine. These vectors are located in Program space (see Table 4).

When an interrupt source generates an interrupt request, and interrupt processing is enabled, the PC register is loaded with the address of the interrupt vector (i.e. of the Jump instruction), which then causes a Jump to the relevant interrupt service routine, thus servicing the interrupt.

Table 4. Interrupt Vector Map

Interrupt Source	Associated Vector	Vector Address
NMI pin	Interrupt vector #0 (NMI)	(FFCh-FFDh)
Port A pins	Interrupt vector #1	(FF6h-FF7h)
Port B pins	Interrupt vector #2	(FF4h-FF5h)
TIMER peripheral	Interrupt vector #3	(FF2h-FF3h)
Reserved	Interrupt vector #4	(FF0h-FF1h)

3.4.1 Interrupt Vectors

Interrupt vectors are Jump addresses to the associated service routine, which reside in specific areas of Program space. The following vectors are present:

The interrupt vector associated with the non-maskable interrupt source is referred to as Interrupt Vector #0. It is located at addresses 0FFCh and 0FFDh in Program space. This vector is associated with the falling edge sensitive Non Maskable Interrupt pin (NMI).

– The interrupt vector associated with Port A pins is referred to as interrupt vector #1. It is located at addresses 0FF6h, 0FF7h is named. It can be programmed either as falling edge sensitive or as low level sensitive, by setting the Interrupt Option Register (IOR) accordingly.

– The interrupt vector associated with Port B pins is referred to as interrupt vector #2. It is located at addresses 0FF4h, 0FF5h is named . It can be programmed either as falling edge sensitive or as rising edge sensitive, by setting the Interrupt Option Register (IOR) accordingly.

– The two interrupt vectors located respectively at addresses 0FF2h, 0FF3h and addresses 0FF0h, 0FF1h are respectively known as Interrupt Vectors #3 and #4. Vector #3 is associated with the TIMER peripheral and Vector #4 is reserved.

On-chip peripheral has an associated interrupt request flag (TMZ for the Timer, which is set to "1" when the peripheral generates an interrupt request. Each on-chip peripheral also has an associated mask bit (ETI for the Timer), which must be set to "1" to enable the associated interrupt request.

3.4.2 Interrupt Priorities

The Non Maskable Interrupt request has the highest priority and can interrupt any interrupt routine at any time; the other four interrupts cannot interrupt each other. If more than one interrupt request is pending, these are processed by the processor core according to their priority level: vector #1 has the higher priority while vector #3 the lower. The priority of each interrupt source is fixed.

IINTERRUPTS (Cont'd)·

3.4.3 Interrupt Option Register (IOR)

The Interrupt Option Register (IOR) is used to en-
able/disable the individual interrupt sources and to
select the operating mode of the external interrupt
inputs. This register is write-only and cannot be
accessed by single-bit operations.

Address: 0C8h — Write Only

Reset status: 00h

```
7                                    0
┌───┬─────┬─────┬─────┬───┬───┬───┬───┐
│ - │ LES │ ESB │ GEN │ - │ - │ - │ - │
└───┴─────┴─────┴─────┴───┴───┴───┴───┘
```

Bit 7, Bits 3-0 = *Unused.*

Bit 6 = **LES**: *Level/Edge Selection bit*

When this bit is set to one, the interrupt #1 (Port A)
is low level sensitive, when cleared to zero the
negative edge sensitive interrupt is selected.

Bit 5 = **ESB**: *Edge Selection bit*

When this bit is set to one, the interrupt #2 (Port B)
is positive edge sensitive, when cleared to zero
the negative edge sensitive interrupt is selected.

Bit 4 = **GEN**: *Global Enable Interrupt* When this
bit is set to one, all interrupts are enabled. When
this bit is cleared to zero all the interrupts (exclud-
ing NMI) are disabled.

When the GEN bit is low, the NMI interrupt is active
but cannot cause a wake up from STOP/WAIT
modes.

This register is cleared on reset.

Table 5. Interrupt Options

GEN	SET	Enables all interrupts
	CLEARED	Disables all interrupts
ESB	SET	Rising edge mode on Interrupt Port B
	CLEARED	Falling edge mode on Interrupt Port B
LES	SET	Level sensitive mode on Interrupt Port A
	CLEARED	Falling edge sensitive mode on Inter-rupt mode Port A

3.4.4 External Interrupt Operating Modes

The NMI interrupt is associated with the external
interrupt pin. This pin is falling edge sensitive and
the interrupt pin signal is latched by a flip-flop
which is automatically reset by the core at the be-
ginning of the non-maskable interrupt service rou-
tine. A Schmitt trigger is present on the NMI pin.
The user can choose to have an on-chip pull-up
on the NMI pin by specifying the appropriate ROM
mask option (see Option List at the end of the Da-
tasheet).

The two interrupt sources associated with the fall-
ing/rising edge mode of the external interrupt pins
(Port A-vector #1, Port B-vector #2) are connected
to two internal latches. Each latch is set when a
falling/rising edge occurs during the processing of
the previous one, will be processed as soon as the
first one has been serviced (unless a higher prior-
ity interrupt request is present). If more than one
interrupt occurs while processing the first one, the
subsequent ones will be lost.

Storage of interrupt requests is not available in
level sensitive detection mode. To be taken into
account, the low level must be present on the in-
terrupt pin when the MCU samples the line after
instruction execution.

At the end of every instruction, the MCU tests the
interrupt lines: if there is an interrupt request the
next instruction is not executed and the appropri-
ate interrupt service routine is executed instead.

When the GEN bit is low, the NMI interrupt is ac-
tive but cannot cause a wake up from STOP/WAIT
modes.

■ 7929237 0080010 701 ■

IINTERRUPTS (Cont'd)

3.4.5 Interrupt Procedure

The interrupt procedure is very similar to a call procedure, indeed the user can consider the interrupt as an asynchronous call procedure. As this is an asynchronous event, the user cannot know the context and the time at which it occurred. As a result, the user should save all Data space registers which may be used within the interrupt routines. There are separate sets of processor flags for normal, interrupt and non-maskable interrupt modes, which are automatically switched and so do not need to be saved.

The following list summarizes the interrupt procedure:

MCU

– The interrupt is detected.

– The C and Z flags are replaced by the interrupt flags (or by the NMI flags).

– The PC contents are stored in the first level of the stack.

– The normal interrupt lines are inhibited (NMI still active).

– The first internal latch is cleared.

– The associated interrupt vector is loaded in the PC.

User

– User selected registers are saved within the interrupt service routine (normally on a software stack).

– The source of the interrupt is found by polling the interrupt flags (if more than one source is associated with the same vector).

– The interrupt is serviced.

– Return from interrupt (RETI)

MCU

– Automatically the MCU switches back to the normal flag set (or the interrupt flag set) and pops the previous PC value from the stack.

The interrupt routine usually begins by the identifying the device which generated the interrupt request (by polling). The user should save the registers which are used within the interrupt routine in a software stack. After the RETI instruction is executed, the MCU returns to the main routine.

Figure 21. Interrupt Processing Flow Chart

VA00 001 4
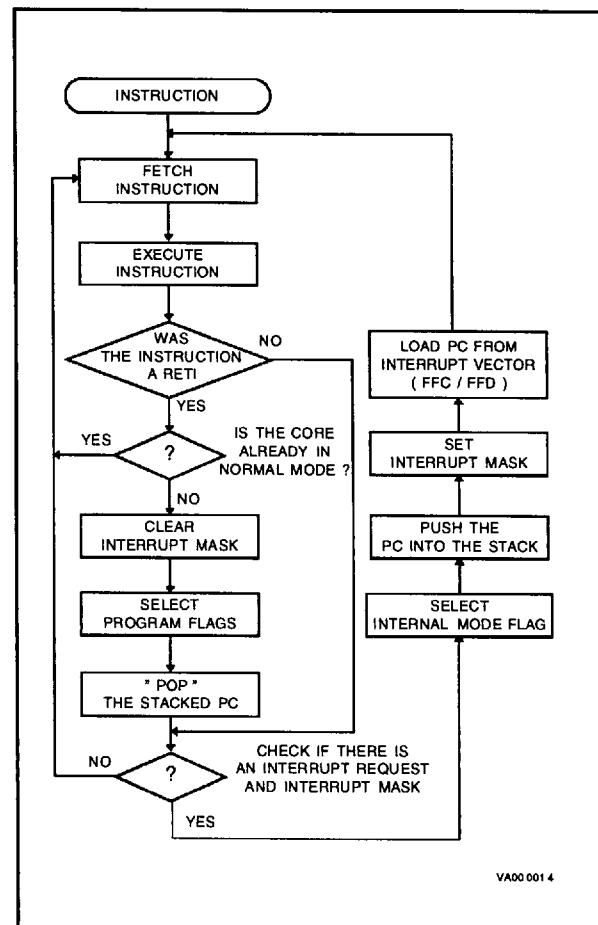
INTERRUPTS (Cont'd)

Table 6. Interrupt Requests and Mask Bits

Peripheral	Register	Address Register	Mask bit	Masked Interrupt Source	Interrupt vector
GENERAL	IOR	C8h	GEN	All Interrupts, excluding NM	
TIMER	TSCR	D4h	ETI	TMZ: TIMER Overflow	Vector 3
Port PAn	ORPA-DRPA	C4h-CCh	ORPAn-DRPAn	PAn pin	Vector 1
Port PBn	ORPB-DRPB	C5h-CDh	ORPBn-DRPBn	PBn pin	Vector 2

Figure 22. Interrupt Block Diagram

7929237 0080012 584
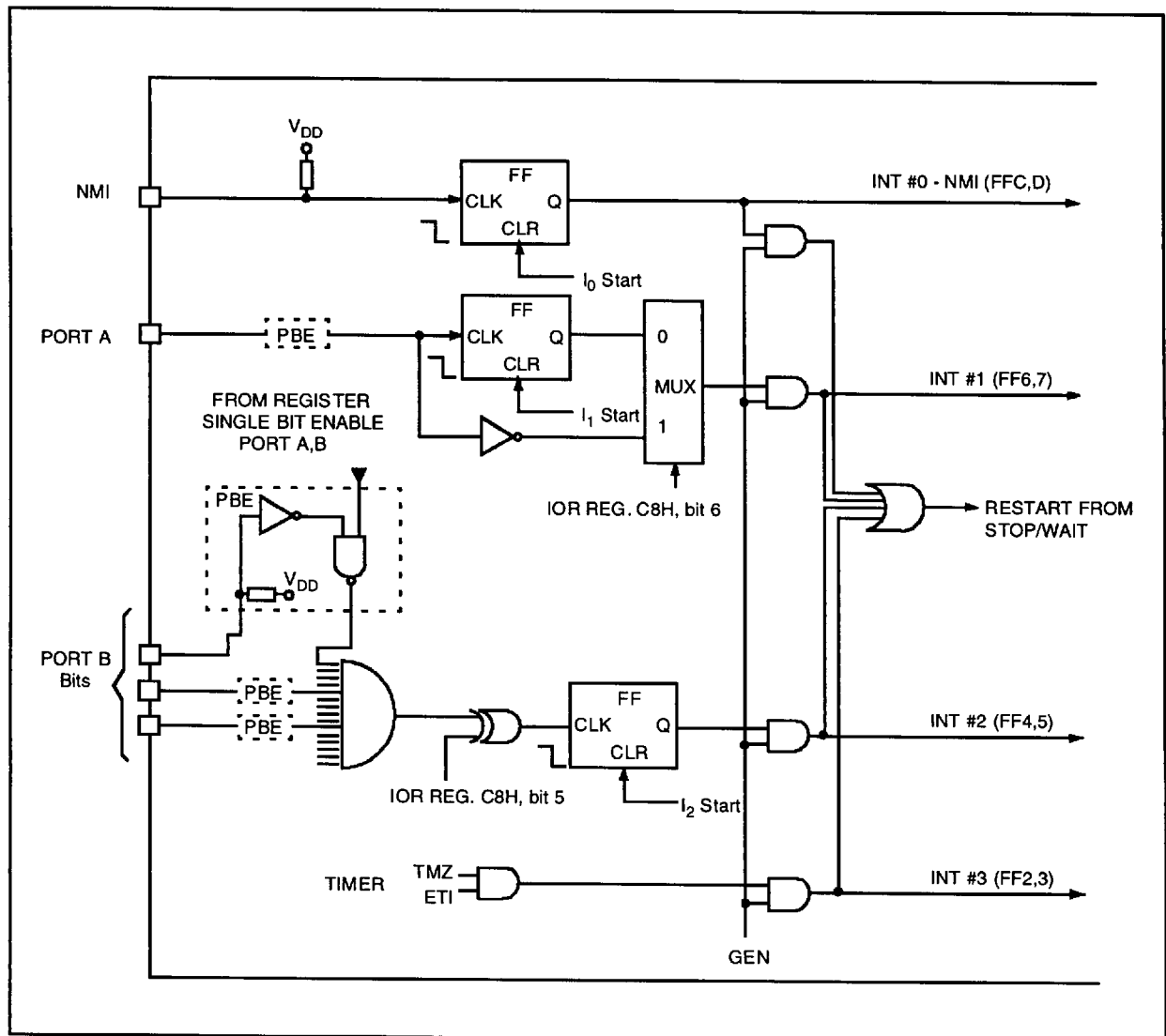
3.5 POWER SAVING MODES

The WAIT and STOP modes have been implemented in the ST62xx family of MCUs in order to reduce the product's electrical consumption during idle periods. These two power saving modes are described in the following paragraphs.

In addition, the Low Frequency Auxiliary Oscillator (LFAO) can be used instead of the main oscillator to reduce power consumption in RUN and WAIT modes.

3.5.1 WAIT Mode

The MCU goes into WAIT mode as soon as the WAIT instruction is executed. The microcontroller can be considered as being in a "software frozen" state where the core stops processing the program instructions, the RAM contents and peripheral registers are preserved as long as the power supply voltage is higher than the RAM retention voltage. In this mode the peripherals are still active.

WAIT mode can be used when the user wants to reduce the MCU power consumption during idle periods, while not losing track of time or the capability of monitoring external events. The active oscillator (main oscillator or LFAO) is not stopped in order to provide a clock signal to the peripherals. Timer counting may be enabled as well as the Timer interrupt, before entering the WAIT mode: this allows the WAIT mode to be exited when a Timer interrupt occurs. The same applies to other peripherals which use the clock signal.

If the power consumption has to be further reduced, the Low Frequency Auxiliary Oscillator (LFAO) can be used in place of the main oscillator, if its operating frequency is lower. If required, the LFAO must be switched on before entering the WAIT mode.

If the WAIT mode is exited due to a Reset (either by activating the external pin or generated by the Watchdog), the MCU enters a normal reset procedure. If an interrupt is generated during WAIT mode, the MCU's behaviour depends on the state of the processor core prior to the WAIT instruction, but also on the kind of interrupt request which is generated. This is described in the following paragraphs. The processor core does not generate a delay following the occurrence of the interrupt, because the oscillator clock is still available and no stabilisation period is necessary.

3.5.2 STOP Mode

If the Watchdog is disabled, STOP mode is available. When in STOP mode, the MCU is placed in the lowest power consumption mode. In this operating mode, the microcontroller can be considered as being "frozen", no instruction is executed, the oscillator is stopped, the RAM contents and peripheral registers are preserved as long as the power supply voltage is higher than the RAM retention voltage, and the ST62xx core waits for the occurrence of an external interrupt request or a Reset to exit the STOP state.

If the STOP state is exited due to a Reset (by activating the external pin) the MCU will enter a normal reset procedure. Behaviour in response to interrupts depends on the state of the processor core prior to issuing the STOP instruction, and also on the kind of interrupt request that is generated.

This case will be described in the following paragraphs. The processor core generates a delay after occurrence of the interrupt request, in order to wait for complete stabilisation of the oscillator, before executing the first instruction.

POWER SAVING MODE (Cont'd)

3.5.3 Exit from WAIT and STOP Modes

The following paragraphs describe how the MCU exits from WAIT and STOP modes, when an interrupt occurs (not a Reset). It should be noted that the restart sequence depends on the original state of the MCU (normal, interrupt or non-maskable interrupt mode) prior to entering WAIT or STOP mode, as well as on the interrupt type.

Interrupts do not affect the oscillator selection, consequently, when the LFAO is used, the user program must manage oscillator selection as soon as normal RUN mode is resumed.

3.5.3.1 Normal Mode

If the MCU was in the main routine when the WAIT or STOP instruction was executed, exit from Stop or Wait mode will occur as soon as an interrupt occurs; the related interrupt routine is executed and, on completion, the instruction which follows the STOP or WAIT instruction is then executed, providing no other interrupts are pending.

3.5.3.2 Non Maskable Interrupt Mode

If the STOP or WAIT instruction has been executed during execution of the non-maskable interrupt routine, the MCU exits from the Stop or Wait mode as soon as an interrupt occurs: the instruction which follows the STOP or WAIT instruction is executed, and the MCU remains in non-maskable interrupt mode, even if another interrupt has been generated.

3.5.3.3 Normal Interrupt Mode

If the MCU was in interrupt mode before the STOP or WAIT instruction was executed, it exits from STOP or WAIT mode as soon as an interrupt occurs. Nevertheless, two cases must be considered:

– If the interrupt is a normal one, the interrupt routine in which the WAIT or STOP mode was entered will be completed, starting with the execution of the instruction which follows the STOP or the WAIT instruction, and the MCU is still in the interrupt mode. At the end of this routine pending interrupts will be serviced in accordance with their priority.

– In the event of a non-maskable interrupt, the non-maskable interrupt service routine is processed first, then the routine in which the WAIT or STOP mode was entered will be completed by executing the instruction following the STOP or WAIT instruction. The MCU remains in normal interrupt mode.

Notes:

To achieve the lowest power consumption during RUN or WAIT modes, the user program must take care of:

– configuring unused I/Os as inputs without pull-up (these should be externally tied to well defined logic levels);

– placing all peripherals in their power down modes before entering STOP mode;

– selecting the Low Frequency Auxiliary Oscillator (provided this runs at a lower frequency than the main oscillator).

When the hardware activated Watchdog is selected, or when the software Watchdog is enabled, the STOP instruction is disabled and a WAIT instruction will be executed in its place.

If all interrupt sources are disabled (GEN low), the MCU can only be restarted by a Reset. Although setting GEN low does not mask the NMI as an interrupt, it will stop it generating a wake-up signal.

The WAIT and STOP instructions are not executed if an enabled interrupt request is pending.

7929237 0080014 357

4 ON-CHIP PERIPHERALS

4.1 I/O PORTS

The MCU features 9 Input/Output lines which may be individually programmed as any of the following input or output configurations:

- Input without pull-up or interrupt

- Input with pull-up and interrupt

- Input with pull-up, but without interrupt

- Push-pull output

- Standard Open drain output

- 20mA Open drain output (PA0-PA3 only)

The lines are organized as two Ports (A and B).

Each port is associated with 3 registers in Data space. Each bit of these registers is associated with a particular line (for instance, bits 0 of Port A Data, Direction and Option registers are associated with the PA0 line of Port A).

The two DATA registers (DRA and DRB), are used to read the voltage level values of the lines which have been configured as inputs, or to write the logic value of the signal to be output on the lines configured as outputs. The port data regis-

ters can be read to get the effective logic levels of the pins, but they can be also written by user software, in conjunction with the related option registers, to select the different input mode options.

Single-bit operations on I/O registers are possible but care is necessary because reading in input mode is done from I/O pins while writing will directly affect the Port data register causing an undesired change of the input configuration.

The two Data Direction registers (DDRA and DDRB) allow the data direction (input or output) of each pin to be set.

The two Option registers (ORA and ORB) are used to select the different port options available both in input and in output mode.

All I/O registers can be read or written to just as any other RAM location in Data space, so no extra RAM cells are needed for port data storage and manipulation. During MCU initialization, all I/O registers are cleared and the input mode with pull-ups and no interrupt generation is selected for all the pins, thus avoiding pin conflicts.

Figure 23. I/O Port Block Diagram
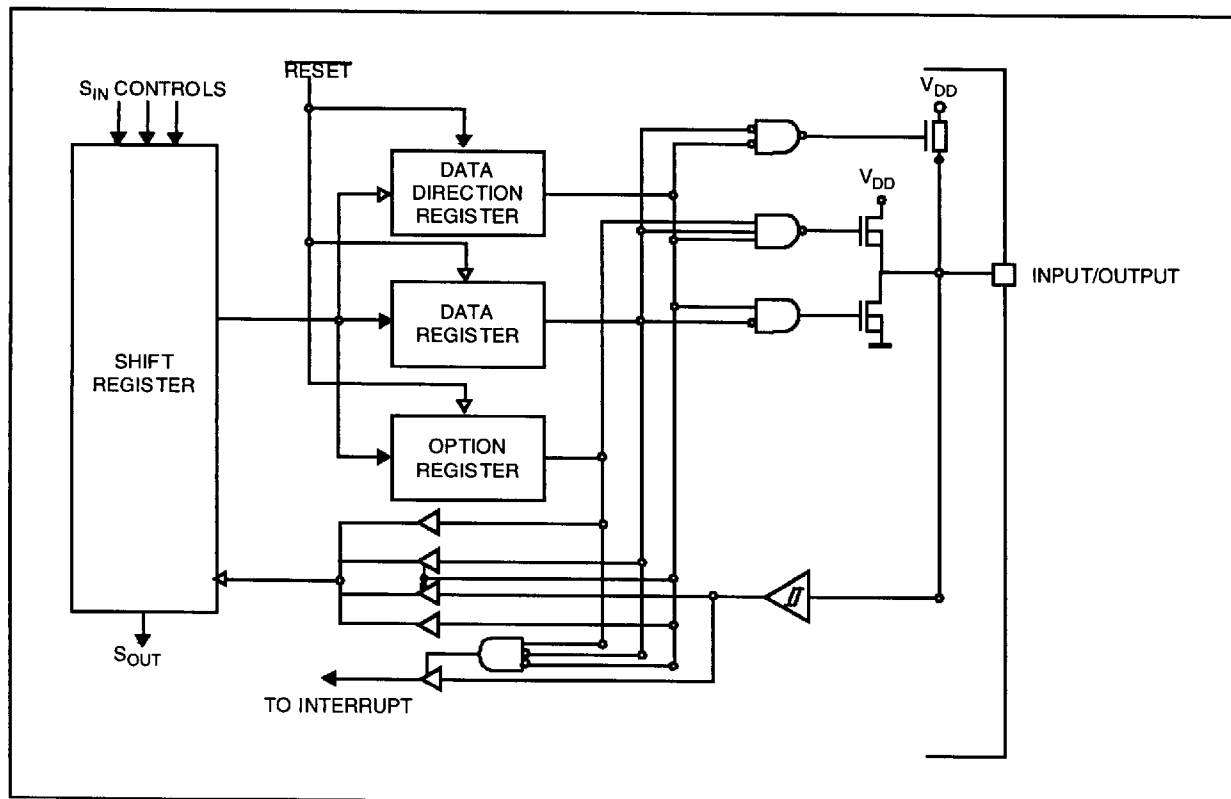
I/O PORTS (Cont'd)

4.1.1 Operating Modes

Each pin may be individually programmed as input or output with various configurations (except for PB0 on devices with the EXTERNAL STOP MODE CONTROL option).

This is achieved by writing the relevant bit in the Data (DR), Data Direction (DDR) and Option registers (OR). Table 7 illustrates the various port configurations which can be selected by user software.

4.1.1.1 Input Options

Pull-up, High Impedance Option. All input lines can be individually programmed with or without an internal pull-up by programming the OR and DR registers accordingly. If the pull-up option is not selected, the input pin will be in the high-impedance state.

4.1.1.2 Interrupt Options

All input lines can be individually connected by software to the interrupt system by programming the OR and DR registers accordingly. The pins of Port A are AND-connected to the interrupt associated with Vector #1. The pins of Port B are AND-connected to the interrupt associated with Vector #2. The interrupt trigger modes (falling edge, rising edge and low level) can be selected by software for each port by programming the IOR register accordingly.

4.1.2 I/O Port Option Registers

ORA/B (CCh PA, CDh PB)
Read/Write

7							0
PA7/P B7	PA6/P B6	PA5/P B5	PA4/P B4	PA3/P B3	PA2/P B2	PA1/P B1	PA0/P B0

Bit 7-0 = **PA/PB7. PA/PB0:** *Port A, B Option Register bits.*

4.1.3 I/O Port Data Direction Registers

DDRA/B (C4h PA, C5h PB)
Read/Write

7							0
PA7/P B7	PA6/P B6	PA5/P B5	PA4/P B4	PA3/P B3	PA2/P B2	PA1/P B1	PA0/P B0

Bit 7-0 = **PA/PB7. PA/PB0:** *Port A, B Data Direction Registers bits.*

4.1.4 I/O Port Data Registers

DRA/B (C0h PA, C1h PB)
Read/Write

7							0
PA7/P B7	PA6/P B6	PA5/P B5	PA4/P B4	PA3/P B3	PA2/P B2	PA1/P B1	PA0/P B0

Bit 7-0 = **PA/PB7. PA/PB0:** *Port A, B Data Registers bits.*

Table 7. I/O Port Option Selection

DDR	OR	DR	Mode	Option
0	0	0	Input	With pull-up, no interrupt (Reset state)
0	0	1	Input	No pull-up, no interrupt
0	1	0	Input	With pull-up and with interrupt
0	1	1		Reserved
1	0	X	Output	20mA sink open-drain output (PA1-PA3 pins)
1	0	X	Output	Standard open-drain output (PB0, PB1, PB3, PB5-PB7 pins)
1	1	X	Output	20mA sink push-pull output (PA1-PA3 pins)

Note: X = Don't care

■ 7929237 0080016 12T ■

I/O PORTS (Cont'd)

4.1.5 Safe I/O State Switching Sequence

Switching the I/O ports from one state to another should be done in a sequence which ensures that no unwanted side effects can occur. The recommended safe transitions are illustrated in Figure 24. All other transitions are potentially risky and should be avoided when changing the I/O operating mode, as it is most likely that undesirable side-effects will be experienced, such as spurious interrupt generation or two pins shorted together by the analog multiplexer.

Single bit instructions (SET, RES, INC and DEC) should be used with great caution on Ports A and B Data registers, since these instructions make an implicit read and write back of the entire register. In port input mode, however, the data register reads from the input pins directly, and not from the data register latches. Since data register information in input mode is used to set the characteristics of the input pin (interrupt, pull-up, analog input), these may be unintentionally reprogrammed depending on the state of the input pins. As a general rule, it is better to limit the use of single bit instructions on data registers to when the whole port

is in output mode. In the case of inputs or of mixed inputs and outputs, it is advisable to keep a copy of the data register in RAM. Single bit instructions may then be used on the RAM copy, after which the whole copy register can be written to the port data register:

```
SET bit, datacopy
LD a, datacopy
LD DRA, a
```

Care must also be taken to not use INC or DEC instructions on a port register when the 8 bits are not available on the devices.

The WAIT and STOP instructions allow the ST62xx to be used in situations where low power consumption is needed. The lowest power consumption is achieved by configuring I/Os in input mode with well-defined logic levels.

The user must take care not to switch outputs with heavy loads during the conversion of one of the analog inputs in order to avoid any disturbance to the conversion.

Figure 24. Diagram showing Safe I/O State Transitions
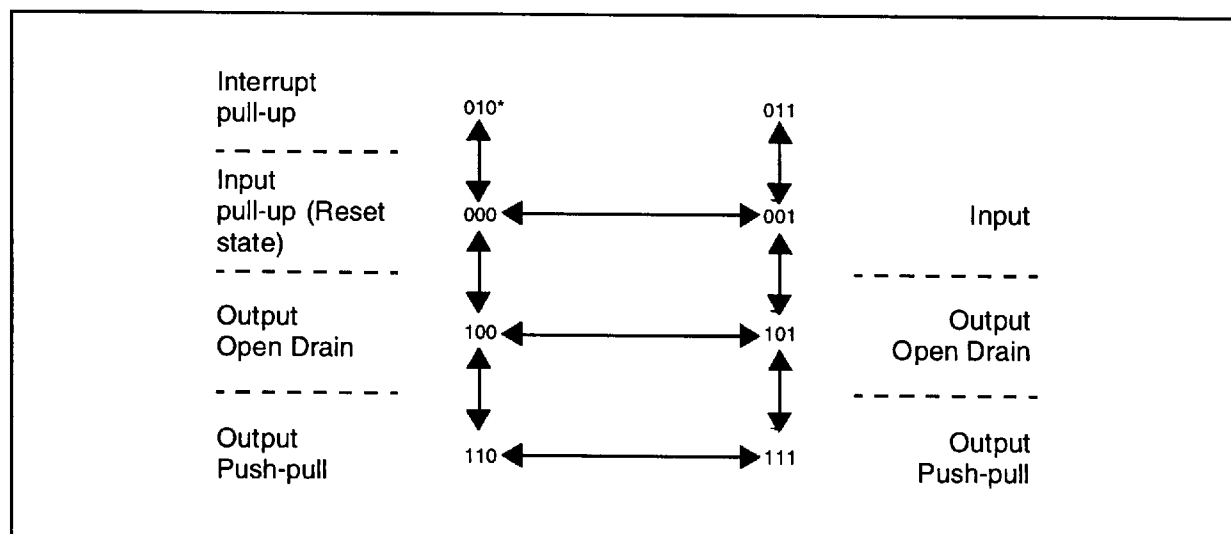
Note *. xxx = DDR, OR, DR Bits respectively

I/O PORTS (Cont'd)

Table 8. I/O Port Option Selections

MODE	AVAILABLE ON(1)	SCHEMATIC
Input	PA1-PA3 PB0, PB1, PB3, PB5-PB7	
Input with pull up	PA1-PA3 PB0, PB1, PB3, PB5-PB7	
Input with pull up with interrupt	PA1-PA3 PB0, PB1, PB3, PB5-PB7	
Open drain output 5mA	PB0, PB1, PB3, PB5-PB7	
Open drain output 20mA	PA1-PA3	
Push-pull output 5mA	PB0, PB1, PB3, PB5-PB7	
Push-pull output 20mA	PA1-PA3	

Note 1. Provided the correct configuration has been selected.

7929237 0080018 TT2

4.2 TIMER

The MCU features an on-chip Timer peripheral, consisting of an 8-bit counter with a 7-bit programmable prescaler, giving a maximum count of 2^{15}.

Figure 25 shows the Timer Block Diagram. The content of the 8-bit counter can be read/written in the Timer/Counter register, TCR, which can be addressed in Data space as a RAM location at address 0D3h. The state of the 7-bit prescaler can be read in the PSC register at address 0D2h. The control logic device is managed in the TSCR register as described in the following paragraphs.

The 8-bit counter is decrement by the output (rising edge) coming from the 7-bit prescaler and can be loaded and read under program control. When it decrements to zero then the TMZ (Timer Zero)bit in the TSCR is set. If the ETI (Enable Timer Interrupt) bit in the TSCR is also set, an interrupt request is generated. The Timer interrupt can be used to exit the MCU from WAIT mode.

The prescaler input is the internal frequency (f_{INT}) divided by 12. The prescaler decrements on the rising edge. Depending on the division factor programmed by PS2, PS1 and PS0 bits in the TSCR (see Table 9), the clock input of the timer/counter register is multiplexed to different sources. For division factor 1, the clock input of the prescaler is also that of timer/counter; for factor 2, bit 0 of the prescaler register is connected to the clock input of TCR. This bit changes its state at half the frequency of the prescaler input clock. For factor 4, bit 1 of the PSC is connected to the clock input of TCR, and so forth. The prescaler initialize bit, PSI, in the TSCR register must be set to allow the prescaler (and hence the counter) to start. If it is cleared, all the prescaler bits are set and the counter is inhibited from counting. The prescaler can be loaded with any value between 0 and 7Fh, if bit PSI is set. The prescaler tap is selected by means of the PS2/PS1/PS0 bits in the control register.

Figure 26 illustrates the Timer's working principle.

Figure 25. Timer Block Diagram

VR02070A
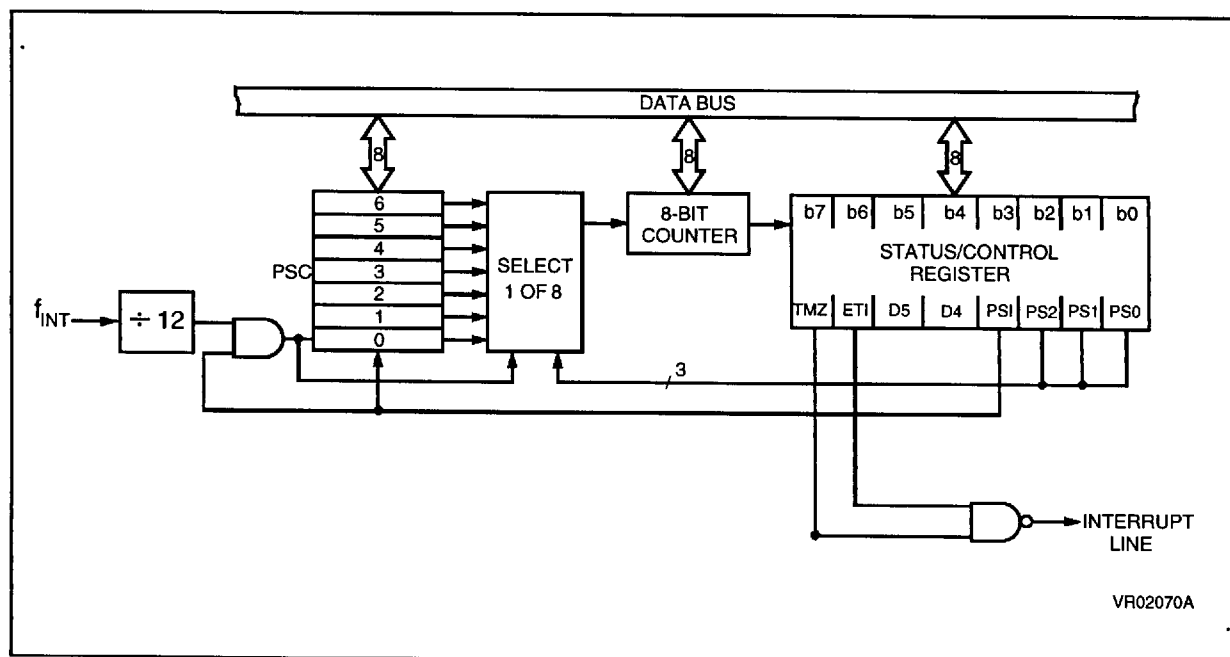
TIMER (Cont'd)

4.2.1 Timer Operation

The Timer prescaler is clocked by the prescaler clock input ($f_{INT} \div 12$).

The user can select the desired prescaler division ratio through the PS2, PS1, PS0 bits. When the TCR count reaches 0, it sets the TMZ bit in the TSCR. The TMZ bit can be tested under program control to perform a timer function whenever it goes high.

4.2.2 Timer Interrupt

When the counter register decrements to zero with the ETI (Enable Timer Interrupt) bit set to one, an interrupt request associated with Interrupt Vector #3 is generated. When the counter decrements

to zero, the TMZ bit in the TSCR register is set to one.

4.2.3 Application Notes

TMZ is set when the counter reaches zero; however, it may also be set by writing 00h in the TCR register or by setting bit 7 of the TSCR register. The TMZ bit must be cleared by user software when servicing the timer interrupt to avoid undesired interrupts when leaving the interrupt service routine. After reset, the 8-bit counter register is loaded with 0FFh, while the 7-bit prescaler is loaded with 07Fh, and the TSCR register is cleared. This means that the Timer is stopped (PSI="0") and the timer interrupt is disabled.

Figure 26. Timer Working Principle

VA00186

■ 7929237 0080020 650 ■
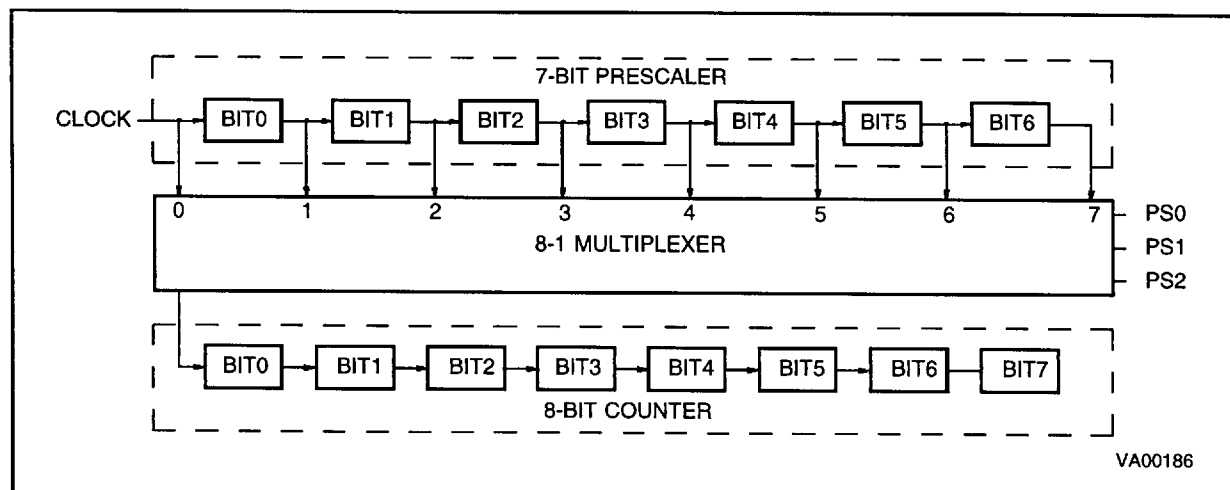
TIMER (Cont'd)

A write to the TCR register will predominate over the 8-bit counter decrement to 00h function, i.e. if a write and a TCR register decrement to 00h occur simultaneously, the write will take precedence, and the TMZ bit is not set until the 8-bit counter reaches 00h again. The values of the TCR and the PSC registers can be read accurately at any time.

4.2.4 Timer Registers

Timer Status Control Register (TSCR)

Address: 0D4h — Read/Write

7							0
TMZ	ETI	D5	D4	PSI	PS2	PS1	PS0

Bit 7 = **TMZ**: *Timer Zero bit*

A low-to-high transition indicates that the timer count register has decrement to zero. This bit must be cleared by user software before starting a new count.

Bit 6 = **ETI**: *Enable Timer Interrup*

When set, enables the timer interrupt request (vector #3). If ETI=0 the timer interrupt is disabled. If ETI=1 and TMZ=1 an interrupt request is generated.

Bit 5 = **D5**: *Reserved*

Must be set to "1".

Bit 4 = **D4**

Do not care.

Bit 3 = **PSI**: *Prescaler Initialize Bit*

Used to initialize the prescaler and inhibit its counting. When PSI="0" the prescaler is set to 7Fh and the counter is inhibited. When PSI="1" the prescaler is enabled to count downwards. As long as PSI="0" both counter and prescaler are not running.

Bit 2, 1, 0 = **PS2, PS1, PS0**: *Prescaler Mux. Select.* These bits select the division ratio of the prescaler register.

Table 9. Prescaler Division Factors

PS2	PS1	PS0	Divided by
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Timer Counter Register (TCR)

Address: 0D3h — Read/Write

7							0
D7	D6	D5	D4	D3	D2	D1	D0

Bit 7-0 = **D7-D0**: *Counter Bits.*

Prescaler Register PSC

Address: 0D2h — Read/Write

7							0
D7	D6	D5	D4	D3	D2	D1	D0

Bit 7 = **D7**: Always read as "0".

Bit 6-0 = **D6-D0**: Prescaler Bits.

5 SOFTWARE

5.1 ST6 ARCHITECTURE

The ST6 software has been designed to fully use the hardware in the most efficient way possible while keeping byte usage to a minimum; in short, to provide byte efficient programming capability. The ST6 core has the ability to set or clear any register or RAM location bit of the Data space with a single instruction. Furthermore, the program may branch to a selected address depending on the status of any bit of the Data space. The carry bit is stored with the value of the bit when the SET or RES instruction is processed.

5.2 ADDRESSING MODES

The ST6 core offers nine addressing modes, which are described in the following paragraphs. Three different address spaces are available: Program space, Data space, and Stack space. Program space contains the instructions which are to be executed, plus the data for immediate mode instructions. Data space contains the Accumulator, the X,Y,V and W registers, peripheral and Input/Output registers, the RAM locations and Data ROM locations (for storage of tables and constants). Stack space contains six 12-bit RAM cells used to stack the return addresses for subroutines and interrupts.

Immediate. In the immediate addressing mode, the operand of the instruction follows the opcode location. As the operand is a ROM byte, the immediate addressing mode is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

Direct. In the direct addressing mode, the address of the byte which is processed by the instruction is stored in the location which follows the opcode. Direct addressing allows the user to directly address the 256 bytes in Data Space memory with a single two-byte instruction.

Short Direct The core can address the four RAM registers X,Y,V,W (locations 80h, 81h, 82h, 83h) in the short-direct addressing mode. In this case, the instruction is only one byte and the selection of the location to be processed is contained in the opcode. Short direct addressing is a subset of the direct addressing mode. (Note that 80h and 81h are also indirect registers).

Extended. In the extended addressing mode, the 12-bit address needed to define the instruction is obtained by concatenating the four less significant bits of the opcode with the byte following the opcode. The instructions (JP, CALL) which use the extended addressing mode are able to branch to any address of the 4K bytes Program space.

An extended addressing mode instruction is two-byte long.

Program Counter Relative. The relative addressing mode is only used in conditional branch instructions. The instruction is used to perform a test and, if the condition is true, a branch with a span of -15 to +16 locations around the address of the relative instruction. If the condition is not true, the instruction which follows the relative instruction is executed. The relative addressing mode instruction is one-byte long. The opcode is obtained in adding the three most significant bits which characterize the kind of the test, one bit which determines whether the branch is a forward (when it is 0) or backward (when it is 1) branch and the four less significant bits which give the span of the branch (0h to Fh) which must be added or subtracted to the address of the relative instruction to obtain the address of the branch.

Bit Direct In the bit direct addressing mode, the bit to be set or cleared is part of the opcode, and the byte following the opcode points to the address of the byte in which the specified bit must be set or cleared. Thus, any bit in the 256 locations of Data space memory can be set or cleared.

Bit Test & Branch The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit test and branch instruction is three-byte long. The bit identification and the tested condition are included in the opcode byte. The address of the byte to be tested follows immediately the opcode in the Program space. The third byte is the jump displacement, which is in the range of -126 to +129. This displacement can be determined using a label, which is converted by the assembler.

Indirect In the indirect addressing mode, the byte processed by the register-indirect instruction is at the address pointed by the content of one of the indirect registers, X or Y (80h,81h). The indirect register is selected by the bit 4 of the opcode. A register indirect instruction is one byte long.

Inherent. In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. These instructions are one byte long.

5.3 INSTRUCTION SET

The ST6 core offers a set of 40 basic instructions which, when combined with nine addressing modes, yield 244 usable opcodes. They can be divided into six different types: load/store, arithmetic/logic, conditional branch, control instructions, jump/call, and bit manipulation. The following paragraphs describe the different types.

All the instructions belonging to a given type are presented in individual tables.

Load & Store. These instructions use one, two or three bytes in relation with the addressing mode. One operand is the Accumulator for LOAD and the other operand is obtained from data memory using one of the addressing modes.

For Load Immediate one operand can be any of the 256 data space bytes while the other is always immediate data.

Table 10. Load & Store Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags Z	Flags C
LD A, X	Short Direct	1	4	Δ	*
LD A, Y	Short Direct	1	4	Δ	*
LD A, V	Short Direct	1	4	Δ	*
LD A, W	Short Direct	1	4	Δ	*
LD X, A	Short Direct	1	4	Δ	*
LD Y, A	Short Direct	1	4	Δ	*
LD V, A	Short Direct	1	4	Δ	*
LD W, A	Short Direct	1	4	Δ	*
LD A, rr	Direct	2	4	Δ	*
LD rr, A	Direct	2	4	Δ	*
LD A, (X)	Indirect	1	4	Δ	*
LD A, (Y)	Indirect	1	4	Δ	*
LD (X), A	Indirect	1	4	Δ	*
LD (Y), A	Indirect	1	4	Δ	*
LDI A, #N	Immediate	2	4	Δ	*
LDI rr, #N	Immediate	3	4	*	*

Notes:

X,Y. Indirect Register Pointers, V & W Short Direct Registers

#. Immediate data (stored in ROM memory)

rr. Data space register

Δ. Affected

*. Not Affected

INSTRUCTION SET (Cont'd)

Arithmetic and Logic These instructions are used to perform the arithmetic calculations and logic operations. In AND, ADD, CP, SUB instructions one operand is always the accumulator while the other can be either a data space memory content or an immediate value in relation with the addressing mode. In CLR, DEC, INC instructions the operand can be any of the 256 data space addresses. In COM, RLC, SLA the operand is always the accumulator.

Table 11. Arithmetic & Logic Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags Z	Flags C
ADD A, (X)	Indirect	1	4	Δ	Δ
ADD A, (Y)	Indirect	1	4	Δ	Δ
ADD A, rr	Direct	2	4	Δ	Δ
ADDI A, #N	Immediate	2	4	Δ	Δ
AND A, (X)	Indirect	1	4	Δ	Δ
AND A, (Y)	Indirect	1	4	Δ	Δ
AND A, rr	Direct	2	4	Δ	Δ
ANDI A, #N	Immediate	2	4	Δ	Δ
CLR A	Short Direct	2	4	Δ	Δ
CLR r	Direct	3	4	*	*
COM A	Inherent	1	4	Δ	Δ
CP A, (X)	Indirect	1	4	Δ	Δ
CP A, (Y)	Indirect	1	4	Δ	Δ
CP A, rr	Direct	2	4	Δ	Δ
CPI A, #N	Immediate	2	4	Δ	Δ
DEC X	Short Direct	1	4	Δ	*
DEC Y	Short Direct	1	4	Δ	*
DEC V	Short Direct	1	4	Δ	*
DEC W	Short Direct	1	4	Δ	*
DEC A	Direct	2	4	Δ	*
DEC rr	Direct	2	4	Δ	*
DEC (X)	Indirect	1	4	Δ	*
DEC (Y)	Indirect	1	4	Δ	*
INC X	Short Direct	1	4	Δ	*
INC Y	Short Direct	1	4	Δ	*
INC V	Short Direct	1	4	Δ	*
INC W	Short Direct	1	4	Δ	*
INC A	Direct	2	4	Δ	*
INC rr	Direct	2	4	Δ	*
INC (X)	Indirect	1	4	Δ	*
INC (Y)	Indirect	1	4	Δ	*
RLC A	Inherent	1	4	Δ	Δ
SLA A	Inherent	2	4	Δ	Δ
SUB A, (X)	Indirect	1	4	Δ	Δ
SUB A, (Y)	Indirect	1	4	Δ	Δ
SUB A, rr	Direct	2	4	Δ	Δ
SUBI A, #N	Immediate	2	4	Δ	Δ

Notes:
X,Y.Indirect Register Pointers, V & W Short Direct RegistersD. Affected
. Immediate data (stored in ROM memory)* . Not Affected
rr. Data space register

INSTRUCTION SET (Cont'd)

Conditional Branch. The branch instructions achieve a branch in the program when the selected condition is met.

Bit Manipulation Instructions. These instructions can handle any bit in data space memory. One group either sets or clears. The other group (see Conditional Branch) performs the bit test branch operations.

Control Instructions. The control instructions control the MCU operations during program execution.

Jump and Call. These two instructions are used to perform long (12-bit) jumps or subroutines call inside the whole program space.

Table 12. Conditional Branch Instructions

Instruction	Branch If	Bytes	Cycles	Flags	
				Z	C
JRC e	C = 1	1	2	*	*
JRNC e	C = 0	1	2	*	*
JRZ e	Z = 1	1	2	*	*
JRNZ e	Z = 0	1	2	*	*
JRR b, rr, ee	Bit = 0	3	5	*	Δ
JRS b, rr, ee	Bit = 1	3	5	*	Δ

Notes:
b.   3-bit address
e.   5 bit signed displacement in the range -15 to +16<F128M>
ee. 8 bit signed displacement in the range -126 to +129

rr. Data space register
Δ.   Affected. The tested bit is shifted into carry.
*.   Not Affected

Table 13. Bit Manipulation Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
SET b,rr	Bit Direct	2	4	*	*
RES b,rr	Bit Direct	2	4	*	*

Notes:
b.   3-bit address;
rr. Data space register;

*.   Not<M> Affected

Table 14. Control Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
NOP	Inherent	1	2	*	*
RET	Inherent	1	2	*	*
RETI	Inherent	1	2	Δ	Δ
STOP (1)	Inherent	1	2	*	*
WAIT	Inherent	1	2	*	*

Notes:
1.   This instruction is deactivated<N>and a WAIT is automatically executed instead of a STOP if the watchdog function is selected.
Δ.   Affected
*.   Not Affected

Table 15. Jump & Call Instructions

Instruction	Addressing Mode	Bytes	Cycles	Flags	
				Z	C
CALL abc	Extended	2	4	*	*
JP abc	Extended	2	4	*	*

Notes:
abc. 12-bit address;
*.   Not Affected

Opcode Map Summary.

The following table contains an opcode map for the instructions used by the ST6

HI \ LOW	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111	LOW HI
0 0000	2 JRNZ e / 1 pcr	4 CALL abc / 2 ext	2 JRNC e / 1 pcr	5 JRR b0,rr,ee / 3 bt	2 JRZ e / 1 pcr	#	2 JRC e / 1 prc	4 LD a,(x) / 1 ind	0 0000
1 0001	2 JRNZ e / 1 pcr	4 CALL abc / 2 ext	2 JRNC e / 1 pcr	5 JRS b0,rr,ee / 3 bt	2 JRZ e / 1 pcr	4 INC x / 1 sd	2 JRC e / 1 prc	4 LDI a,nn / 2 imm	1 0001
2 0010	2 JRNZ e / 1 pcr	4 CALL abc / 2 ext	2 JRNC e / 1 pcr	5 JRR b4,rr,ee / 3 bt	2 JRZ e / 1 pcr	#	2 JRC e / 1 prc	4 CP a,(x) / 1 ind	2 0010
3 0011	2 JRNZ e / 1 pcr	4 CALL abc / 2 ext	2 JRNC e / 1 pcr	5 JRS b4,rr,ee / 3 bt	2 JRZ e / 1 pcr	4 LD a,x / 1 sd	2 JRC e / 1 prc	4 CPI a,nn / 2 imm	3 0011
4 0100	2 JRNZ e / 1 pcr	4 CALL abc / 2 ext	2 JRNC e / 1 pcr	5 JRR b2,rr,ee / 3 bt	2 JRZ e / 1 pcr	#	2 JRC e / 1 prc	4 ADD a,(x) / 1 ind	4 0100
5 0101	2 JRNZ e / 1 pcr	4 CALL abc / 2 ext	2 JRNC e / 1 pcr	5 JRS b2,rr,ee / 3 bt	2 JRZ e / 1 pcr	4 INC y / 1 sd	2 JRC e / 1 prc	4 ADDI a,nn / 2 imm	5 0101
6 0110	2 JRNZ e / 1 pcr	4 CALL abc / 2 ext	2 JRNC e / 1 pcr	5 JRR b6,rr,ee / 3 bt	2 JRZ e / 1 pcr	#	2 JRC e / 1 prc	4 INC (x) / 1 ind	6 0110
7 0111	2 JRNZ e / 1 pcr	4 CALL abc / 2 ext	2 JRNC e / 1 pcr	5 JRS b6,rr,ee / 3 bt	2 JRZ e / 1 pcr	4 LD a,y / 1 sd	2 JRC e / 1 prc	#	7 0111
8 1000	2 JRNZ e / 1 pcr	4 CALL abc / 2 ext	2 JRNC e / 1 pcr	5 JRR b1,rr,ee / 3 bt	2 JRZ e / 1 pcr	#	2 JRC e / 1 prc	4 LD (x),a / 1 ind	8 1000
9 1001	2 RNZ e / 1 pcr	4 CALL abc / 2 ext	2 JRNC e / 1 pcr	5 JRS b1,rr,ee / 3 bt	2 JRZ e / 1 pcr	4 INC v / 1 sd	2 JRC e / 1 prc	#	9 1001
A 1010	2 JRNZ e / 1 pcr	4 CALL abc / 2 ext	2 JRNC e / 1 pcr	5 JRR b5,rr,ee / 3 bt	2 JRZ e / 1 pcr	#	2 JRC e / 1 prc	4 AND a,(x) / 1 ind	A 1010
B 1011	2 JRNZ e / 1 pcr	4 CALL abc / 2 ext	2 JRNC e / 1 pcr	5 JRS b5,rr,ee / 3 bt	2 JRZ e / 1 pcr	4 LD a,v / 1 sd	2 JRC e / 1 prc	4 ANDI a,nn / 2 imm	B 1011
C 1100	2 JRNZ e / 1 pcr	4 CALL abc / 2 ext	2 JRNC e / 1 pcr	5 JRR b3,rr,ee / 3 bt	2 JRZ e / 1 pcr	#	2 JRC e / 1 prc	4 SUB a,(x) / 1 ind	C 1100
D 1101	2 JRNZ e / 1 pcr	4 CALL abc / 2 ext	2 JRNC e / 1 pcr	5 JRS b3,rr,ee / 3 bt	2 JRZ e / 1 pcr	4 INC w / 1 sd	2 JRC e / 1 prc	4 SUBI a,nn / 2 imm	D 1101
E 1110	2 JRNZ e / 1 pcr	4 CALL abc / 2 ext	2 JRNC e / 1 pcr	5 JRR b7,rr,ee / 3 bt	2 JRZ e / 1 pcr	#	2 JRC e / 1 prc	4 DEC (x) / 1 ind	E 1110
F 1111	2 JRNZ e / 1 pcr	4 CALL abc / 2 ext	2 JRNC e / 1 pcr	5 JRS b7,rr,ee / 3 bt	2 JRZ e / 1 pcr	4 LD a,w / 1 sd	2 JRC e / 1 prc	#	F 1111

Abbreviations for Addressing Modes:

dir	Direct
sd	Short Direct
imm	Immediate
inh	Inherent
ext	Extended
b.d	Bit Direct
bt	Bit Test
pcr	Program Counter Relative
ind	Indirect

Legend:

#	Indicates Illegal Instructions
e	5 Bit Displacement
b	3 Bit Address
rr	1 byte dataspace address
nn	1 byte immediate data
abc	12 bit address
ee	8 bit Displacement

Cycle — 2 JRC — Mnemonic
Operand — e
Bytes — 1 prc
Addressing Mode

7929237 0080026 079

ST6203B
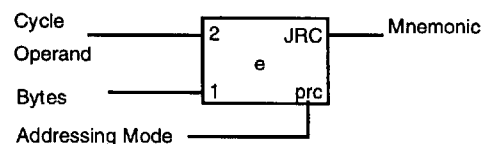
Opcode Map Summary (Continued)

HI \ LOW	8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	LOW \ HI
0 0000	2 JRNZ / e / 1 pcr	4 JP / abc / 2 ext	2 JRNC / e / 1 pcr	4 RES / b0,rr / 2 b.d	2 JRZ / e / 1 pcr	4 LDI / rr,nn / 3 imm	2 JRC / e / 1 prc	4 LD / a,(y) / 1 ind	**0** 0000
1 0001	2 JRNZ / e / 1 pcr	4 JP / abc / 2 ext	2 JRNC / e / 1 pcr	4 SET / b0,rr / 2 b.d	2 JRZ / e / 1 pcr	4 DEC / x / 1 sd	2 JRC / e / 1 prc	4 LD / a,rr / 2 dir	**1** 0001
2 0010	2 JRNZ / e / 1 pcr	4 JP / abc / 2 ext	2 JRNC / e / 1 pcr	4 RES / b4,rr / 2 b.d	2 JRZ / e / 1 pcr	4 COM / a	2 JRC / e / 1 prc	4 CP / a,(y) / 1 ind	**2** 0010
3 0011	2 JRNZ / e / 1 pcr	4 JP / abc / 2 ext	2 JRNC / e / 1 pcr	4 SET / b4,rr / 2 b.d	2 JRZ / e / 1 pcr	4 LD / x,a / 1 sd	2 JRC / e / 1 prc	4 CP / a,rr / 2 dir	**3** 0011
4 0100	2 JRNZ / e / 1 pcr	4 JP / abc / 2 ext	2 JRNC / e / 1 pcr	4 RES / b2,rr / 2 b.d	2 JRZ / e / 1 pcr	2 RETI / 1 inh	2 JRC / e / 1 prc	4 ADD / a,(y) / 1 ind	**4** 0100
5 0101	2 JRNZ / e / 1 pcr	4 JP / abc / 2 ext	2 JRNC / e / 1 pcr	4 SET / b2,rr / 2 b.d	2 JRZ / e / 1 pcr	4 DEC / y / 1 sd	2 JRC / e / 1 prc	4 ADD / a,rr / 2 dir	**5** 0101
6 0110	2 JRNZ / e / 1 pcr	4 JP / abc / 2 ext	2 JRNC / e / 1 pcr	4 RES / b6,rr / 2 b.d	2 JRZ / e / 1 pcr	2 STOP / 1 inh	2 JRC / e / 1 prc	4 INC / (y) / 1 ind	**6** 0110
7 0111	2 JRNZ / e / 1 pcr	4 JP / abc / 2 ext	2 JRNC / e / 1 pcr	4 SET / b6,rr / 2 b.d	2 JRZ / e / 1 pcr	4 LD / y,a / 1 sd	2 JRC / e / 1 prc	4 INC / rr / 2 dir	**7** 0111
8 1000	2 JRNZ / e / 1 pcr	4 JP / abc / 2 ext	2 JRNC / e / 1 pcr	4 RES / b1,rr / 2 b.d	2 JRZ / e / 1 pcr	#	2 JRC / e / 1 prc	4 LD / (y),a / 1 ind	**8** 1000
9 1001	2 RNZ / e / 1 pcr	4 JP / abc / 2 ext	2 JRNC / e / 1 pcr	4 SET / b1,rr / 2 b.d	2 JRZ / e / 1 pcr	4 DEC / v / 1 sd	2 JRC / e / 1 prc	4 LD / rr,a / 2 dir	**9** 1001
A 1010	2 JRNZ / e / 1 pcr	4 JP / abc / 2 ext	2 JRNC / e / 1 pcr	4 RES / b5,rr / 2 b.d	2 JRZ / e / 1 pcr	4 RCL / a / 1 inh	2 JRC / e / 1 prc	4 AND / a,(y) / 1 ind	**A** 1010
B 1011	2 JRNZ / e / 1 pcr	4 JP / abc / 2 ext	2 JRNC / e / 1 pcr	4 SET / b5,rr / 2 b.d	2 JRZ / e / 1 pcr	4 LD / v,a / 1 sd	2 JRC / e / 1 prc	4 AND / a,rr / 2 dir	**B** 1011
C 1100	2 JRNZ / e / 1 pcr	4 JP / abc / 2 ext	2 JRNC / e / 1 pcr	4 RES / b3,rr / 2 b.d	2 JRZ / e / 1 pcr	2 RET / 1 inh	2 JRC / e / 1 prc	4 SUB / a,(y) / 1 ind	**C** 1100
D 1101	2 JRNZ / e / 1 pcr	4 JP / abc / 2 ext	2 JRNC / e / 1 pcr	4 SET / b3,rr / 2 b.d	2 JRZ / e / 1 pcr	4 DEC / w / 1 sd	2 JRC / e / 1 prc	4 SUB / a,rr / 2 dir	**D** 1101
E 1110	2 JRNZ / e / 1 pcr	4 JP / abc / 2 ext	2 JRNC / e / 1 pcr	4 RES / b7,rr / 2 b.d	2 JRZ / e / 1 pcr	2 WAIT / 1 inh	2 JRC / e / 1 prc	4 DEC / (y) / 1 ind	**E** 1110
F 1111	2 JRNZ / e / 1 pcr	4 JP / abc / 2 ext	2 JRNC / e / 1 pcr	4 SET / b7,rr / 2 b.d	2 JRZ / e / 1 pcr	4 LD / w,a / 1 sd	2 JRC / e / 1 prc	4 DEC / rr / 2 dir	**F** 1111

Abbreviations for Addressing Modes:

dir	Direct
sd	Short Direct
imm	Immediate
inh	Inherent
ext	Extended
b.d	Bit Direct
bt	Bit Test
pcr	Program Counter Relative
ind	Indirect

Legend:

#	Indicates Illegal Instructions
e	5 Bit Displacement
b	3 Bit Address
rr	1byte dataspace address
nn	1 byte immediate data
abc	12 bit address
ee	8 bit Displacement

Cycle — 2 JRC — Mnemonic
Operand — e
Bytes — 1 prc
Addressing Mode
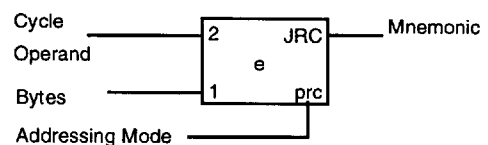
6 ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

This product contains devices to protect the inputs against damage due to high static voltages, however it is advisable to take normal precaution to avoid application of any voltage higher than the specified maximum rated voltages.

For proper operation it is recommended that V_I and V_O be higher than V_{SS} and lower than V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriate logic voltage level (V_{DD} or V_{SS}).

Power Considerations. The average chip-junction temperature, Tj, in Celsius can be obtained from:

$$Tj = TA + PD \times RthJA$$

Where: TA = Ambient Temperature.

RthJA = Package thermal resistance (junction-to ambient).

PD = Pint + Pport.

Pint = IDD x VDD (chip internal power).

Pport = Port power dissipation (determined by the user).

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to 7.0	V
V_I	Input Voltage	VSS - 0.3 to VDD + 0.3[1]	V
V_O	Output Voltage	VSS - 0.3 to VDD + 0.3[1]	V
I_O	Current Drain per Pin Excluding VDD, VSS	10	mA
I_{INJ+}	Pin Injection current (positive), All I/O, VDD = 4.5V	+5	mA
I_{INJ-}	Pin Injection current (negative), All I/O, VDD = 4.5V	-5	mA
IV_{DD}	Total Current into VDD (source)	50[2]	mA
IV_{SS}	Total Current out of VSS (sink)	50[2]	mA
T_j	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-60 to 150	°C

Notes:

- Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

- (1) Within these limits, clamping diodes are guarantee to be not conductive. Voltages outside these limits are authorised as long as injection current is kept within the specification.

(2) The total current through ports A and B combined may not exceed 50mA. If the application is designed with care and observing the limits stated above, total current may reach 50mA.

THERMAL CHARACTERISTIC

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
RthJA	Thermal Resistance	PDIP20			60	°C/W
		PSO20			80	

■ 7929237 0080028 941 ■

6.2 RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
T_A	Operating Temperature	6 Suffix Version 1 Suffix Version	-40 0		85 70	°C
V_{DD}	Operating Supply Voltage		3.0V		6.0V	V
V_{PP}	Programming Voltage		12	12.5	13	V
I_{INJ+}	Pin Injection Current (positive) Digital Input	$V_{DD} = 4.5$ to 5.5V			+5	mA
I_{INJ-}	Pin Injection Current (negative) Digital Input	$V_{DD} = 4.5$ to 5.5V			-5	mA

Figure 27. Maximum Operating FREQUENCY (Fmax) Versus SUPPLY VOLTAGE (V_{DD})
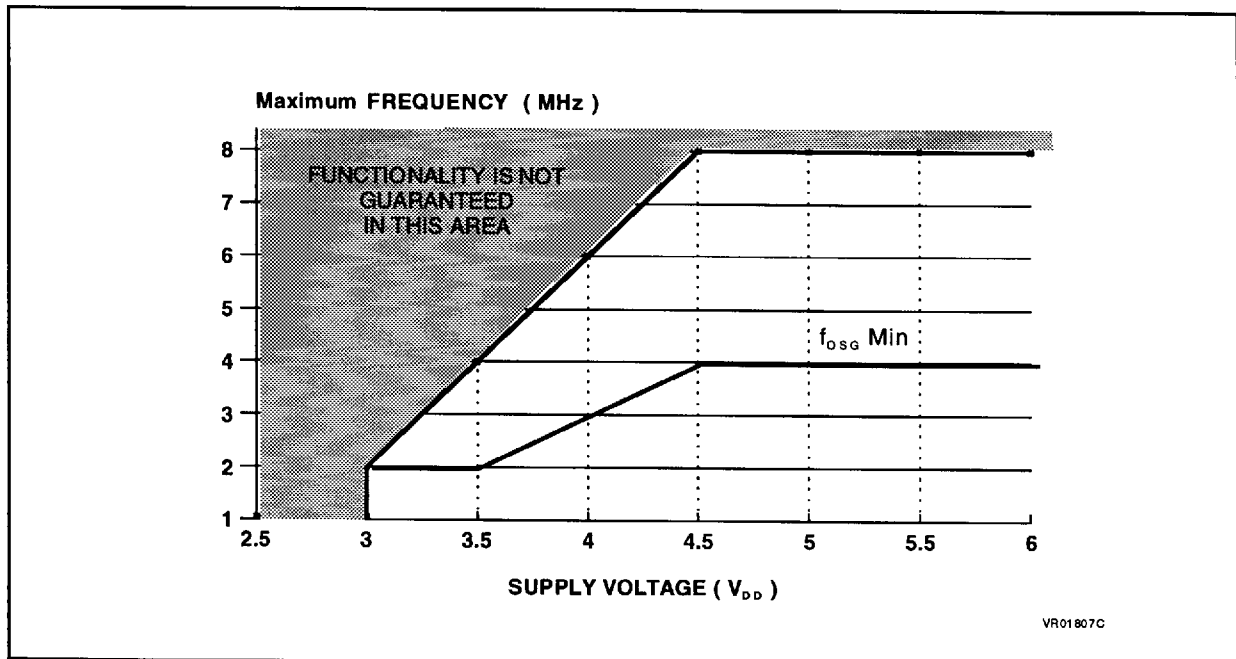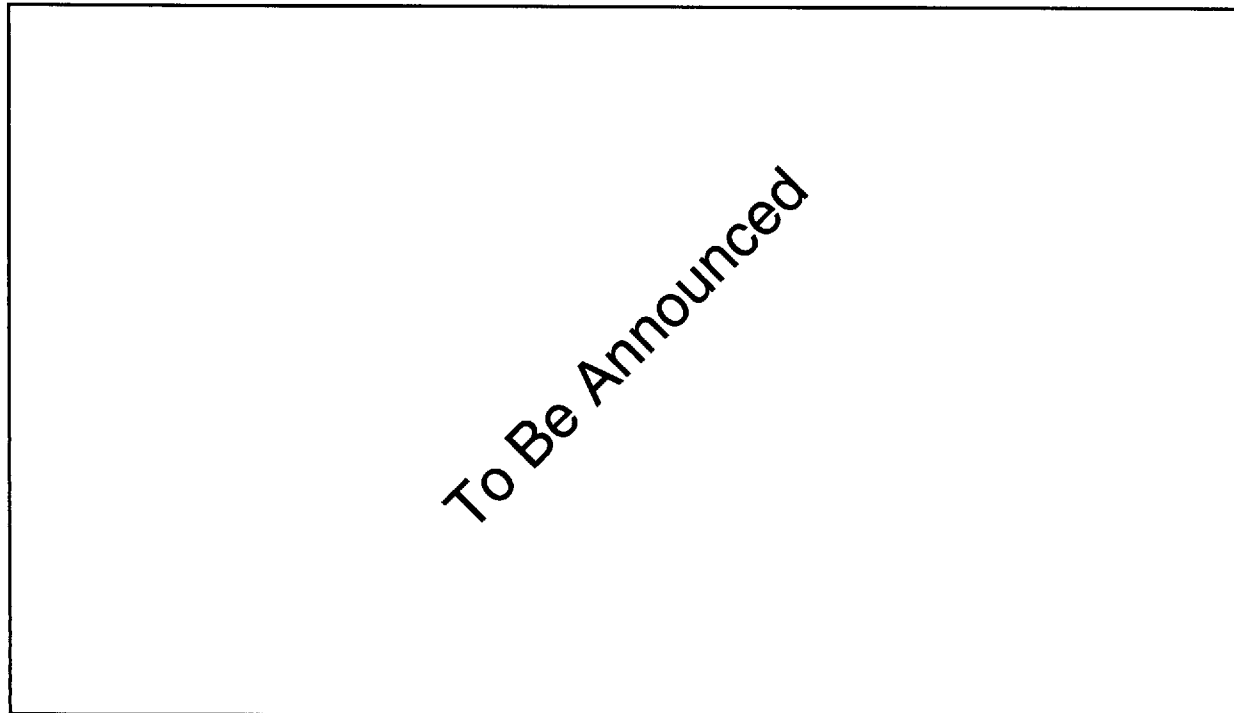

The shaded area is outside the recommended operating range; device functionality is not guaranteed under these conditions.

Figure 28. RC Oscillator. F$_{INT}$ versus RNET (Indicative Values)
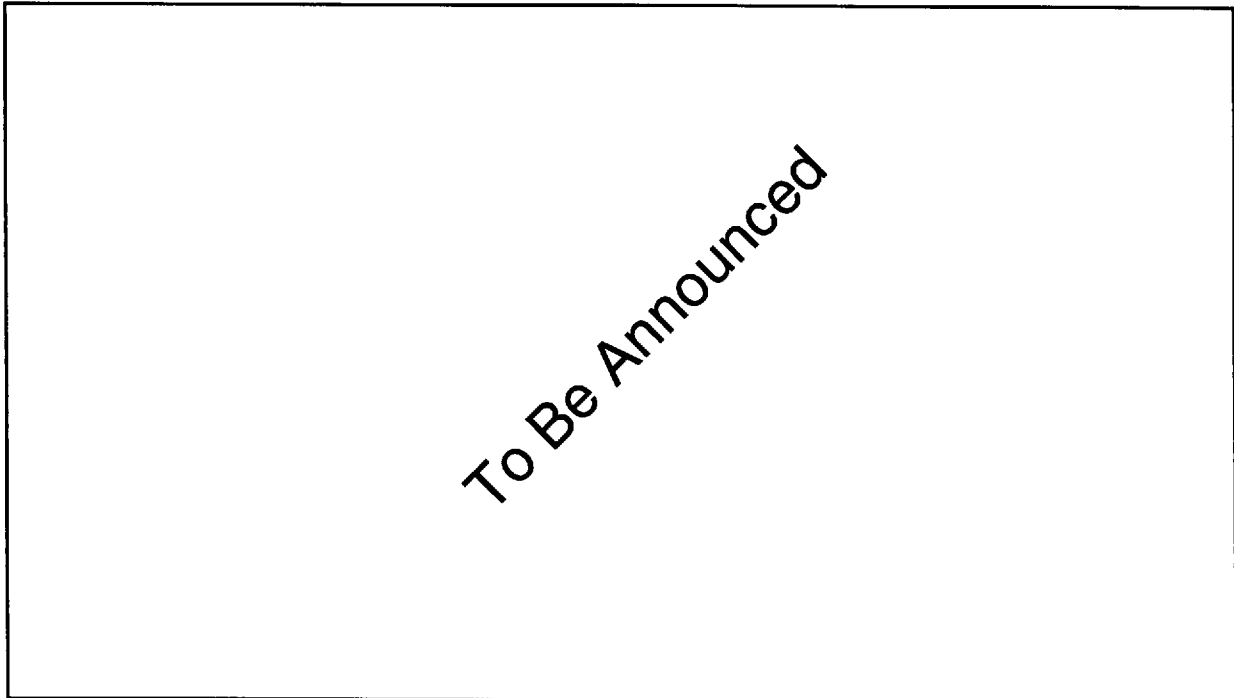
To Be Announced

The shaded area is outside the recommended operating range; device functionality is not guaranteed under these conditions.

**Figure 29. RC Oscillator. F$_{INT}$ versus RNET (Indicative Values)**

To Be Announced

The shaded area is outside the recommended operating range; device functionality is not guaranteed under these conditions.

7929237 0080030 5TT

6.3 READOUT PROTECTION FUSE

If the ROM READOUT PROTECTION option is selected, the waveform illustrated below must be applied to the TEST pin in order to blow the fuse.
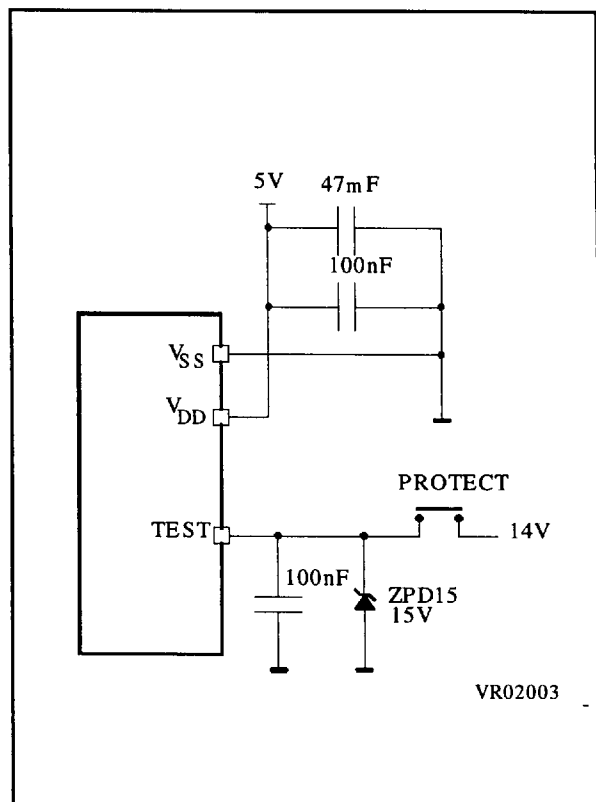
The following circuit can be used for this purpose:

Figure 30. Programming wave form

VR02001
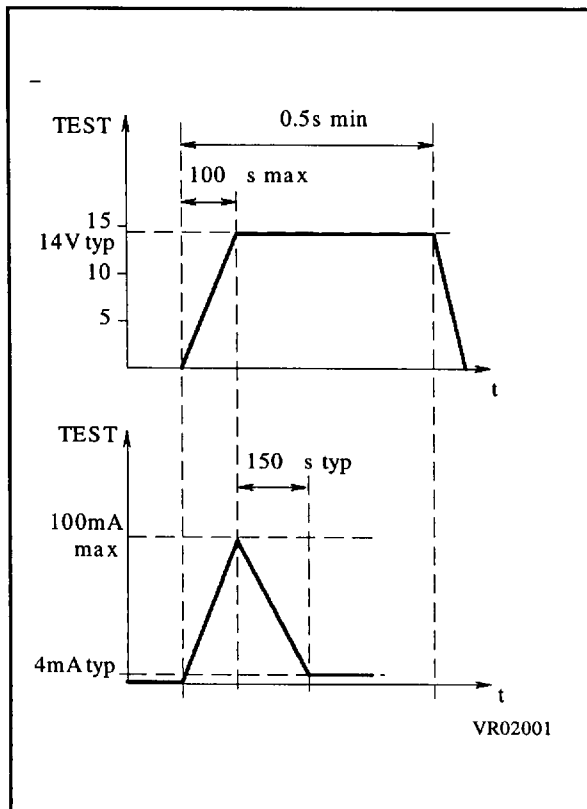
Note: ZPD15 is used for overvoltage protection

Figure 31. Programming Circuit

VR02003

7 GENERAL INFORMATION

7.1 PACKAGE MECHANICAL DATA

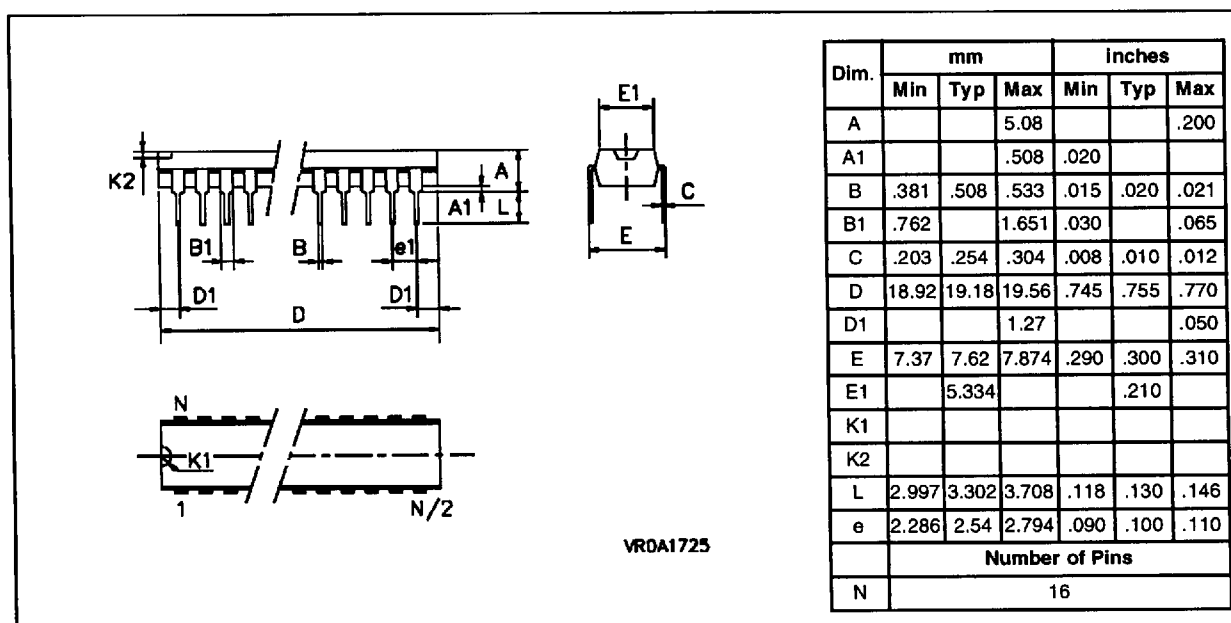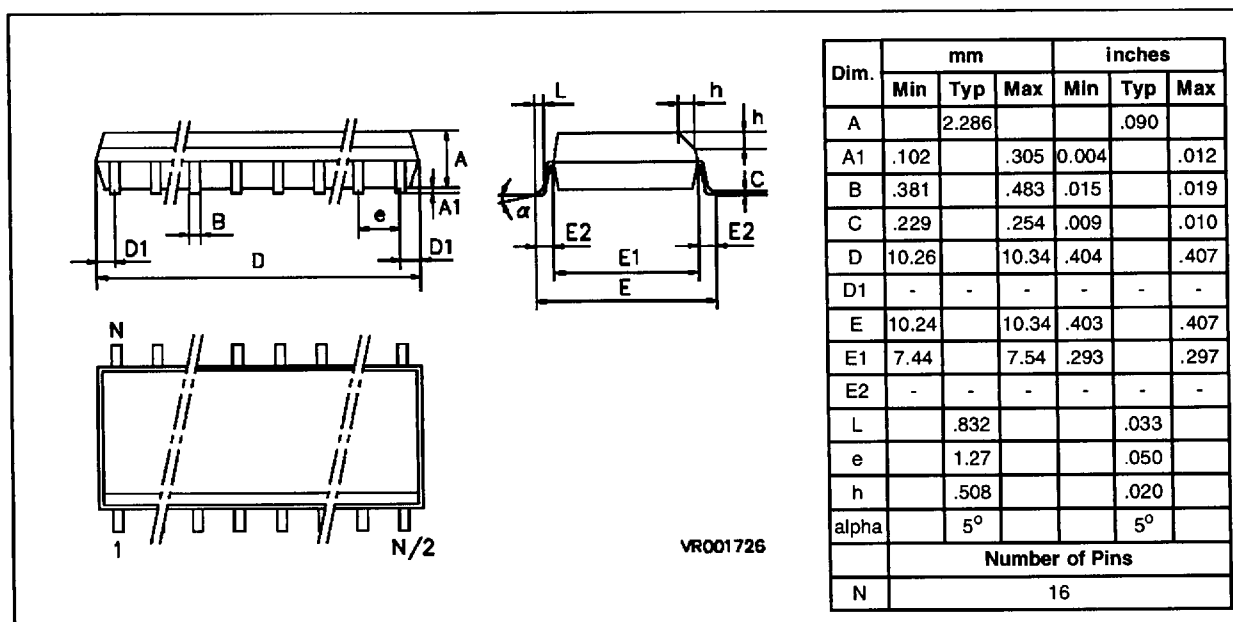**Figure 32. 16-Pin Plastic Dual In Line Package (B), 300-mil Width**

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			5.08			.200
A1			.508	.020		
B	.381	.508	.533	.015	.020	.021
B1	.762		1.651	.030		.065
C	.203	.254	.304	.008	.010	.012
D	18.92	19.18	19.56	.745	.755	.770
D1			1.27			.050
E	7.37	7.62	7.874	.290	.300	.310
E1		5.334			.210	
K1						
K2						
L	2.997	3.302	3.708	.118	.130	.146
e	2.286	2.54	2.794	.090	.100	.110
	Number of Pins					
N	16					

VR0A1725

Figure 33. 16-Pin Plastic Small Outline Package (M), 300-mil Width

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A		2.286			.090	
A1	.102		.305	0.004		.012
B	.381		.483	.015		.019
C	.229		.254	.009		.010
D	10.26		10.34	.404		.407
D1	-	-	-	-	-	-
E	10.24		10.34	.403		.407
E1	7.44		7.54	.293		.297
E2	-	-	-	-	-	-
L		.832			.033	
e		1.27			.050	
h		.508			.020	
alpha		5°			5°	
	Number of Pins					
N	16					

VR001726

■ 7929237 0080032 372 ■

ST6203B MICROCONTROLLER OPTION LIST

Customer
Address

Contact
Phone No
Reference

SGS-THOMSON Microelectronics references
Device: [ ] ST6203B
Package: [ ] Dual in Line Plastic[ ] Small Outline Plastic
                     In this case, select conditioning
                     [ ] Standard (Stick)
                     [ ] Tape & Reel
Temperature Range: [ ] 0°C to + 70°C[ ] - 40°C to + 85°C
Special Marking: [ ] No
                     [ ] Yes "_ _ _ _ _ _ _ _ _ _"
Authorized characters are letters, digits, '.', '-', '/' and spaces only.
Maximum character count:DIP20: 9
                     SO20: 6
Oscillator Source Selection[ ] Crystal Quartz/Ceramic resonator (Default)
                     [ ] RC Network
Watchdog Selection: [ ] Software Activation (STOP mode available)
                     [ ] Hardware Activation (no STOP mode)
OSG: [ ] Enabled
                     [ ] Disabled (Default)
Input pull-up selection on NMI pin[ ] Yes[ ] No
ROM Readout Protection:[ ] Standard (Fuse cannot be blown)
                     [ ] Enabled (Fuse can be blown by the customer)
Note: No part is delivered with protected ROM.
                     The fuse must be blown for protection to be effective.
External STOP Mode Contro[ ] Enabled[ ] Disabled (Default)
Comments :
Supply Operating Range in the application:
Oscillator Fequency in the application:
Notes

Signature
Date

7.2 ORDERING INFORMATION

The following section deals with the procedure for transfer of customer codes to SGS-THOMSON.

7.2.1 Transfer of Customer Code

Customer code is made up of the ROM contents and the list of the selected mask options. The ROM contents are to be sent on diskette, or by electronic means, with the hexadecimal file generated by the development tool. All unused bytes must be set to FFh.

The selected mask options are communicated to SGS-THOMSON using the correctly filled OP-TION LIST appended.

7.2.2 Listing Generation and Verification

When SGS-THOMSON receives the user's ROM contents, a computer listing is generated from it. This listing refers exactly to the mask which will be used to produce the specified MCU. The listing is then returned to the customer who must thoroughly check, complete, sign and return it to SGS-THOMSON. The signed listing forms a part of the contractual agreement for the creation of the specific customer mask.

The SGS-THOMSON Sales Organization will be pleased to provide detailed information on contractual points.

Table 16. ROM Memory Map for ST6203B

Device Address	Description
0000h-0B9Fh	Reserved
0BA0h-0F9Fh	User ROM
0FA0h-0FEFh	Reserved
0FF0h-0FF7h	Interrupt Vectors
0FF8h-0FFBh	Reserved
0FFCh-0FFDh	NMI Interrupt Vector
0FFEh-0FFFh	Reset Vector

Table 17. Ordering Information

Sales Type	ROM	I/O	Temperature Range	Package
ST6203BB1/XXX ST6203BB6/XXX	1036 Bytes	9	0 to +70°C -40 to + 85°C	PDIP16
ST6203BM1/XXX ST6203BM6/XXX			0 to +70°C -40 to + 85°C	PSO16

■ 7929237 0080034 145 ■