

SONY**CXP87200A****CMOS 8-bit Single Chip Microcomputer****Piggyback/
evaluator type****Description**

The CXP87200A is a CMOS 8-bit single chip microcomputer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP87240A/87248A.

Features

- A wide instruction set (213 instructions) which cover various types of data.
 - 16-bit operation/multiplication and division/boolean bit operation instructions

- Minimum instruction cycle
 - 333ns at 12MHz operation (3.0 to 5.5V)
 - 250ns at 16MHz operation (4.5 to 5.5V)
 - 122µs at 32kHz operation

- Applicable EPROM
 - LCC type 27C256, LCC type 27C512
(Maximum 48Kbytes are available.)

- Incorporated RAM capacity
 - 1376 bytes

- Peripheral functions

- A/D converter

8-bit, 12-channel, successive approximation method
(Conversion time of 20µs/16MHz)

Incorporated buffer RAM

(Auto transfer for 1 to 32 bytes), 1 channel

Incorporated 8-bit and 8-stage FIFO

(Auto transfer for 1 to 8 bytes), 1 channel

8-bit timer, 8-bit timer/counter,

19-bit time base timer, 32kHz timer/counter

- High precision timing pattern generator

PPG 19-pin, 32-stage programmable

RTG 5 pins, 2 channels

PWM output 12 bits, 2 channels

(Repetitive frequency 62.5kHz/16MHz)

DA gate pulse output 13 bits, 4 channels

Capstan FG, drum FG/PG, CTL input

- Servo input control

- VSYNC separator

- FRC capture unit

- PWM output

- VISS/VASS circuit

- Remote control receiving circuit

- General purpose prescaler

- HSYNC counter

Incorporated 26-bit and 8-stage FIFO

14 bits, 1 channel

Pulse duty auto detection circuit

8-bit pulse measurement counter with on-chip 6-stage FIFO

7 bits (SYNC1 input frequency division, FRC capture possible)

12-bit event counter (SYNC1 input count)

22 factors, 15 vectors, multi-interruption possible

- Interruption

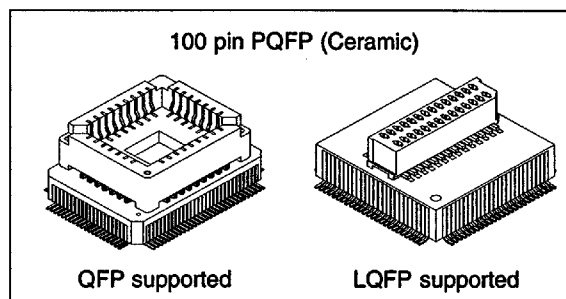
SLEEP/STOP

- Standby mode

- Package

100-pin ceramic PQFP

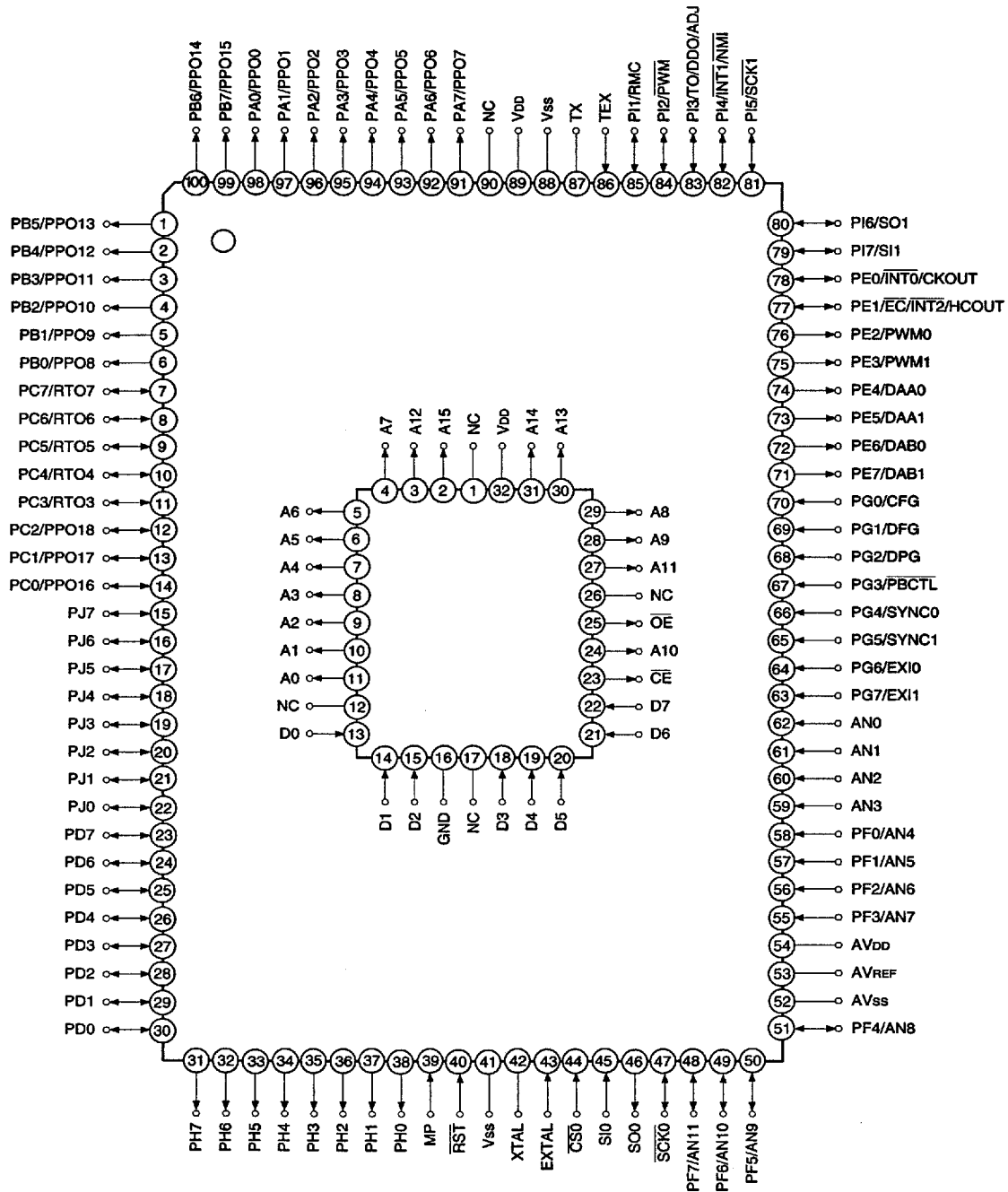
Note) Mask option depends on the type of the CXP87200A. Refer to the Products List for details.

**Structure**

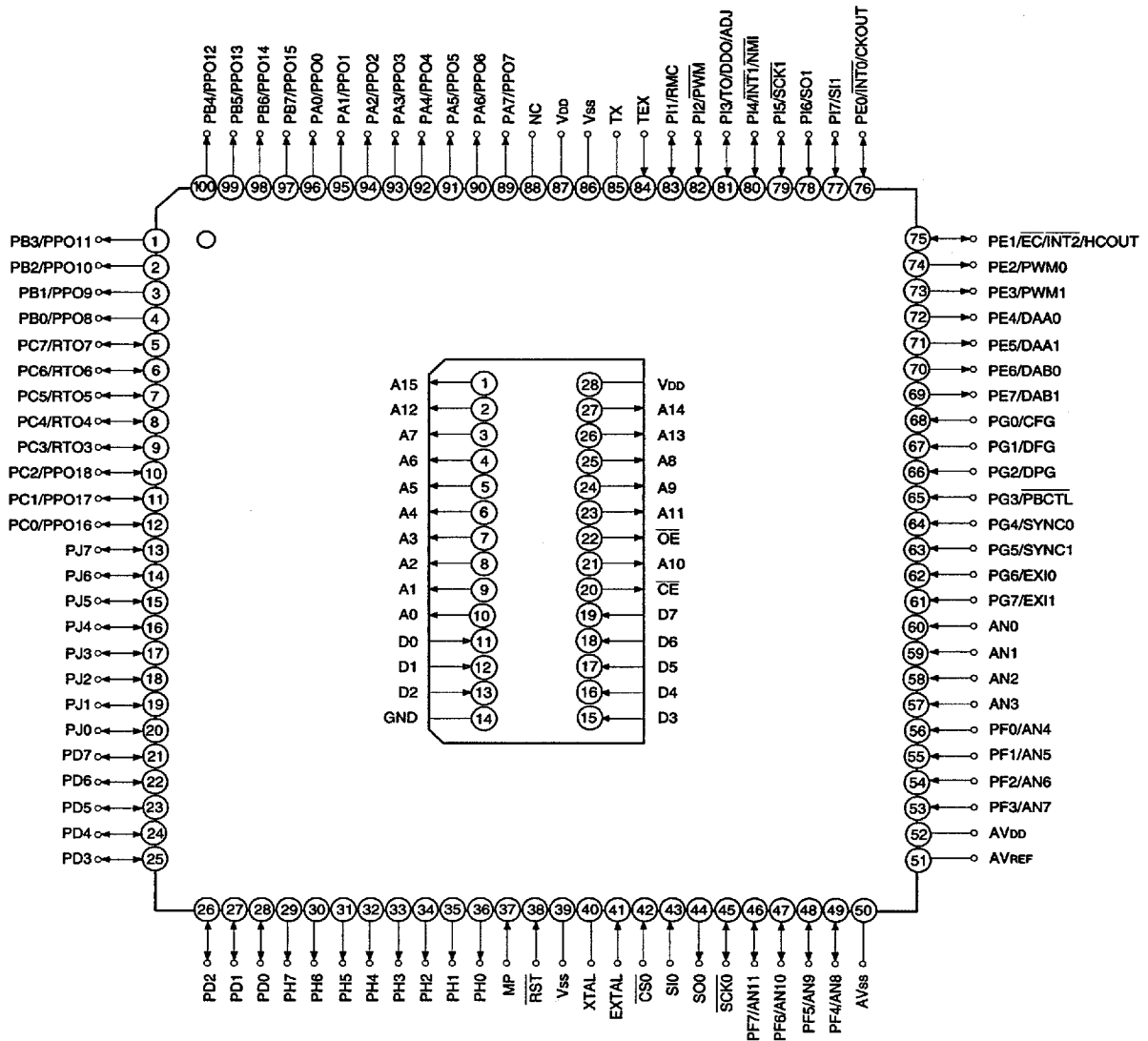
Silicon gate CMOS IC

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Pin Assignment in Piggyback Mode (QFP package)

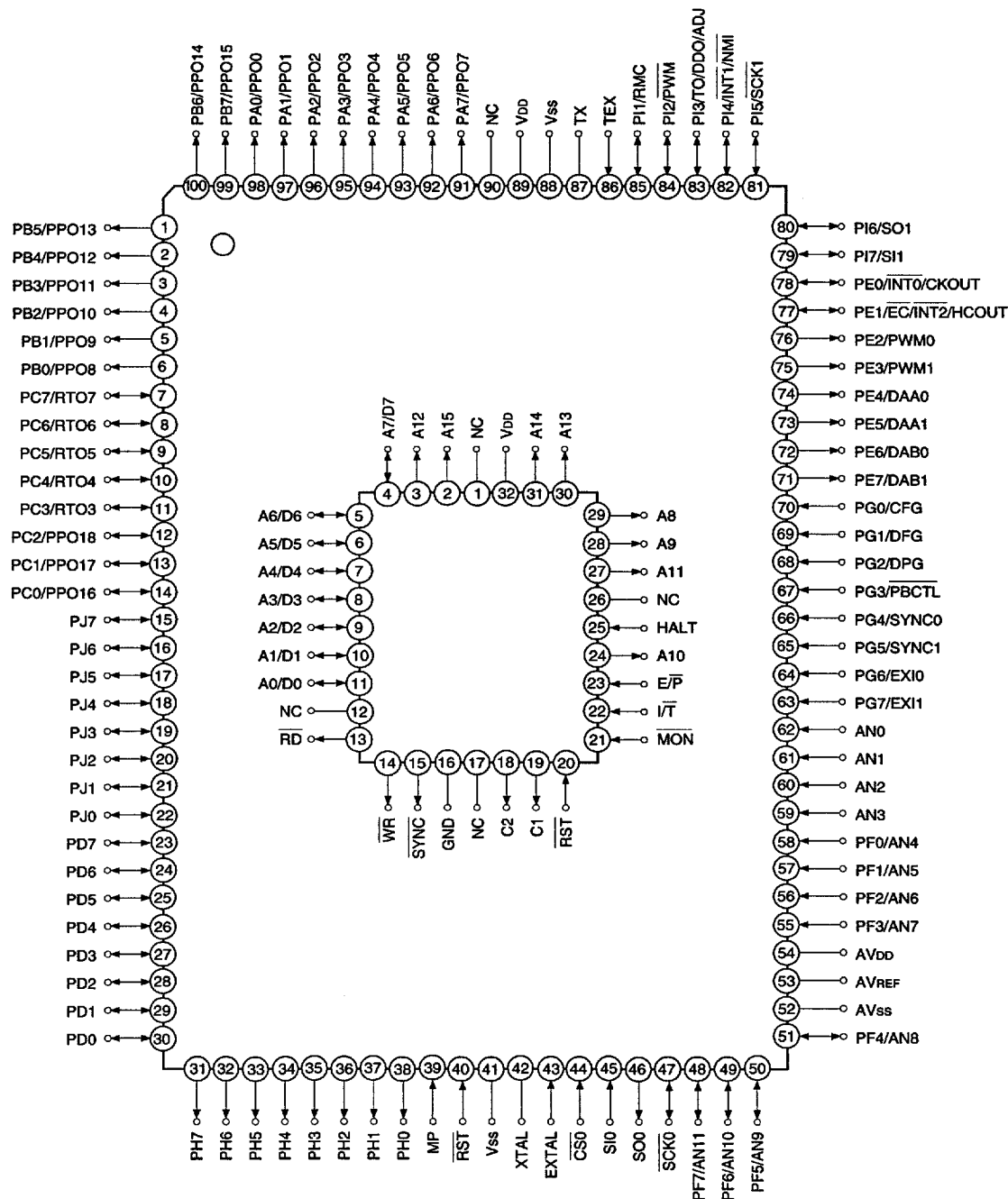


Pin Assignment in Piggyback Mode (LQFP package)



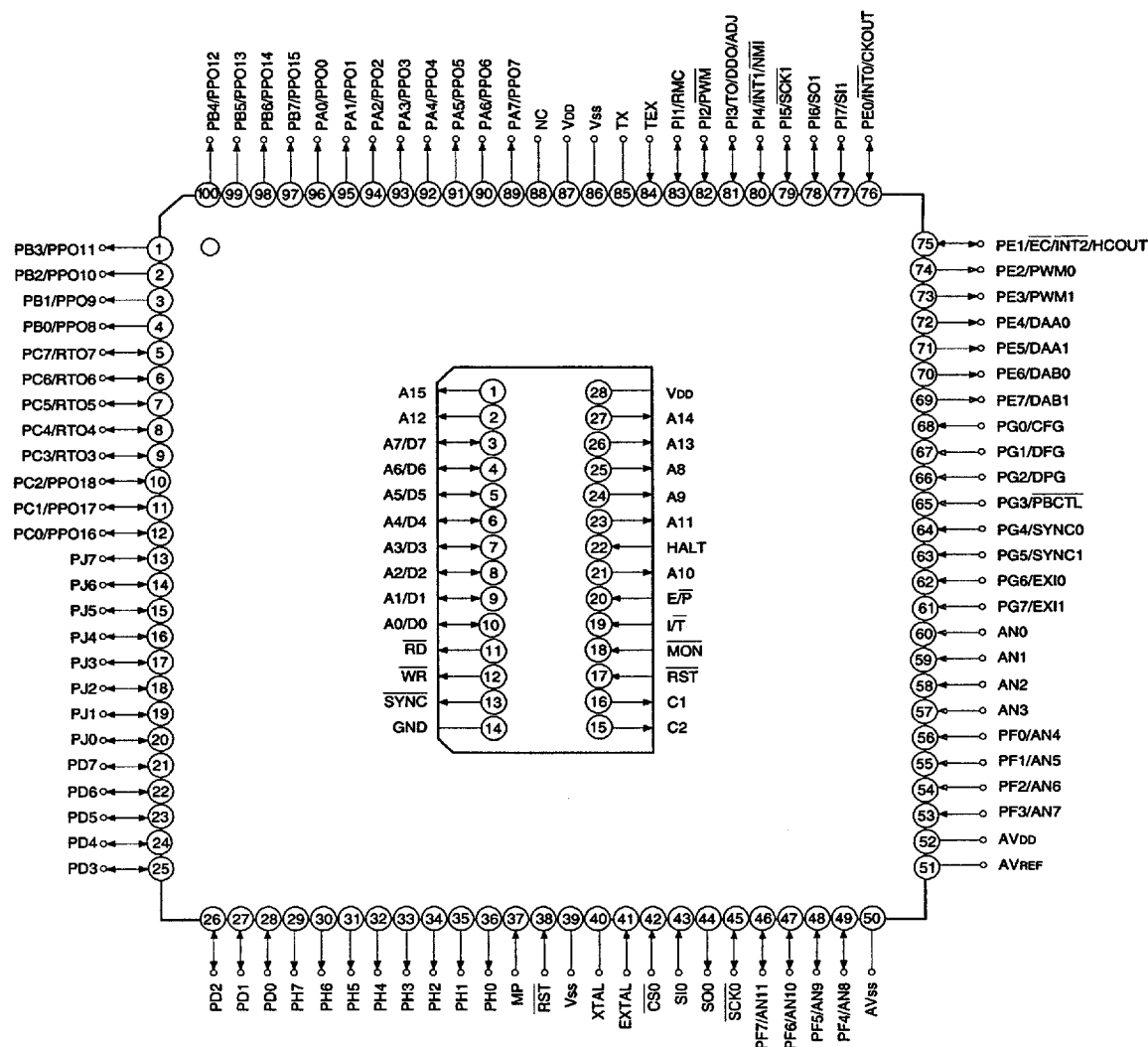
- Note)**
1. NC (Pin 88) is always connected to VDD.
 2. VSS (Pins 39 and 86) are both connected to GND.
 3. MP (Pin 37) is always connected to GND.

Pin Assignment in Evaluator Mode (QFP package)



- Note)** 1. NC (Pin 90) is always connected to VDD.
2. VSS (Pins 41 and 88) are both connected to GND.
3. MP (Pin 39) is always connected to GND.

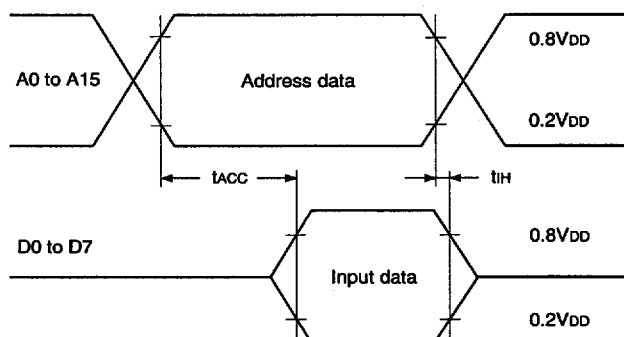
Pin Assignment in Evaluator Mode (LQFP package)



- Note)** 1. NC (Pin 88) is always connected to VDD.
 2. Vss (Pins 39 and 86) are both connected to GND.
 3. MP (Pin 37) is always connected to GND.

EPROM Read Timing ($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 3.0$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pin	Min.	Max.	Unit
Address → data input delay time	t_{ACC}	A0 to A15 D0 to D7		100*1	ns
				75*2	
Address → data hold time	t_{IH}	A0 to A15 D0 to D7	0		ns

*1 At 12MHz operation ($V_{DD} = 4.5$ to 5.5V)*2 At 12MHz operation ($V_{DD} = 3.0$ to 5.5V), At 16MHz operation ($V_{DD} = 4.5$ to 5.5V)**Products List**

Option item	Products			
	Mask product		Piggyback/evaluator product	
	CXP87240A	CXP87248A	CXP87200A-U01Q CXP87200A-U01R	CXP87200A-U02R
Package	100-pin plastic QFP/LQFP		100-pin ceramic PQFP	
ROM capacity	40Kbytes	48Kbytes	EPROM 48Kbytes	
			27C512 × 1	27C256 × 2
Pull-up resistor for reset pin	Existent/Non-existent		Existent	
Input circuit format*1	CMOS schmitt/TTL schmitt		TTL schmitt	CMOS schmitt

*1 On PG4/SYNC0 pin and PG5/SYNC1 pin, the input circuit format can be selected to every pin.

Piggyback mode/evaluator mode can be switched as shown below.

