CYPRESS SEMICONDUCTOR

ADVANCED INFORMATION

CY7B175
CY7B176

32K x 16 Synchronous Cache R/W RAM

Features

- **Supports 66-MHz cache systems with zero wait states**
- **Available in PQFP with 25-mil lead pitch**
- **Supports 3.3V I/O logic levels**
- **BiCMOS for optimum speed/power**
- **9-ns access delay (clock to output)**
- **Two-bit wraparound counter supporting the 486/Pentium burst sequence (7B175)**
- **Two-bit wraparound counter supporting the linear burst sequence (7B176)**
- **Separate address strobes from processor and from cache controller**
- **Synchronous self-timed write**
- **Direct interface with the processor and external cache controller**
- **Internal clamp diodes**
- **Synchronous chip enable**
- **Asynchronous output enable**

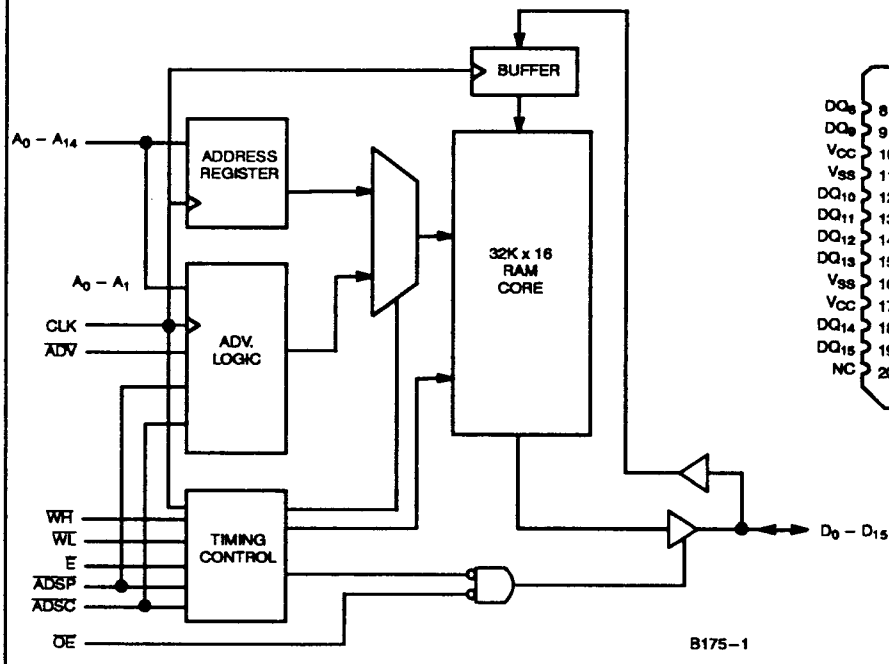
Functional Description

The CY7B175 and CY7B176 are 32K by 16 synchronous cache RAMs designed to interface with high-speed microprocessors with minimum glue logic. Maximum access delay from clock rise is 9 ns. A 2-bit on-chip counter captures the first address in a burst and increments the address automatically for the rest of the burst access.

The CY7B175 is designed for Intel i486/Pentium-based systems; its counter follows the burst sequence of the i486/Pentium. The CY7B176 is architected for other processors with linear burst sequences. Burst accesses can be initiated with the processor address strobe ($\overline{ADSP}$) or the cache controller address strobe ($\overline{ADSC}$) inputs. Address advancement is controlled by the address advancement ($\overline{ADV}$) input.

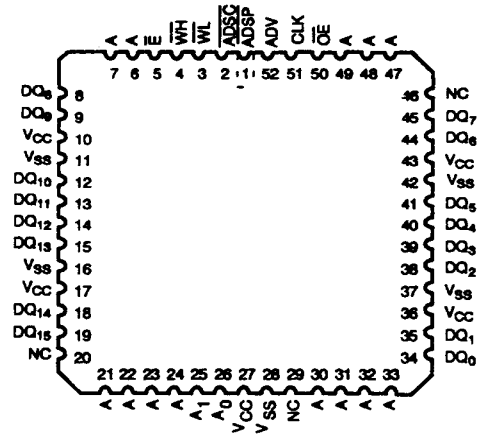
A synchronous self-timed write mechanism is provided to simplify the write interface. The I/O and address pins have internal clamp diodes to limit overshoot and undershoot. Also, the data outputs are prevented from going above 3.3V (V_{OH} max.) by an internal bandgap reference. The part is available in the very small outline Plastic Quad Flat Pack (PQFP).

Logic Block Diagram



Pin Configuration

LCC/PLCC/PQFP
Top View



Selector Guide

		7B175–9 7B176–9	7B175–10 7B176–10	7B175–14 7B176–14
Maximum Access Time (ns)		9	10	14
Maximum Operating Current (mA)	Commercial	210	210	210
	Military		230	230

Pentium is a trademark of Intel Corporation.

Functional Description (continued)

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{E}$ = 0 and (2) $\overline{ADSP}$ is LOW. $\overline{ADSP}$- triggered write cycles are completed in two clock periods. The address at A_0 through A_{14} is loaded into the address advancement logic and delivered to the RAM core. The write signal is ignored in this cycle because the cache tag or other external logic use this clock period to perform address comparisons or protection checks. If the write is allowed to proceed, the write input to the CY7B175 and CY7B176 will be pulled LOW before the next clock rise.

If $\overline{WH}$ or $\overline{WL}$ is LOW at the next clock rise, information presented at D_0 through D_8 will be stored into the location specified by the address advancement logic. Because the CY7B175 and CY7B176 are common-I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the CPU is delivered to D_0 through D_8. As a safety precaution, the data lines (D_0 through D_8) are three-stated in the cycle where $\overline{WH}$ and $\overline{WL}$ is sampled LOW, regardless of the state of the $\overline{OE}$ input.

Single Write Accesses Initiated by $\overline{ADSC}$

This write access is initiated when the following conditions are satisfied at rising edge of the clock: (1) $\overline{E}$ = 0, (2) $\overline{ADSC}$ is LOW, and (3) $\overline{WE}$ is LOW. $\overline{ADSC}$ trigger accesses are completed in a single clock cycle.

The address at A_0 through A_{14} is loaded into the address advancement logic and delivered to the RAM core. Information presented at D_0 through D_8 will be stored into the location specified by the address advancement logic. Since the CY7B175 and CY7B176 are common I/O devices, the output enable signal ($\overline{OE}$) must be deasserted before data from the cache controller is delivered to D_0 through D_8. As a safety precaution, the data lines (D_0 through D_8) are three-stated in the cycle where $\overline{WH}$ and $\overline{WL}$ is sampled LOW regardless of the state of the $\overline{OE}$ input.

Single Read Accesses

A single read access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{E}$ = 0, (2) $\overline{ADSP}$ or $\overline{ADSC}$ is LOW, and (3) $\overline{WE}$ is HIGH. The address at A_0 through A_{14} is stored into the address advancement logic and delivered to the RAM core. If the output enable ($\overline{OE}$) signal is asserted (LOW), data will be available at D_0 through D_8 a maximum of 9 ns after clock rise.

Burst Sequences

The CY7B175 provides a 2-bit wraparound counter implementing the Intel 80486/Pentium sequence (see *Table 1*). Note that the burst sequence depends on the location of the first burst address.

Table 1. Counter Implementation for the Intel 80486/Pentium Sequence

First Address		Second Address		Third Address		Fourth Address	
$A_X + 1$	A_X	$A_X + 1$	A_X	$A_X + 1$	A_X	$A_X + 1$	A_X
0	0	0	1	1	0	1	1
0	1	0	0	1	1	1	0
1	0	1	1	0	0	0	1
1	1	1	0	0	1	0	0

The CY7B176 provides a two-bit wraparound counter implementing a linear sequence (see *Table 2*).

Table 2. Counter Implementation for a Linear Sequence

First Address		Second Address		Third Address		Fourth Address	
$A_X + 1$	A_X	$A_X + 1$	A_X	$A_X + 1$	A_X	$A_X + 1$	A_X
0	0	0	1	1	0	1	1
0	1	1	0	1	1	0	0
1	0	1	1	0	0	0	1
1	1	0	0	0	1	1	0

Application Example

Figure 1 shows a 128-Kbyte secondary cache for the i486 using four CY7B175 cache RAMs and a CY7B181 cache tag. Address from the i486 is checked by the cache tag at the beginning of each access. Match reset is delivered to the cache controller after 10 ns. (The same arrangement can be used with Pentium).

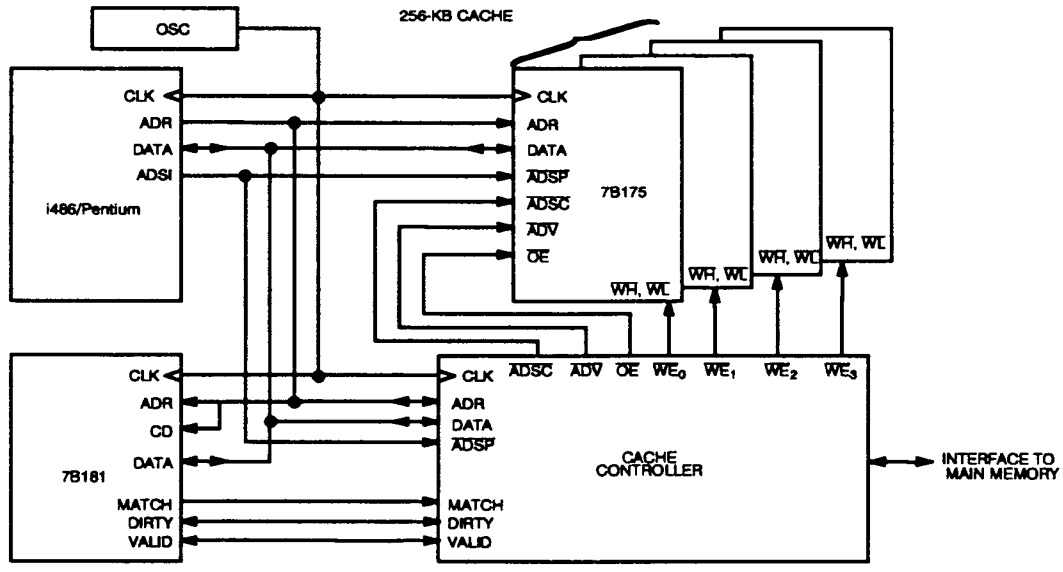


Figure 1. Cache Using Four CY7B175s

Synchronous Truth Tables[13, 14, 15, 16]

E	$\overline{ADSP}$	$\overline{ADSC}$	ADV	$\overline{W}$	CLK	Address Used	Operation
F	L	X	X	X	L–H	N/A	Deselected
F	X	L	X	X	L–H	N/A	Deselected
T	L	X	X	X	L–H	External Address	Read Cycle, Begin Burst
T	H	L	X	L	L–H	External Address	Write Cycle, Begin Burst
T	H	L	X	H	L–H	External Address	Read Cycle, Begin Burst
X	H	H	L	L	L–H	Next Address	Write Cycle, Continue Burst
X	H	H	L	H	L–H	Next Address	Read Cycle, Continue Burst
X	H	H	H	L	L–H	Current Address	Write Cycle, Supported Burst
X	H	H	H	H	L–H	Current Address	Read Cycle, Suspend Burst

Asynchronous Truth Tables[13, 17]

Operation	$\overline{OE}$	I/O Status
Read	L	Data Out (DQ_0 – DQ_8)
Read	H	High Z
Write	X	High Z – Data In (DQ_0 – DQ_8)
Deselected	X	High Z

Notes:

13. X means Don't Care.
14. All inputs except $\overline{G}$ must meet set-up and hold times for the low-to-high transition of clock (K).
15. E represents $\overline{E}$. T implies $\overline{E}$ = L; F implies $\overline{E}$ = H.
16. $\overline{W}$ represents $\overline{WL}$ and $\overline{WH}$ for lower and/or upper byte write.
17. For a write operation following a read operation, $\overline{OE}$ must be HIGH before the input data required set-up time and held HIGH through the input data hold time.

Pin Definitions

Signal Name	I/O	Description
$A_0 - A_{14}$	I	Address Inputs
CLK	I	Clock
$\overline{WL}$, $\overline{WH}$	I	Write Enable (Low Byte, High Byte)
$\overline{OE}$	I	Output Enable
$\overline{E}$	I	Chip Enable
$\overline{ADV}$	I	Address Advance
$\overline{ADSP}$	I	Processor Address Strobe
$\overline{ADSC}$	I	Cache Controller Address Strobe
$D_0 - D_{15}$	I/O	Data I/O
V_{CC}	–	+5V Power Supply
V_{SS}	–	Ground

Pin Descriptions

Input Signals	
CLK	Clock signal used as the reference for most on-chip operations.
$\overline{ADSP}$	Address strobe signal from the processor: $\overline{ADSP}$ is asserted when the processor address is valid. If $\overline{ADSP}$ is LOW at clock rise, the address at A_0 through A_{14} will be loaded into the address register and the address advancement logic. The write signals, $\overline{WH}$ and $\overline{WL}$, are ignored in the clock cycle where $\overline{ADSP}$ is asserted. If both $\overline{ADSP}$ or $\overline{ADSC}$ are active at clock rise, only $\overline{ADSP}$ will be recognized.
$\overline{ADSC}$	Address strobe signal from the cache controller: $\overline{ADSC}$ is asserted when a new address generated by the cache controller is ready to be strobed into the CY7B175/6. The write signal, $\overline{WH}/\overline{WL}$, is recognized in the clock cycle where $\overline{ADSC}$ is asserted. If both $\overline{ADSP}$ and $\overline{ADSC}$ are active at clock rise, only $\overline{ADSP}$ will be recognized.
$A_0 - A_{14}$	Address lines: These address inputs are loaded into the address register and the address advancement logic at clock rise if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW. They are used to select one of the 32K locations.
$\overline{WL}$, $\overline{WH}$	Write Enable Low Byte and Write Enable High Byte: These signals are sampled at the rising edge of the clock signal. If $\overline{WL}/\overline{WH} = 0$, a self-timed write operation will be initiated and data on $D_0 - D_{15}$ will be stored into the selected memory location. The only exception occurs if both $\overline{ADSP}$, $\overline{WH}$, and $\overline{WL}$ are LOW at clock rise. In this case, the write signal is ignored. $\overline{WL}$ is for $D_0 - D_7$ and $\overline{WH}$ is for $D_8 - D_{15}$.
$\overline{ADV}$	Address advance input: $\overline{ADV}$ is sampled at the rising edge of the clock. In the case of the CY7B175, LOW at this input will advance the address in the advancement logic according to the Intel 80486/Pentium burst sequence. In the case of the CY7B176, the addresses will be advanced linearly. This input is ignored if $\overline{ADSP}$ or $\overline{ADSC}$ is active (LOW).
$\overline{E}$	Chip enable inputs: $\overline{E}$ is active HIGH and $\overline{E}$ is active LOW. Both inputs are sampled at clock rise if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW. The RAM is selected if $\overline{E} = 1$ and $\overline{E} = 0$.
$\overline{OE}$	Output enable – $\overline{OE}$ is an asynchronous signal that disables all output drivers ($D_0 - D_8$) when it is deasserted. $\overline{OE}$ should be deasserted during write cycles because the CY7B175,/6 is a common I/O device and three-state conflict may occur at the data pins.
Bidirectional Signals	
$D_0 - D_{15}$	Data I/O lines: During a read cycle, if $\overline{OE}$ is asserted, data in the selected location will appear at these pins. During a write cycle, data presented at these pins is captured at clock rise and stored into the selected RAM location if $\overline{WH}$ and $\overline{WL}$ is LOW. All nine outputs will be placed in a three-state condition when $\overline{OE}$ is deasserted, when the RAM is deselected via the chip select inputs, or during a write cycle.

CYPRESS SEMICONDUCTOR

ADVANCED INFORMATION

CY7B175
CY7B176

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... − 65°C to +150°C

Ambient Temperature with Power Applied ..... − 55°C to +125°C

Supply Voltage on V_{CC} Relative to GND ... − 0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... − 0.5V to V_{CC} + 0.5V

DC Input Voltage[1] ..... − 0.5V to V_{CC} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[2]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	− 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		7B175−9 7B176−9 Min.	7B175−9 7B176−9 Max.	7B175−10, 14 7B176−10, 14 Min.	7B175−10, 14 7B176−10, 14 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = − 4.0 mA		2.4	3.3V	2.4	3.3V	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage[1]			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{CC}, Output Disabled		−100	+100	−100	+100	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−300		−300	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		210		210	mA
			Mil				230	
I_{SB1}	AC Standby Current	$\overline{E}$ = V_{IH}, I_{OUT} = 0 mA, All inputs = V_{IL} or V_{IH}, V_{IL} = 0.0V, and V_{IH} ≥ 3.0V, Cycle Time ≥ t_{CYC} (Min.)			60		60	mA
I_{SB2}	CMOSStandbyCurrent	$\overline{E}$ ≥ V_{CC} − 0.2V, All Inputs = V_{CC} − 0.2V, or ≤ 0.2V, Cycle Time ≥ t_{CYC} (Min.)			40		40	mA

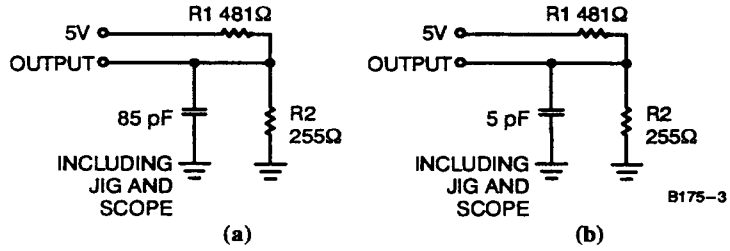
Capacitance[4]

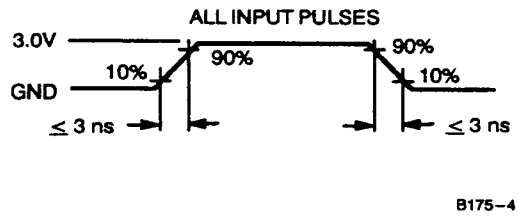
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}: Addresses	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	4	pF
C_{IN}: Other Inputs			5	pF
C_{OUT}	Output Capacitance		5	pF

Notes:

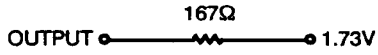
1. $V_{IL\,(min.)}$ = − 1.5V for pulse durations of less than 20 ns.
1. T_A is the "instant on" case temperature.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
5. Tested initially and after any design or process changes that may affect these parameters (PLCC package).

AC Test Loads and Waveforms





Equivalent to: THÉVENIN EQUIVALENT



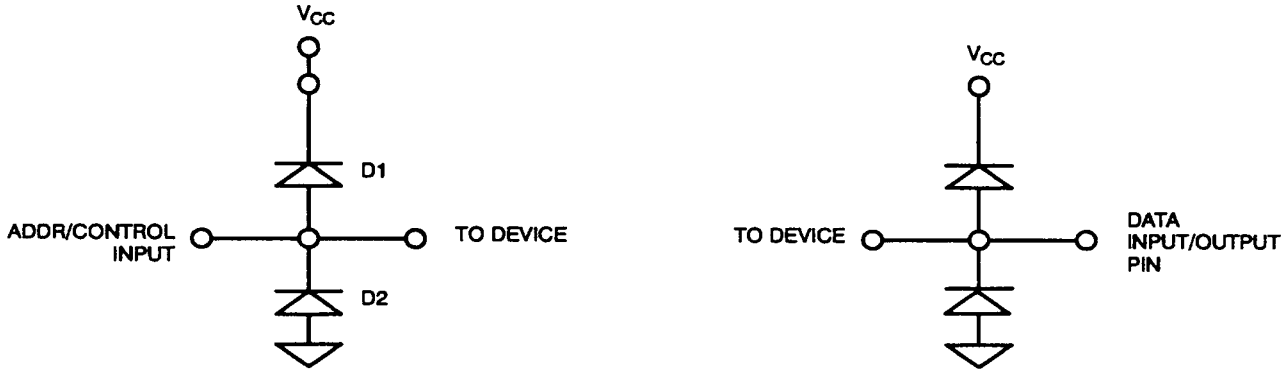
Switching Characteristics Over the Operating Range[5]

Parameter	Description	7B175–9 7B176–9		7B175–10 7B176–10		7B175–14 7B175–14		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	12.5		15		20		ns
f_{MAX}	Maximum Frequency		66		60		50	MHz
t_{CH}	Clock HIGH	5		5		8		ns
t_{CL}	Clock LOW	5		5		8		ns
t_{AS}	Address Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		1		ns
t_{CDV}	Data Output Valid After CLK Rise		9		10		14	ns
t_{DOH}	Data Output Hold After CLK Rise	3		3		3		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		0.5		1		ns
t_{WES}	$\overline{WE}$ Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{WEH}	$\overline{WE}$ Hold After CLK Rise	0.5		0.5		1		ns
t_{ADVS}	$\overline{ADV}$ Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.5		0.5		1		ns
t_{DS}	Data Input Set-Up Before CLK Rise	2.5		2.5		3		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		1		ns
t_{CES}	Chip Enable Set-Up	2.5		2.5		3		ns
t_{CEH}	Chip Enable Hold After CLK Rise	0.5		0.5		1		ns
t_{CEOZ}	Chip Enable Sampled to Output High Z[6, 7]	2	6	2	6	2	7	ns
t_{CEOV}	Chip Enable Sampled to Output Valid		9		10		14	ns
t_{EOZ}	$\overline{OE}$ HIGH to Output High Z[6]	2	6	2	6	2	7	ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid		5		5		6	ns
t_{WEOZ}	$\overline{WE}$ Sampled LOW to Output High Z[6]		5		6		7	ns
t_{WEOV}	$\overline{WE}$ Sampled HIGH to Output Valid		9		10		14	ns

Notes:

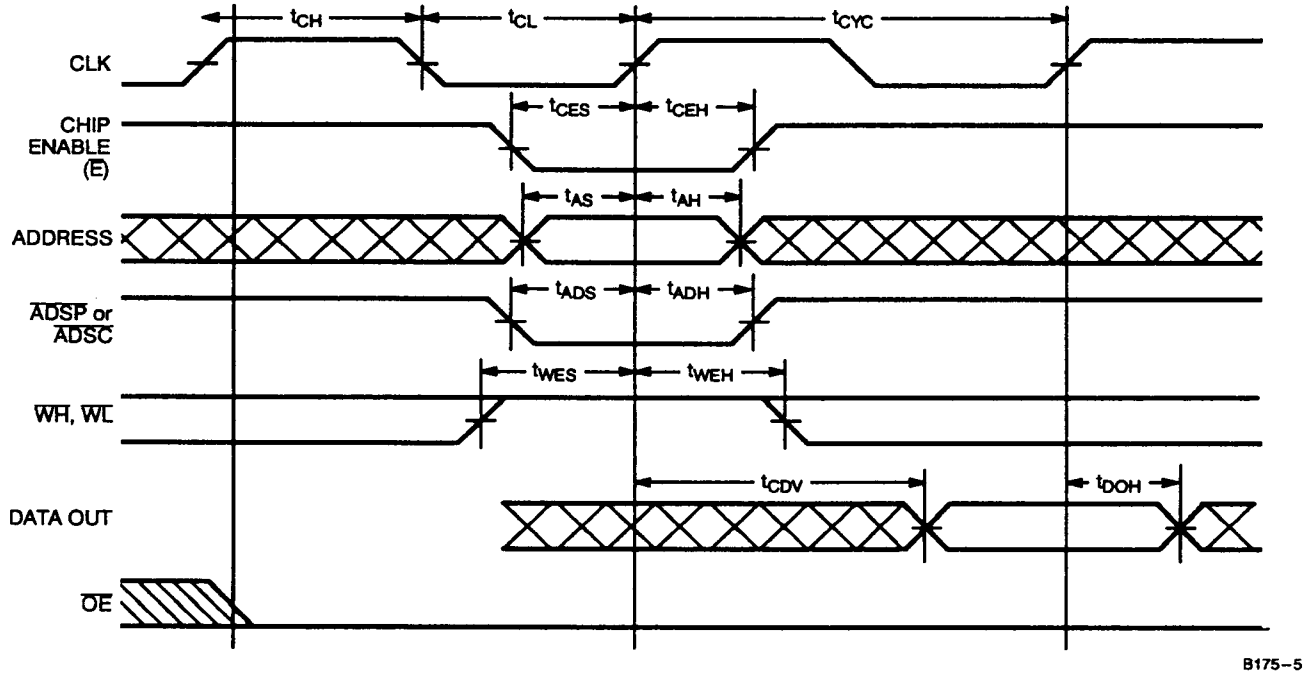
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 85-pF load capacitance.
6. t_{CEOZ}, t_{EOZ}, and t_{WEOZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
7. At any given voltage and temperature, t_{CEOZ} (t_{WEOZ}) min. is less than t_{CEOV} (t_{WEOV}) min.

Input/Output ESD and Clamp Diode Protection



Switching Waveforms

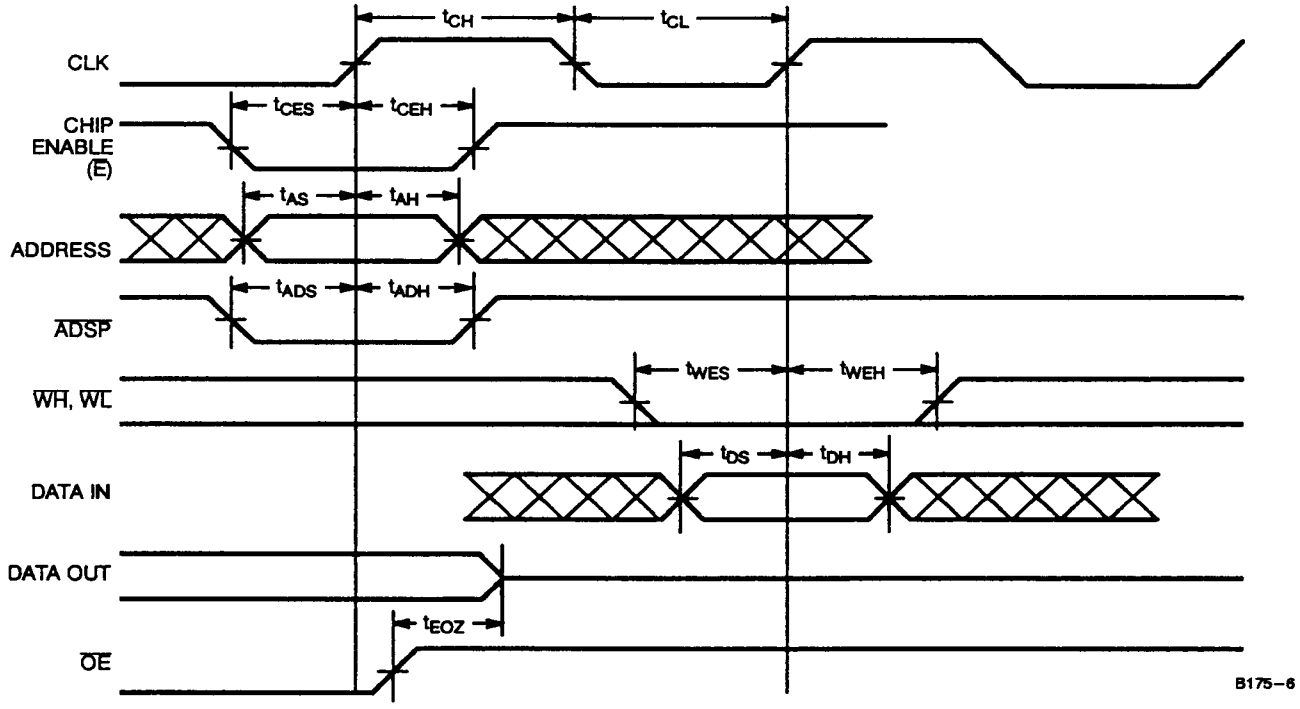
Single Read



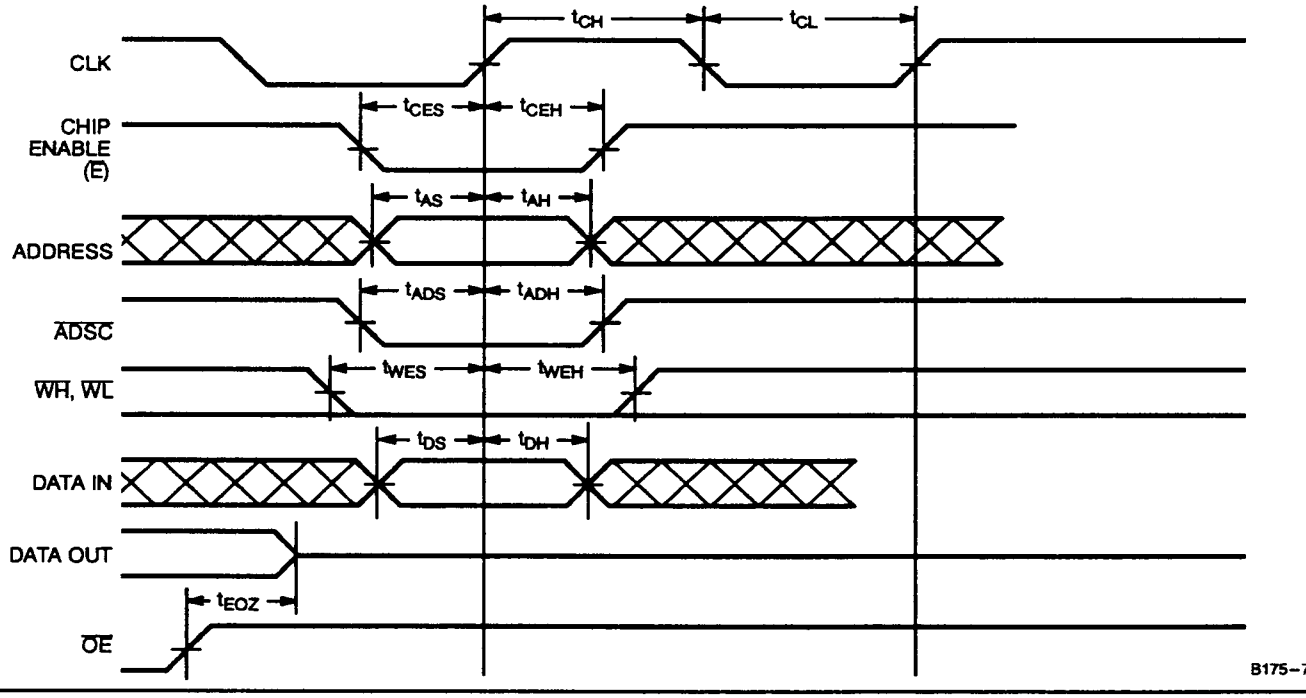
B175–5

Switching Waveforms (continued)

ADSP Write

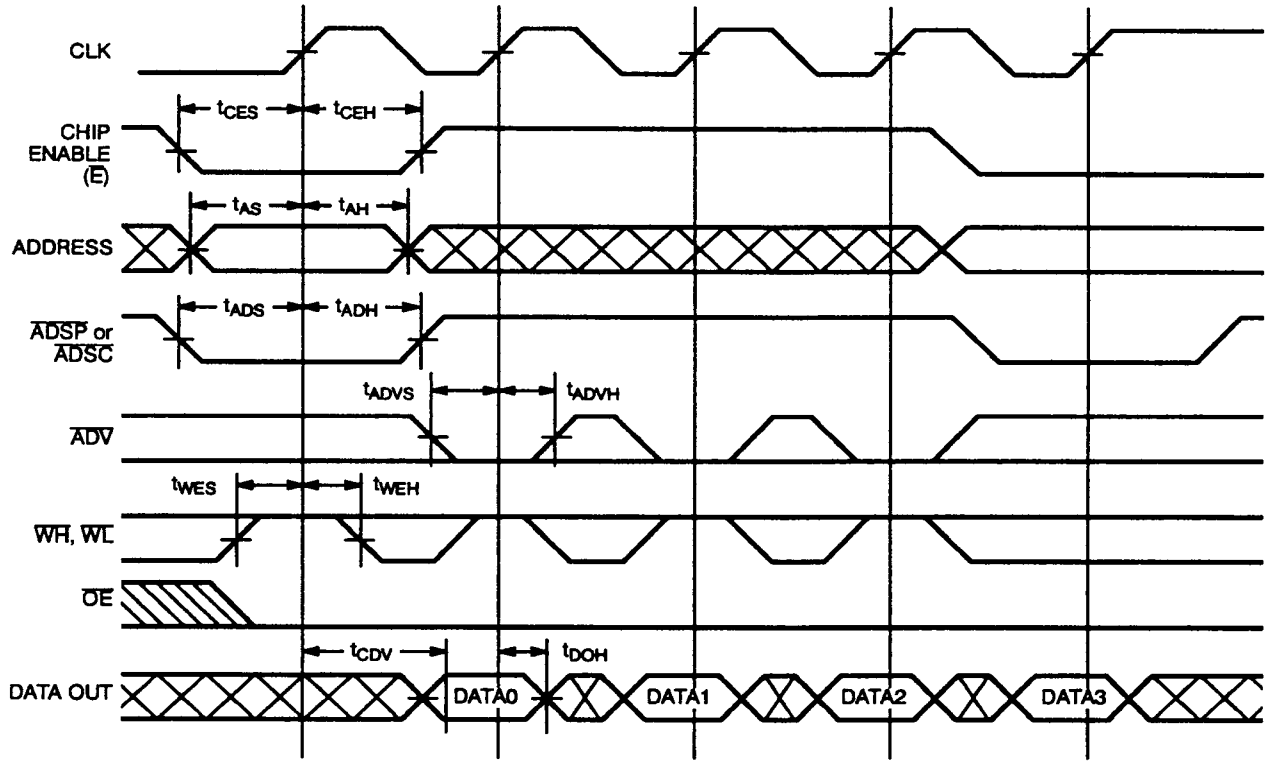


ADSC Write



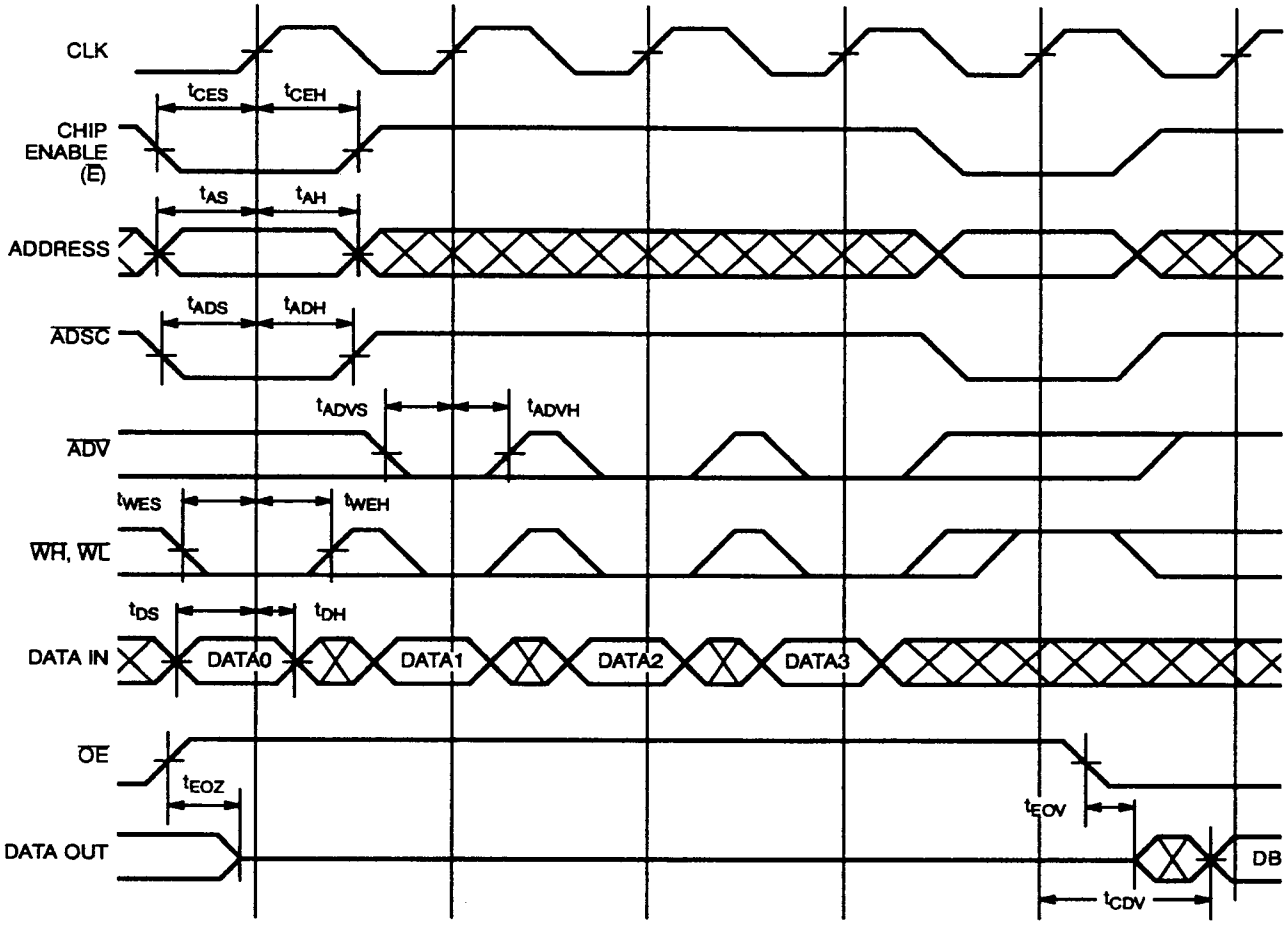
Switching Waveforms (continued)

Burst Read Sequence with Four Accesses

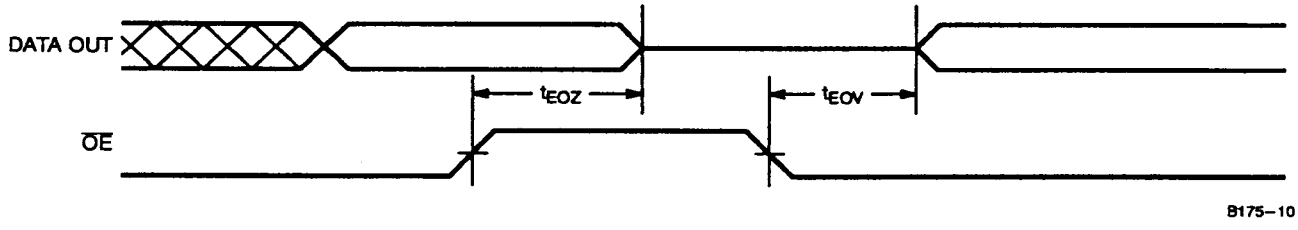


Switching Waveforms (continued)

ADSC Burst Write Sequence with Four Accesses Followed by a Single Read Cycle

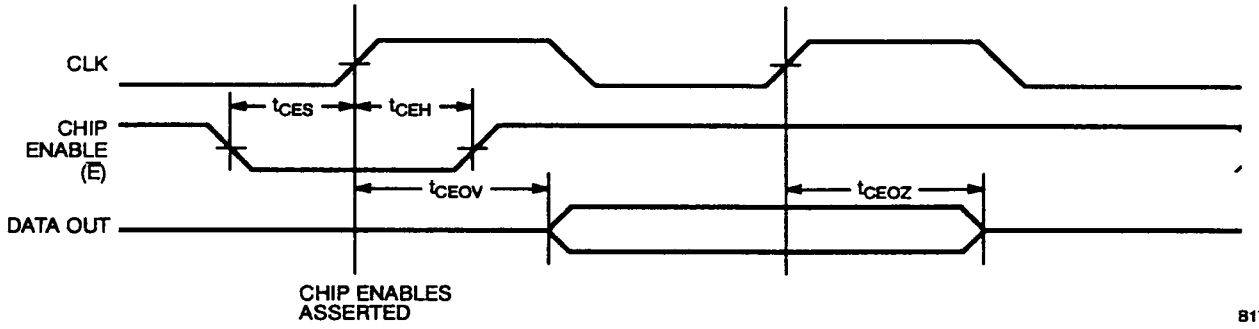


Output (Controlled by $\overline{OE}$)

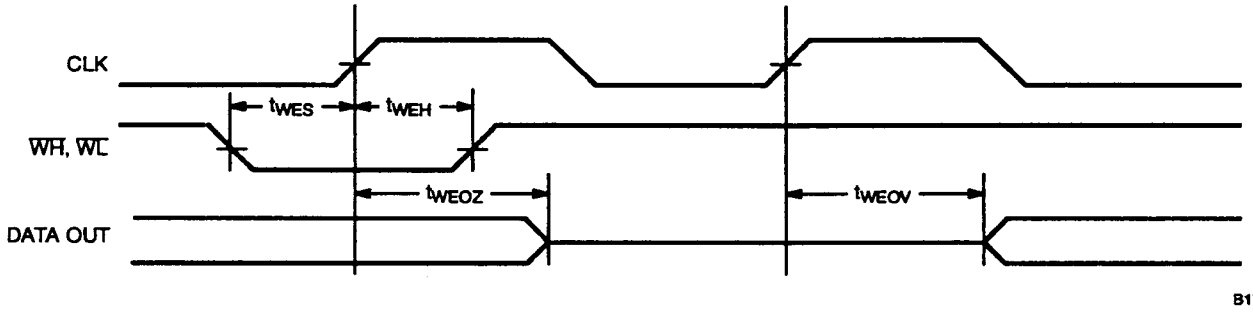


Switching Waveforms (continued)

Output Timing (Controlled by CE)



Output Timing (Controlled by $\overline{WE}$)



Ordering Information

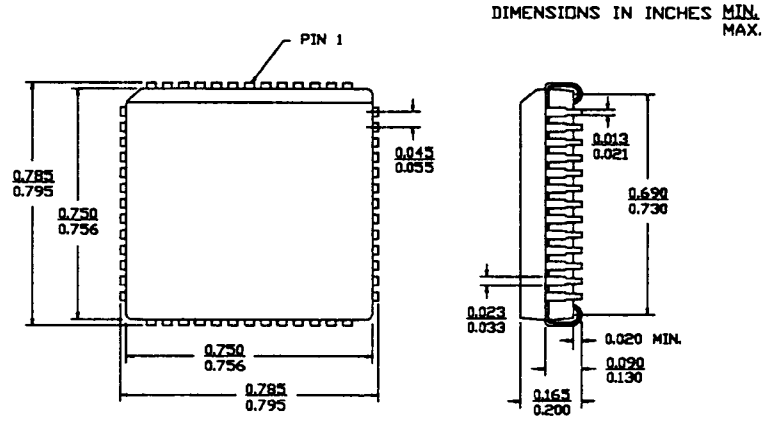
Speed (ns)	Ordering Code	Package Type	Operating Range
9	CY7B175–9JC	J69	Commercial
	CY7B175–9NC	TBD	
10	CY7B175–10JC	J69	Commercial
	CY7B175–10NC	TBD	
14	CY7B175–14JC	J69	Commercial
	CY7B175–14NC	TBD	
	CY7B175–14LMB	L69	Military

Speed (ns)	Ordering Code	Package Type	Operating Range
9	CY7B176–9JC	J69	Commercial
	CY7B176–9NC	TBD	
10	CY7B176–10JC	J69	Commercial
	CY7B176–10NC	TBD	
14	CY7B176–14JC	J69	Commercial
	CY7B176–14NC	TBD	
	CY7B176–14LMB	L69	Military

Document #: 38–A–00036–A

Package Diagrams

52-Lead Plastic Leaded Chip Carrier J69



52-Square Leadless Chip Carrier L69