

ispGAL16Z8

In-System Programmable High Performance E²CMOS PLD

FEATURES

- · IN-SYSTEM-PROGRAMMABLE --- 5-VOLT ONLY
- Change Logic "On The Fly" in Seconds
- Non-volatile E² Technology
- MINIMUM 10,000 ERASE/WRITE CYCLES
- DIAGNOSTIC MODE FOR CONTROLLING AND OBSERVING SYSTEM LOGIC
- · HIGH PERFORMANCE E1CMOST TECHNOLOGY
- 20 ns Maximum Propagation Delay
- Fmax = 41.6 MHz
- 90 mA MAX icc
- · E2 CELL TECHNOLOGY
- -- 100% Tested/Guaranteed 100% Yields
- 20 Year Data Retention
- · EIGHT OUTPUT LOGIC MACROCELLS
- Maximum Flexibility for Complex Logic Designs
- Programmable Output Polarity
- Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility
- · PRELOAD AND POWER-ON RESET OF REGISTERS
- 100% Functional Testability
- · APPLICATIONS INCLUDE:
 - Reconfigurable Interfaces and Decoders
 - "Soft" Hardware (Generic Systems)
- Copy Protection and Security Schemes
- Reconfiguring Systems for Testing
- · ELECTRONIC SIGNATURE FOR IDENTIFICATION

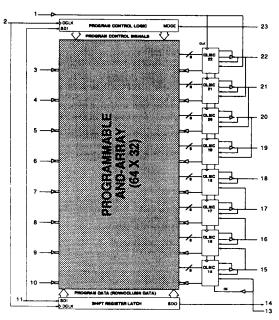
DESCRIPTION

The Lattice ispGAL® 16Z8 is a revolutionary programmable logic device featuring 5-volt only in-system programmability and insystem diagnostic capabilities. This is made possible by on-chip circuitry which generates and shapes the necessary high voltage programming signals. Using Lattice's proprietary UltraMOS® technology, this device provides true bipolar performance at significantly reduced power levels.

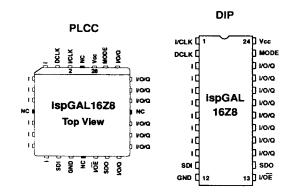
The 24-pin ispGAL16Z8 is architecturally and parametrically identical to the 20-pin GAL16V8, but includes 4 extra pins to control in-system programming. These pins are not associated with normal logic functions and are used only during programming and diagnostic operations. This 4-pin interface allows an unlimited number of devices to be cascaded to form a serial programming and diagnostics loop.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products.





PIN CONFIGURATION



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Specifications ispGAL16Z8 Commercial

ABSOLUTE MAXIMUM RATINGS(1)

Supply voltage V _{cc}	0.5 to +7V
Input voltage applied	
Off-state output voltage applied	
Storage Temperature	
Ambient Temperature with	
Power Applied	55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Ambient Temperature (T _A)	0 to +75°C
Supply voltage (V _{cc})	
with Respect to Ground	+4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.2	MAX.	UNITS
VIL	Input Low Voltage		Vss - 0.5	_	0.8	V
VIH	Input High Voltage		2.0	_	Vcc+1	V
lı.	Input or I/O Low Leakage Current	OV ≤ VIN ≤ VIL (MAX.)	_	_	-10	μА
Iн	Input or I/O High Leakage Current	V _{IH} ≤ V _{IN} ≤ V _{CC}	_	_	10	μА
V OL	Output Low Voltage	IoL = MAX. Vin = VIL or VIH	_	_	0.5	V
Vон	Output High Voltage	IOH = MAX. Vin = VIL or VIH	2.4	_		v
IOL	Low Level Output Current		 	_	24	mA
Юн	High Level Output Current			_	-3.2	mA
los¹	Output Short Circuit Current	Vcc = 5V Vout = 0.5V T _A = 25°C	-30	_	-150	mA
ICC	Operating Power Supply Current	VIL = 0.5V VIH = 3.0V ftoggle = 15Mhz Outputs Open	_	75	90	mA

One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.

CAPACITANCE ($T_A = 25 \text{ C}, f = 1.0 \text{ MHz}$)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C,	Input Capacitance	8	pF	V _{cc} = 5.0V, V _i = 2.0V
C ¹⁰	I/O Capacitance	10	pF	$V_{cc} = 5.0V, V_{vo} = 2.0V$

^{*}Guaranteed but not 100% tested.

²⁾ Typical values are at Vcc = 5V and Ta = 25 °C



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AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

54 54 WETER	TEST	DECOMM NON		-20		-25	
PARAMETER	COND.1			MIN. MAX.		MIN. MAX.	
t pd	1	Input or I/O to Combinational Output	3	20	3	25	ns
tco	1	Clock to Output Delay	2	15	2	15	ns
t su		Setup Time, Input or Feedback before Clock↑	15	_	20	_	ns
t h	_	Hold Time, Input or Feedback after Clock↑	0	_	0	_	ns
1 Maximum Clock Frequency with External Feedback, 1/(tsu + tco) 1 Maximum Clock Frequency with No Feedback		· -	33.3	_	28.5	_	MHz
			41.6	-	33.3	_	MHz
t wh³	_	Clock Pulse Duration, High	12	_	15	_	ns
tw 3	_	Clock Pulse Duration, Low	12	_	15	_	ns
t en	n 2 Input or I/O to Output Enabled			20	_	25	ns
	2	OE↓ to Output Enabled		18	_	20	ns
tdis 3 Input or 1/		Input or I/O to Output Disabled		20	_	25	ns
	3 OE↑ to Output Disabled			18		20	ns

- 1) Refer to Switching Test Conditions section.
- 2) Refer to fmax Description section.
- 3) Clock pulses of widths less than the specification may be detected as valid clock signals.

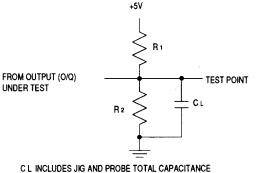
SWITCHING TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% - 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active

Output Load Conditions (see figure)

Test Condition		st Condition R ₁ R ₂		CL
1		200Ω	390Ω	50pF
2	Active High	∞	390Ω	50pF
	Active Low	200Ω	390Ω	50pF
3	Active High	∞	390Ω	5pF
	Active Low	200Ω	390Ω	5pF





ispGAL16Z8 ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	lcc (mA)	Ordering #	Package
20	15	15	90	ispGAL16Z8-20LP	24-Pin Plastic DIP
			90	ispGAL16Z8-20LJ	28-Lead PLCC
25	20	15	90	ispGAL16Z8-25LP	24-Pin Plastic DIP
			90	ispGAL16Z8-25LJ	28-Lead PLCC

PART NUMBER DESCRIPTION

