PRELIMINARY DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD70742

V820™
32-BIT MICROPROCESSOR

The μPD70742 (V820) is a 32-bit RISC-based microprocessor that features as processor core the V810™, a high-performance 32-bit microprocessor for embedded applications, and includes on-chip peripheral functions such as a DMA controller, an interrupt controller, a timer, a serial controller, a refresh function, and a chip select function.

The V820 has high real-time response capability and powerful instructions such as high-speed integer arithmetic instructions, bit string instructions, and floating-point processing instructions, and can achieve high cost-performance for equipment such as facsimile machines, digital plain paper copiers, image processing equipment, and real-time operating equipment.

Its functions are described in details in the manual indicated below. Please read this manual before starting design.

- **V820 User's Manual (Preliminary) : To be published**

FEATURES

- High-performance 32-bit microprocessor for embedded applications, V810, used for processor core.
  - On-chip 1KB cache memory
  - 1-clock pitch pipeline architecture
  - 16-bit fixed-length instruction set (except some instructions)
  - 32-bit address/data separated bus
  - Thirty two 32-bit general-purpose registers
  - 4GB linear address space
  - Hardware interlock against register/flag hazard
  - Powerful instruction set for various applications
    - Floating-point operation instructions (based upon IEEE754 data format)
    - Bit string instructions
- Dynamic bus sizing function (16-bit)
- 16-Bit bus fixing function
  - 16-bit bus system configurable
- 16 levels of high-speed interrupt response function
- On-chip peripherals
  - Clock synthesizer
  - Bus interface supported
  - Interrupt controller
  - Timer/counter (μPD71054 equivalent)
  - Serial controller (μPD71051 equivalent × 2)
  - 32-bit DMA controller (4 chs.)
- Clock control for each unit
  - Clock stop mode by internal static operation
    - Operable with low power consumption
- Wait setting/$\overline{CS}$ signal generation for divided memory and I/O area (by 4)
- Refresh timer, bus arbitration

ORDERING INFORMATION

Part Number	Package	Maximum Operating Frequency (MHz)
μPD70742GD-25-LML	208-pin plastic QFP (Fine pitch)(□28 mm)	25
μPD70742R-25	280-pin ceramic PGA	25

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

The information in this document is subject to change without notice.

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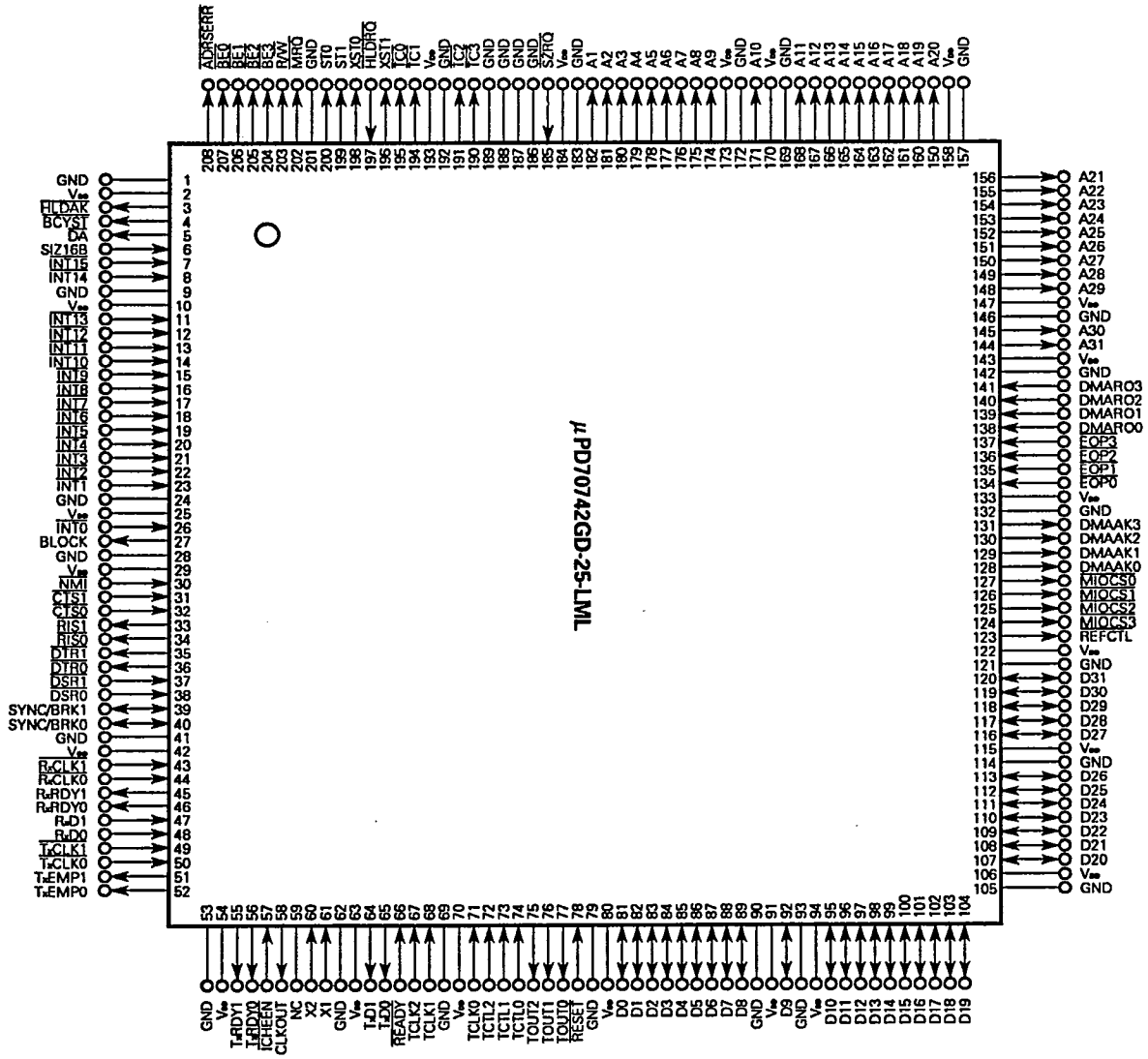
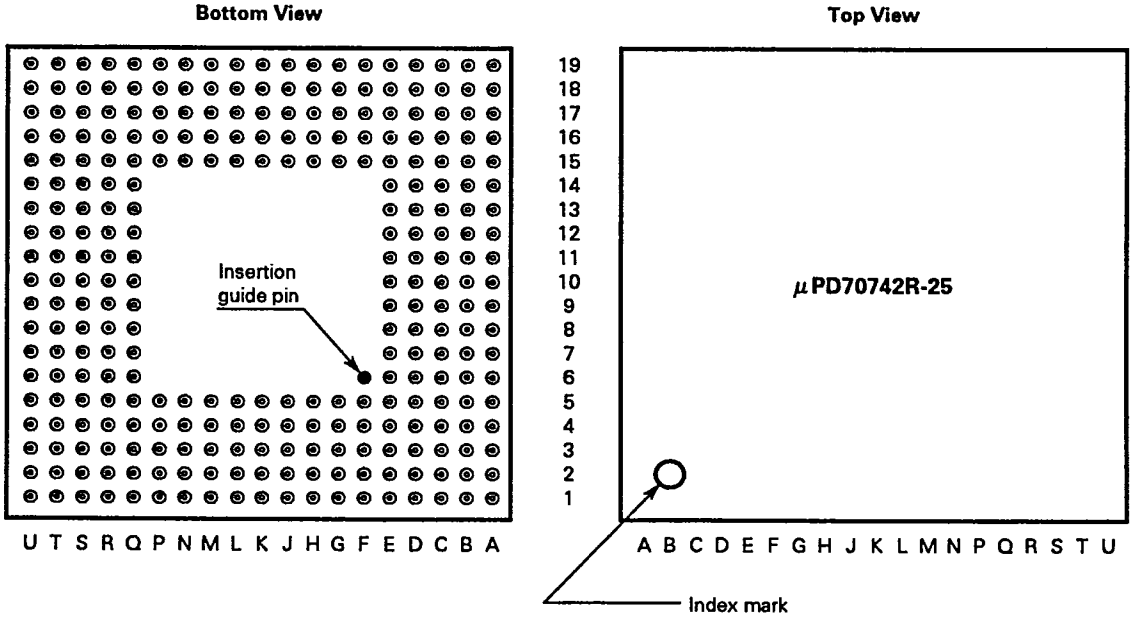
PIN CONFIGURATIONS

208-pin plastic QFP (Fine pitch)(□28 mm)(Top View)



PIN CONFIGURATIONS (Cont'd)

280-pin ceramic PGA



Remark Pin count does not include insertion guide pin.

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No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
A1	NC	A19	NC	B18	NC	C17	NC	D16	NC
A2	NC	B1	NC	B19	NC	C18	$\overline{BE0}$	D17	NC
A3	NC	B2	NC	C1	NC	C19	NC	D18	$\overline{BE2}$
A4	$\overline{RxCLK0}$	B3	NC	C2	V_{DD}	D1	X1	D19	R/$\overline{W}$
A5	IC2	B4	RxD0	C3	NC	D2	X2	E1	TxD0
A6	$\overline{DSR1}$	B5	RxRDY0	C4	$\overline{TxCLK0}$	D3	GND	E2	NC
A7	$\overline{RTS0}$	B6	V_{DD}	C5	TxEMP1	D4	NC	E3	$\overline{ICHEEN}$
A8	IC1	B7	SYNC/BRK1	C6	RxRDY1	D5	NC	E4	TxRDY0
A9	V_{DD}	B8	$\overline{DTR0}$	C7	$\overline{DSR0}$	D6	RxD1	E5	TxEMP0
A10	$\overline{INT0}$	B9	$\overline{CTS1}$	C8	$\overline{DTR1}$	D7	GND	E6	$\overline{TxCLK1}$
A11	GND	B10	GND	C9	$\overline{NMI}$	D8	IC2	E7	$\overline{RxCLK1}$
A12	$\overline{INT3}$	B11	$\overline{INT2}$	C10	V_{DD}	D9	$\overline{CTS0}$	E8	SYNC/BRK0
A13	$\overline{INT7}$	B12	$\overline{INT5}$	C11	$\overline{INT1}$	D10	IC1	E9	$\overline{RTS1}$
A14	$\overline{INT10}$	B13	$\overline{INT8}$	C12	$\overline{INT6}$	D11	IC1	E10	BLOCK
A15	V_{DD}	B14	$\overline{INT12}$	C13	$\overline{INT11}$	D12	IC1	E11	$\overline{INT4}$
A16	NC	B15	$\overline{INT14}$	C14	GND	D13	$\overline{INT13}$	E12	$\overline{INT9}$
A17	$\overline{BCYST}$	B16	SIZ16B	C15	$\overline{INT15}$	D14	$\overline{DA}$	E13	NC
A18	NC	B17	V_{DD}	C16	NC	D15	NC	E14	$\overline{HLDAK}$

(2/2)

No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name	No.	Pin Name
E15	GND	J4	TCTL1	N2	GND	R1	D14	T1	NC
E16	$\overline{\text{ADRSERR}}$	J5	TCTL2	N3	D8	R2	D16	T2	NC
E17	$\overline{\text{BE3}}$	J15	GND	N4	IC1	R3	NC	T3	V_{DD}
E18	GND	J16	GND	N5	D11	R4	NC	T4	D23
E19	ST1	J17	V_{DD}	N15	A19	R5	NC	T5	D25
F1	GND	J18	IC1	N16	A15	R6	D22	T6	D27
F2	V_{DD}	J19	$\overline{\text{SZRQ}}$	N17	A10	R7	V_{DD}	T7	D30
F3	TxD1	K1	D0	N18	V_{DD}	R8	D31	T8	$\overline{\text{REFCTL}}$
F4	TxRDY1	K2	V_{DD}	N19	A9	R9	$\overline{\text{MIOCS2}}$	T9	$\overline{\text{MIOCS1}}$
F5	CLKOUT	K3	TOUT0	P1	D9	R10	DMAAK2	T10	NC
F15	$\overline{\text{BE1}}$	K4	GND	P2	GND	R11	EOP0	T11	IC1
F16	$\overline{\text{MRQ}}$	K5	$\overline{\text{RESET}}$	P3	V_{DD}	R12	DMARQ1	T12	DMARQ0
F17	XST0	K15	A1	P4	D13	R13	A31	T13	IC1
F18	$\overline{\text{HLDRQ}}$	K16	A2	P5	D17	R14	A27	T14	A30
F19	$\overline{\text{TC0}}$	K17	A3	P15	NC	R15	A21	T15	A28
G1	TCLK0	K18	NC	P16	A17	R16	NC	T16	A26
G2	TCLK2	K19	GND	P17	A11	R17	NC	T17	A24
G3	TCLK1	L1	D1	P18	A12	R18	A18	T18	NC
G4	NC	L2	D2	P19	GND	R19	A14	T19	NC
G5	NC	L3	NC	Q1	D10	S1	NC	U1	NC
G15	ST0	L4	IC1	Q2	D12	S2	D18	U2	NC
G16	XST1	L5	D5	Q3	D15	S3	NC	U3	D21
G17	V_{DD}	L15	IC1	Q4	D19	S4	NC	U4	NC
G18	IC1	L16	A7	Q5	GND	S5	D24	U5	GND
G19	GND	L17	A5	Q6	D20	S6	D26	U6	D29
H1	TCTL0	L18	A4	Q7	NC	S7	D28	U7	GND
H2	IC2	L19	IC1	Q8	IC1	S8	V_{DD}	U8	IC1
H3	V_{DD}	M1	D4	Q9	$\overline{\text{MIOCS3}}$	S9	$\overline{\text{MIOCS0}}$	U9	DMAAK0
H4	$\overline{\text{READY}}$	M2	D6	Q10	DMAAK3	S10	DMAAK1	U10	IC1
H5	GND	M3	D3	Q11	$\overline{\text{EOP2}}$	S11	V_{DD}	U11	GND
H15	$\overline{\text{TC1}}$	M4	IC1	Q12	GND	S12	IC1	U12	$\overline{\text{EOP1}}$
H16	$\overline{\text{TC2}}$	M5	V_{DD}	Q13	GND	S13	DMARQ3	U13	$\overline{\text{EOP3}}$
H17	GND	M15	A13	Q14	A25	S14	A29	U14	DMARQ2
H18	$\overline{\text{TC3}}$	M16	GND	Q15	A22	S15	A23	U15	V_{DD}
H19	GND	M17	V_{DD}	Q16	V_{DD}	S16	NC	U16	V_{DD}
J1	IC2	M18	A8	Q17	A20	S17	NC	U17	NC
J2	TOUT1	M19	A6	Q18	A16	S18	GND	U18	NC
J3	TOUT2	N1	D7	Q19	IC1	S19	NC	U19	NC

Cautions 1. V_{DD} is the power supply pin. All V_{DD} pins should be connected to the same +5 V power supply line.

2. GND is the ground pin. All GND pins should be directly connected to the same GND line.

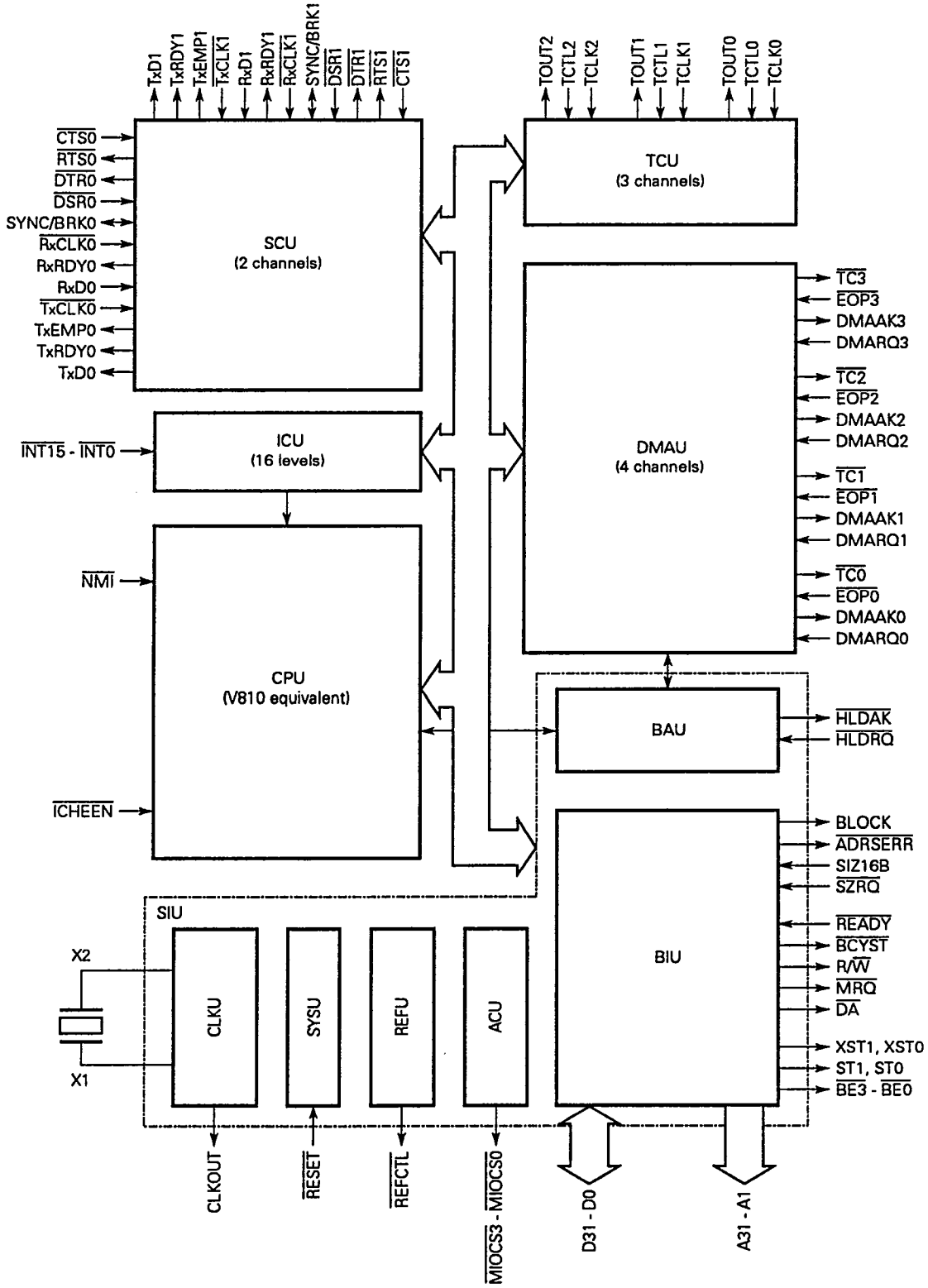
3. IC1 pins should be left open.

4. IC2 pins should be connected to V_{DD} line.

Remarks IC : Internally connected

NC: No connection

BLOCK DIAGRAM



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1. PIN FUNCTIONS

1.1 LIST OF PIN FUNCTIONS

(1/3)

Pin name	Input/Output	Functions	Bus holding state during operation	Bus holding state after reset	Bus idling state after reset
A31-A1 (Address Bus)	3-state output	Address bus	Hi-Z	Hi-Z	H Note
D31-D0 (Data Bus)	3-state I/O	Bidirectional data bus	Hi-Z	Hi-Z	Hi-Z
$\overline{BE3}$-$\overline{BE0}$ (Byte Enable)	3-state output	Indicate effective data when accessing data.	Hi-Z	Hi-Z	H
ST1, ST0 (Status)	3-state output	Indicate bus cycle type.	Hi-Z	Hi-Z	H
XST1, XST0 (Extended Status)	3-state output	Indicate bus cycle type for peripherals.	Hi-Z	Hi-Z	H
$\overline{DA}$ (Data Access)	3-state output	Outputs strobe signal in bus cycle.	Hi-Z	Hi-Z	H
$\overline{MRQ}$ (Memory Request)	3-state output	Indicates memory access.	Hi-Z	Hi-Z	H
R/$\overline{W}$ (Read/Write)	3-state output	Indicates read access or write access.	Hi-Z	Hi-Z	H
$\overline{BCYST}$ (Bus Cycle Start)	3-state output	Indicates start of bus cycle.	Hi-Z	Hi-Z	H
$\overline{READY}$ (Ready)	Input	Extends bus cycle.	–	–	–
$\overline{HLDRQ}$ (Hold Request)	Input	Requests bus control.	–	–	–
$\overline{HLDAK}$ (Hold Acknowledge)	Output	Outputs acknowledge signal in response to $\overline{HLDRQ}$.	L	L	H
$\overline{SZRQ}$ (Bus Sizing Request)	Input	Requests bus sizing.	–	–	–
SIZ16B (Bus Size 16 Bit)	Input	Fixes external data bus width to 16-bit.	–	–	–
BLOCK (Bus Lock)	Output	Outputs signal disabling bus control.	L	L	L
$\overline{ADRSERR}$ (Address Error)	Output	Indicates incorrect data alignment.	Unchanged	H	H
$\overline{ICHEEN}$ (Instruction Cache Enable)	Input	Enables operation of instruction cache.	–	–	–
$\overline{REFCTL}$ (Refresh Control)	Output	Outputs refresh control signals.	H	H	H

Note A1 pin is high in the 16-bit bus mode, and is low at all other times.

(2/3)

Pin name	Input/Output	Functions	Bus holding state during operation	Bus holding state after reset	Bus idling state after reset
$\overline{\text{MIOCS3}}$-$\overline{\text{MIOCS0}}$ (Memory I/O Chip Select)	Output	Output chip select signal for memory and I/O.	H	H	H
$\overline{\text{RESET}}$ (Reset)	Input	Resets internal circuits.	–	–	–
X1, X2 (Crystal)	Input	Connected with crystal resonator or external clock generator. X2 should be left open when external clock is used.	–	–	–
CLKOUT (System Clock Out)	Output	Outputs internally generated system clock signals.	Note	Note	Note
$\overline{\text{INT15}}$-$\overline{\text{INT0}}$ (Interrupt)	Input	Issue interrupt request to interrupt control unit.	–	–	–
$\overline{\text{NMI}}$ (Non-maskable Interrupt)	Input	Issue non-maskable interrupt request to CPU.	–	–	–
TOUT2-TOUT0 (Timer Output)	Output	Output signals from timer/counter.	–	–	–
TCTL2-TCTL0 (Timer Control)	Input	Control operation of timer/counter.	–	–	–
TCLK2-TCLK0 (Timer Clock)	Input	Determine transmission rate of timer/counter.	–	–	–
TxD1, TxD0 (Transmit Data)	Output	Output serial transmission data.	–	L	L
TxRDY1, TxRDY0 (Transmitter Ready)	Output	Indicate that write of transmission data to serial control unit is enabled.	–	H	H
TxEMP1, TxEMP0 (Transmitter Buffer Ready)	Output	Indicate that 2-stage transmission data buffer is empty.	–	H	H
$\overline{\text{TxCLK1}}$, $\overline{\text{TxCLK0}}$ (Transmitter Clock)	Input	Output reference clock signal to determine transmission rate.	–	–	–
RxD1, RxD0 (Receive Data)	Input	Input serial reception data.	–	–	–
RxRDY1, RxRDY0 (Receiver Ready)	Output	Indicate that read of reception data from serial control unit is enabled.	–	L	L
$\overline{\text{RxCLK1}}$, $\overline{\text{RxCLK0}}$ (Receiver Clock)	Input	Output reference clock signal to determine reception rate.	–	–	–
SYNC/BRK1, SYNC/BRK0 (Synchronization/Break)	I/O	SYNC used to detect synchronization in synchronous mode. BRK used to detect break state in asynchronous mode.	–	L	L
$\overline{\text{DSR1}}$, $\overline{\text{DSR0}}$ (Data Set Ready)	Input	Input communication status signal.	–	–	–

Note Always outputs clock signals.

(3/3)

Pin name	Input/Output	Functions	Bus holding state during operation	Bus holding state after reset	Bus idling state after reset
$\overline{DTR1}$, $\overline{DTR0}$ (Data terminal Ready)	Output	Output communication status signal.	–	H	H
$\overline{RTS1}$, $\overline{RTS0}$ (Request To Send)	Output	Output communication status signal.	–	H	H
$\overline{CTS1}$, $\overline{CTS0}$ (Clear To Send)	Input	Input signals for transmission control.	–	–	–
DMARQ3-DMARQ0 (DMA Request)	Input	Request DMA service.	–	–	–
DMAAK3-DMAAK0 (DMA Acknowledge)	Output	Indicate that DMA service request is acknowledged.	–	L	L
$\overline{EOP3}$-$\overline{EOP0}$ (End Of Process)	Input	Terminate DMA service from external.	–	–	–
$\overline{TC3}$-$\overline{TC0}$ (Terminal Count)	Output	Terminate DMA service.	–	H	H
V_{DD} (Power Supply)	–	Connected to +5V power supply.	–	–	–
GND (Ground)	–	Connected to ground line (0 V).	–	–	–
IC1 (Internally Connected 1)	–	Internally connected. Should be left open.	–	–	–
IC2 (Internally Connected 2)	–	Internally connected. Should be directly connected to V_{DD} line.	–	–	–

2. CPU

The CPU has functions equivalent to those of the V810 microprocessor for embedded applications, and additionally has bit string instructions, floating-point operation instructions, and high real-time response capability.

Features of CPU

- High-performance RISC-based microprocessor
  - On-chip 1KB cache memory
  - 1-clock pitch pipeline architecture
  - 16-bit fixed-length instruction set (except some instructions)
  - 32-bit address/data separated bus
  - Thirty two 32-bit general-purpose registers
  - 4GB linear address space
  - Hardware interlock against register/flag hazard
- Powerful instruction set for various applications
  - Floating-point operation instructions (based upon IEEE754 data format)
  - Bit string instructions
- High-speed interrupt response
- Standby function by stopping clock
- Debugging support function

3. SIU (System Integration Unit)

The SIU consists of six function sub-units, and performs system start-up, initialization, configuration, internal clock generation, bus controlling, and memory controlling.

(1) System control unit (SYSU)

Has the following functions:

- Selection of clock input to the TCU
- Selection of clock input to the SCU

(2) Clock control unit (CLKU)

Generates system clock that is used by V820, and controls supply for each unit.

(3) Bus interface unit (BIU)

Controls pins of data bus, address bus, and control bus. These buses are used by CPU and DMAU.

BIU provides 32-bit separated bus interface for both address and data based on the bus interface system of V810.

BIU also supports dynamic bus sizing function that dynamically corresponds to 16-bit or 32-bit data accessing, and 16-bit fixed data bus sizing function. The dynamic bus sizing function cannot be used for the DMAU.

(4) Bus arbitration unit (BAU)

Arbitrates bus controls among bus hold requests from the CPU, the DMAU, and an external bus master.

(5) Refresh support unit (REFU)

Supports refresh operation of DRAM.

The REFU has an interval timer function that generates refresh timings, bus control request function for executing refresh cycles, and refresh control signal generation function to DRAM controller.

During the refresh cycle, CPU and DMAU pass bus control to external refresh control circuit (bus hold state).

Refresh cycle and period should be programmed by software.

Caution Note that the bus control for refresh cannot be obtained if the CPU clock is stopped by using clock control unit.

(6) Access control unit (ACU)

The ACU has a programmable wait control function that controls the generation of chip select signal and the insertion of wait state into access bus cycle.

Up to four access spaces can be supported, each of which can be specified independently by means of base address and address masking. Each space can be sized in 2^n intervals from 16 bytes to 4 gigabytes.

4. ICU (Interrupt Control Unit)

The ICU performs arbitration of up to sixteen interrupt requests (maskable interrupt), and generation of interrupt request to the CPU.

Features of ICU

- Sixteen interrupt requests
- Interrupt request masking function
- Edge-triggered/level-triggered selection

5. TCU (Timer/Counter Unit)

The TCU includes three counters which can be used as timers, event counters, or rate generators. The functions of the TCU are equivalent to those of the μPD71054.

Features of TCU

- Three 16-bit counters
- Programmable six count modes
- Selection from binary count or BCD count
- Multiple latch command
- Count rate: 0 (DC) to 10 MHz

6. SCU (Serial Control Unit)

The SCU provides 2 channels for synchronous or asynchronous serial communication. Both channels have functions equivalent to those of the μPD71051.

Features of SCU

- Synchronous/asynchronous mode
  - Synchronous mode
    - Synchronizing characters: 1 or 2
    - Internal/external synchronization detection
    - Automatic insertion of synchronizing characters
  - Asynchronous mode
    - Clock rate: baud rate × 1, 16, or 64
    - Transmission stop bit: 1, 1.5, or 2 bits
    - Break transmission
    - Automatic break detection
    - Fault start bit detection
- Baud rate: 0 (DC) to 300K bps
- Full-duplex double buffered transmitter/receiver
- Parity append/check
- Error detection: parity, overrun, framing
- Characters of 5 to 8 bits

7. DMAU (Direct Memory Access Control Unit)

The V820 has on-chip four-independent-channel 32-bit DMA controller.

The DMAU supports two types of DMA transfer: 2-cycle transfer that performs DMA transfer by buffering transferred data in the DMAU, and fly-by transfer that performs DMA transfer without buffering transferred data in the DMAU.

The DMAU also has a funneling function that performs pack/unpack of transfer data, enabling DMA transfer between I/O device and memory with different data widths each other.

Features of DMAU

- Four independent DMA channels
- Four 32-bit address registers
- Four 32-bit count registers
- 2-clock bus cycle
- Three transfer modes
  - Single transfer mode
  - Demand transfer mode
  - Block transfer mode
- Three transfer types
  - Fly-by I/O to memory transfer
  - 2-cycle I/O to memory transfer
  - Memory to memory transfer
- Data funneling function
- DMA request masking for each channel
- Automatic initialization
- $\overline{TC}$ output at transfer end
- Forced termination of DMA servicing by $\overline{EOP}$ input

8. ELECTRICAL SPECIFICATIONS (PRELIMINARY)

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	V_{DD}		−0.5 to +7.0	V
Input voltage	V_I	V_{DD} = 5 V ±10 %	−0.5 to V_{DD}+0.3	V
Clock input voltage	V_K	V_{DD} = 5 V ±10 %	−0.5 to V_{DD}+0.3	V
Output voltage	V_O	V_{DD} = 5 V ±10 %	−0.5 to V_{DD}+0.3	V
Operating ambient temperature	T_{opt}		−10 to +70	°C
Storage temperature	T_{stg}		−65 to +150	°C

Cautions 1. Do not connect output (and bidirectional) pins each other. Do not connect output (or bidirectional) pins directly to the V_{DD}, V_{CC}, or GND line. However, open drain pin and open collector pins can be directly connected to V_{DD}, V_{CC}, or GND line. If timing design is made so that no signal conflict occurs, three-state pins can also be connected directly to three-state pins of external circuit.

2. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently. The device should be operated within the limits specified under DC and AC Characteristics.

DC CHARACTERISTICS (T_a = −10 °C to +70 °C, V_{DD} = 5 V ±10 %)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Clock input voltage, high	V_{KH}		4.0	V_{DD}+0.3	V
Clock input voltage, low	V_{KL}		−0.5	+0.6	V
Input voltage, high	V_{IH}		2.2	V_{DD}+0.3	V
Input voltage, low	V_{IL}		−0.5	+0.8	V
Output voltage, high	V_{OH}	I_{OH} = −400 μA	2.4		V
Output voltage, low	V_{OL}	I_{OL} = 3.2 mA		0.45	V
Input leakage current, high	I_{LIH}	V_{IN} = V_{DD}		10	μA
Input leakage current, low	I_{LIL}	V_{IN} = 0 V		−10	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD}		10	μA
Output leakage current, low	I_{LOL}	V_O = 0 V		−10	μA
Supply current	I_{DD}	f = 25 MHz		360	mA

Remark Power supply current is nearly proportional to operating clock frequency in operation mode.

CAPACITANCE (T_a = 25 °C, V_{DD} = 5 V ±10 %)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Input capacitance	C_I	f_c = 1 MHz		15	pF
I/O capacitance	C_{IO}			15	pF

AC CHARACTERISTICS (T_a = −10 °C to +70°C, V_{DD} = 5 V ±10 %)

CLOCK

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Clock cycle	t_{CYX}		240	1000	ns
CLKOUT stabilization time (from V_{DD})	t_{CYVS}		1000		μs
Clock pulse high level width	t_{XXH}		117		ns
Clock pulse low level width	t_{XXL}		117		ns
Clock rise time	t_{XXR}			3	ns
Clock fall time	t_{XXF}			3	ns
CLKOUT delay time (for external clock)	t_{DXK}		15		ns
CLKOUT cycle	t_{CYK}		40		ns
CLKOUT high level	t_{KKH}		0.5t_{CYK}−5		ns
CLKOUT low level	t_{KKL}		0.5t_{CYK}−5		ns
CLKOUT rise time	t_{KR}			5	ns
CLKOUT fall time	t_{KF}			5	ns

RESET

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ setup time (for CLKOUT ↓, active)	t_{SRKF}		15		ns
$\overline{\text{RESET}}$ setup time (for CLKOUT ↓, inactive)	t_{SRKR}		15		ns
$\overline{\text{RESET}}$ hold time (for CLKOUT ↓)	t_{HKR}		15		ns
$\overline{\text{RESET}}$ pulse low level width (after CLKOUT stabilized, for CLKOUT ↑)	t_{WRL}		20t_{CYKR}		ns
CLKOUT cycle (at $\overline{\text{RESET}}$)	t_{CYKR}		40	1000	ns
CLKOUT pulse high level	t_{KKHR}		0.5t_{CYKR}−5		ns
CLKOUT pulse low level	t_{KKLR}		0.5t_{CYKR}−5		ns

MEMORY, I/O ACCESS

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Address, etc., output delay (from CLKOUT ↑)	t_{DKA}		3	19	ns
Address, etc., output hold time (from CLKOUT ↑)	t_{HKA}		3	19	ns
$\overline{MIOCSn}$ output delay (from CLKOUT ↓)	t_{DKMS}		3	19	ns
$\overline{MIOCSn}$ output hold time (from CLKOUT ↓)	t_{HKMS}		3	19	ns
$\overline{BCYST}$ output delay (from CLKOUT ↑)	t_{DKBC}		3	19	ns
$\overline{BCYST}$ output hold time (from CLKOUT ↑)	t_{HKBC}		3	19	ns
$\overline{DA}$ output delay (from CLKOUT ↑)	t_{DKDA}		3	19	ns
$\overline{DA}$ output hold time (from CLKOUT ↑)	t_{HKDA}		3	19	ns
$\overline{READY}$ setup time (to CLKOUT ↓)	t_{SRYK}		6		ns
$\overline{READY}$ hold time (from CLKOUT ↓)	t_{HKRY}		6		ns
Data setup time (to CLKOUT ↑)	t_{SDK}		6		ns
Data hold time (from CLKOUT ↑)	t_{HKD}		6		ns
Data output delay (from active, from CLKOUT ↓)	t_{DKDT}		3	19	ns
Data output hold time (to active, from CLKOUT ↓)	t_{HKDT}		3	19	ns
Data output delay (from float, from CLKOUT ↓)	t_{LZKDT}		2	20	ns
Data output hold time (to float, from CLKOUT ↓)	t_{HZKDT}		2	20	ns

DYNAMIC BUS SIZING

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SZRQ}$ setup time (for CLKOUT ↓)	t_{SSZK}		6		ns
$\overline{SZRQ}$ hold time (for CLKOUT ↓)	t_{HKSZ}		6		ns

INTERRUPT

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{NMI}$ setup time (to CLKOUT ↓)	t_{SNK}		6		ns
$\overline{NMI}$ hold time (from CLKOUT ↓)	t_{HKN}		6		ns
Level mode $\overline{INTn}$ setup time (to CLKOUT ↑)	t_{SILK}		6		ns
Level mode $\overline{INTn}$ hold time (from CLKOUT ↑)	t_{HKIL}		6		ns
Edge mode $\overline{INTn}$ setup time (to CLKOUT ↑)	t_{SIEK}		9		ns
Edge mode $\overline{INTn}$ pulse width	t_{CYIE}		20		ns

BUS HOLD

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{HLDRQ}}$ setup time (to CLKOUT ↓)	t_{SHQK}		6		ns
$\overline{\text{HLDRQ}}$ hold time (from CLKOUT ↓)	t_{HKHQ}		6		ns
$\overline{\text{HLDAK}}$ output delay (from CLKOUT ↑)	t_{DKHA}		3	19	ns
$\overline{\text{HLDAK}}$ output hold time (from CLKOUT ↑)	t_{HKHA}		3	19	ns
Address, etc., delay (from active, from CLKOUT ↑)	t_{HZKA}		2	20	ns
Address, etc., delay (from float, from CLKOUT ↑)	t_{LZKA}		2	20	ns
Data delay (from active, from CLKOUT ↓)	t_{HZKD}		2	20	ns
Data delay (from float, from CLKOUT ↓)	t_{LZKD}		2	20	ns
$\overline{\text{MIOCS}}$n output delay (from CLKOUT ↓)	t_{DKMS}		3	19	ns
$\overline{\text{MIOCS}}$n output hold time (from CLKOUT ↓)	t_{HKMS}		3	19	ns
$\overline{\text{DA}}$ output delay (from active, from CLKOUT ↑)	t_{HZKDA}		2	20	ns
$\overline{\text{DA}}$ output delay (from float, from CLKOUT ↑)	t_{LZKDA}		2	20	ns

REFRESH

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{REFCTL}}$ output delay time	t_{DKRE}		3	19	ns
$\overline{\text{REFCTL}}$ output hold time	t_{HKRE}		3	19	ns
Data delay (from active, from CLKOUT ↓)	t_{HZKD}		2	20	ns
Data delay (from float, from CLKOUT ↓)	t_{LZKD}		2	20	ns
$\overline{\text{MIOCS}}$n output delay (from CLKOUT ↓)	t_{DKMS}		3	19	ns
$\overline{\text{MIOCS}}$n output hold time (from CLKOUT ↓)	t_{HKMS}		3	19	ns
$\overline{\text{BCYST}}$ output delay (from CLKOUT ↑)	t_{DKBC}		3	19	ns
$\overline{\text{BCYST}}$ output hold time (from CLKOUT ↑)	t_{HKBC}		3	19	ns
$\overline{\text{DA}}$ output delay (from CLKOUT ↑)	t_{DKDA}		3	19	ns
$\overline{\text{DA}}$ output hold time (from CLKOUT ↑)	t_{HKDA}		3	19	ns

TCU

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
TCLKn cycle	t_{CYTK}		100		ns
TCLKn high level width	t_{TKTKH}		30		ns
TCLKn low level width	t_{TKTKL}		45		ns
TCLKn rise time	t_{TKR}			15	ns
TCLKn fall time	t_{TKF}			15	ns
TCTLn high level width	t_{GGH}		50		ns
TCTLn low level width	t_{GGL}		50		ns
TOUT output delay (from TCTLn ↓)	t_{DGTO}			100	ns
TCTLn hold time	t_{HTKG}		100		ns
TCTLn setup time	t_{SGTK}		50		ns
TOUT output delay (from TCLKn ↓)	t_{DTKTO}			100	ns

SCU

Serial transfer

Parameter		Symbol	Conditions	MIN.	MAX.	Unit
Clock cycle		t_{CYS}		2t_{CYK}		ns
TxDn delay (from TxCLKn)		t_{DTKTD}			0.5	μs
Transmitter input clock pulse high level width	1 × BR	t_{TKTKH}		15t_{CYS}		ns
	16 ×, 64 × BR			3t_{CYS}		ns
Transmitter input clock pulse low level width	1 × BR	t_{TKTKL}		12t_{CYS}		ns
	16 ×, 64 × BR			1t_{CYS}		ns
Transmitter input clock frequency	1 × BR	f_{TK} Note			300	kHz
	16 × BR				1920	kHz
	64 × BR				1920	kHz
Receiver input clock pulse high level width	1 × BR	t_{RKRKH}		15t_{CYS}		ns
	16 ×, 64 × BR			3t_{CYS}		ns
Receiver input clock pulse low level width	1 × BR	t_{RKRKL}		12t_{CYS}		ns
	16 ×, 64 × BR			1t_{CYS}		ns
Receiver input clock frequency	1 × BR	f_{RK} Note			300	kHz
	16 × BR				1920	kHz
	64 × BR				1920	kHz
RxDn setup time (to sampling pulse)		t_{SRDSP}		1		μs
RxDn hold time (from sampling pulse)		t_{HSPRD}		1		μs

Note $\overline{\text{TxCLK}}$ and $\overline{\text{RxCLK}}$ frequencies have the following restriction:
1 × BR : f_{TK}, $f_{RK} \leq 1/30\ t_{CYS}$
16 ×, 64 × BR : f_{TK}, $f_{RK} \leq 1/4.5\ t_{CYS}$

Reamrks BR : Baud Rate

FLAG

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
TxRDYn delay (from TxRDY ↑)	t_{DTXR}			8tcys	ns
TxEMPn delay	t_{DTXEP}			20tcys	ns
RxRDYn delay (from RxRDY ↑)	t_{DRXR}			26tcys	ns

Remarks Status changes after a delay of 28 tcys max. following the occurrence of an effective event.

RxDn AND SYNCn

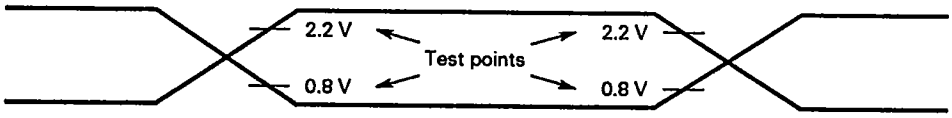
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SYNCn output delay (internally synchronized)	t_{DRKSY}			26tcys	ns
SYNCn input setup time (externally synchronized)	t_{SSYRK}		18tcys		ns

DMAU

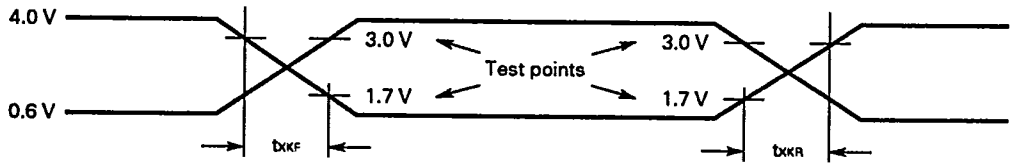
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
DMARQn setup time (to CLKOUT ↓)	t_{SDQK}		6		ns
DMARQn hold time (from CLKOUT ↓)	t_{HKDQ}		6		ns
DMAAKn output delay (from CLKOUT ↑)	t_{DKDAK}		3	19	ns
DMAAKn output hold time (from CLKOUT ↑)	t_{HKDAK}		3	19	ns
$\overline{TC}$n output delay (from CLKOUT ↑)	t_{DKTC}		3	19	ns
$\overline{TC}$n output hold time (from CLKOUT ↑)	t_{HKTC}		3	19	ns
$\overline{EOP}$n setup time (to CLKOUT ↓)	t_{SEK}		6		ns
$\overline{EOP}$n hold time (from CLKOUT ↓)	t_{HKE}		6		ns

AC CHARACTERISTICS

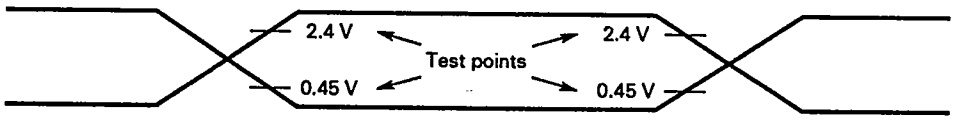
AC test input waveform (except X1 when external clock is used)



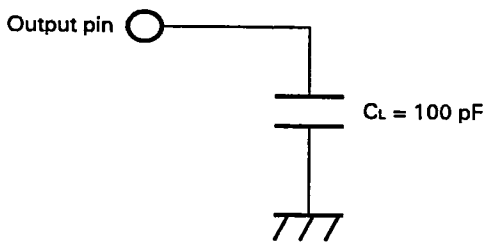
AC test input waveform (X1 when external clock is used)



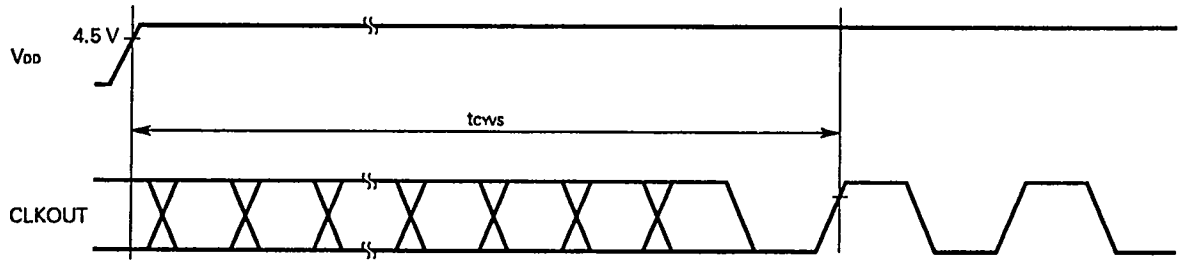
AC test output waveform



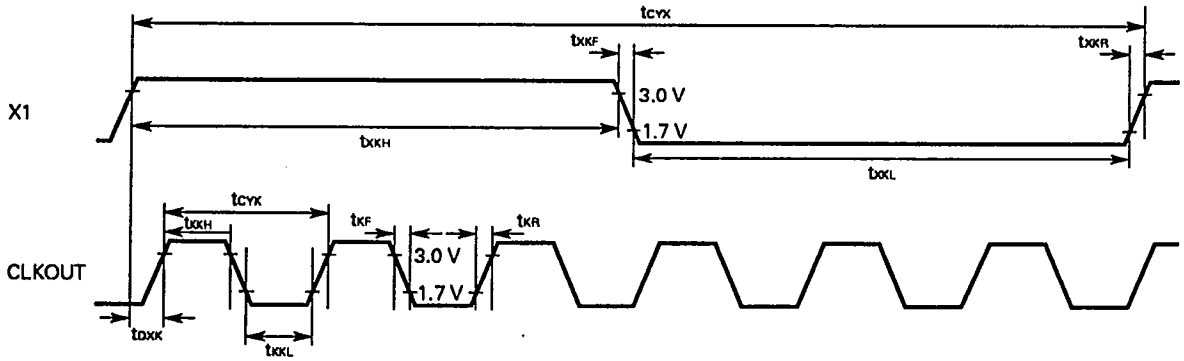
Test load



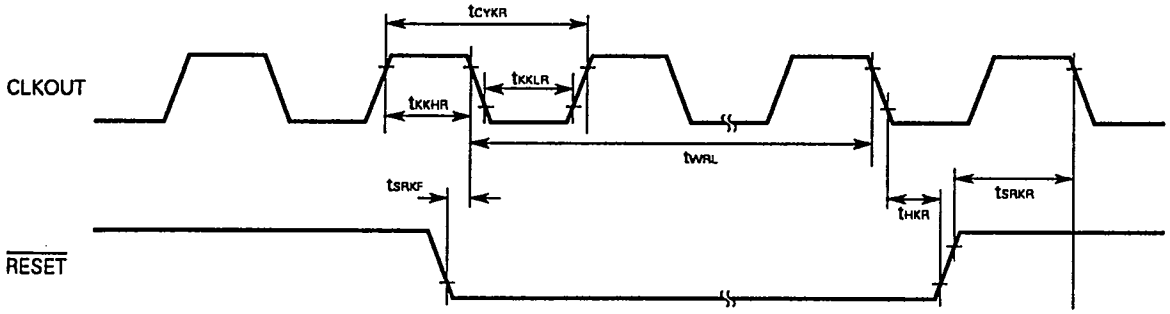
CLKOUT STABILIZATION TIME



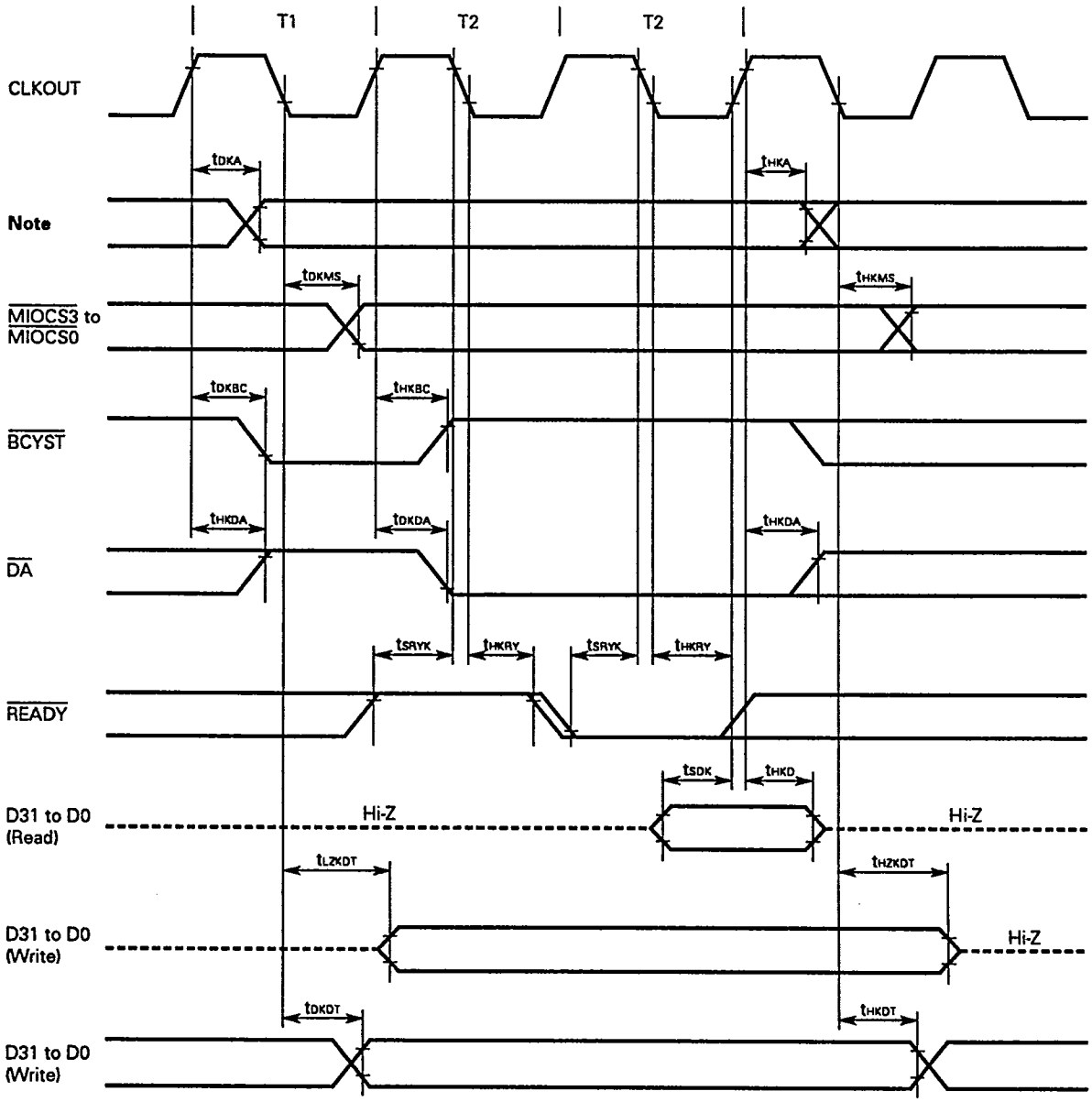
CLOCK TIMING



RESET TIMING

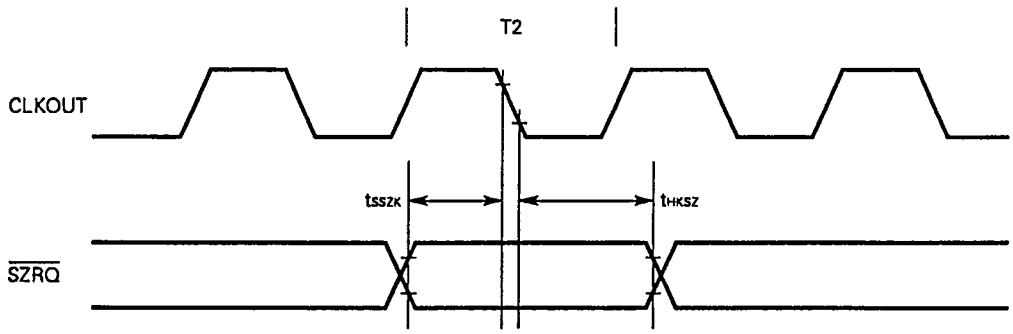


MEMORY, I/O ACCESS TIMING

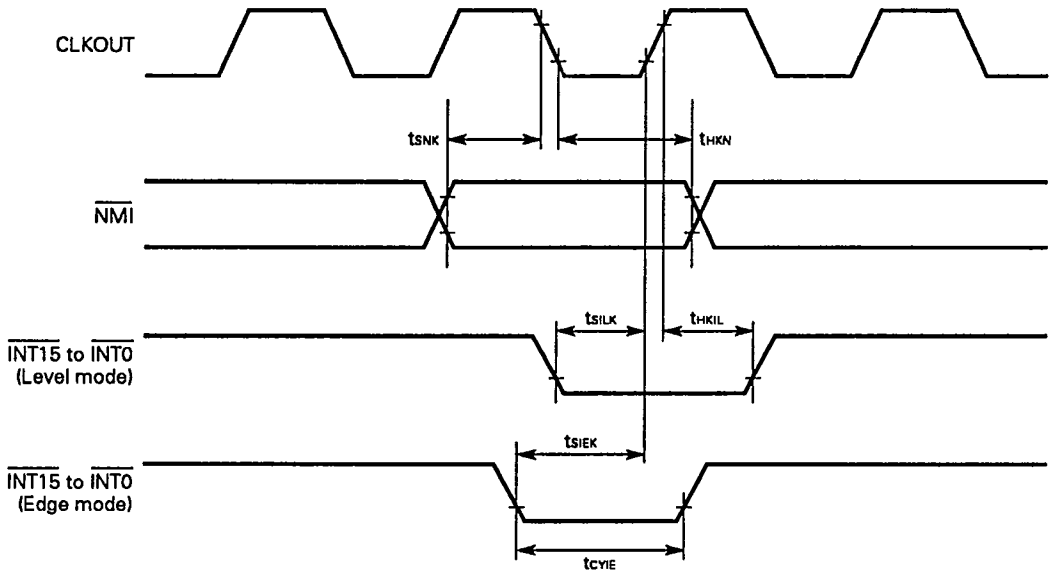


Note A31 - A1, $\overline{BE3}$ - $\overline{BE0}$, R/$\overline{W}$, $\overline{MRQ}$, ST1, ST0, XST1, XST0, BLOCK, $\overline{ADRSERR}$

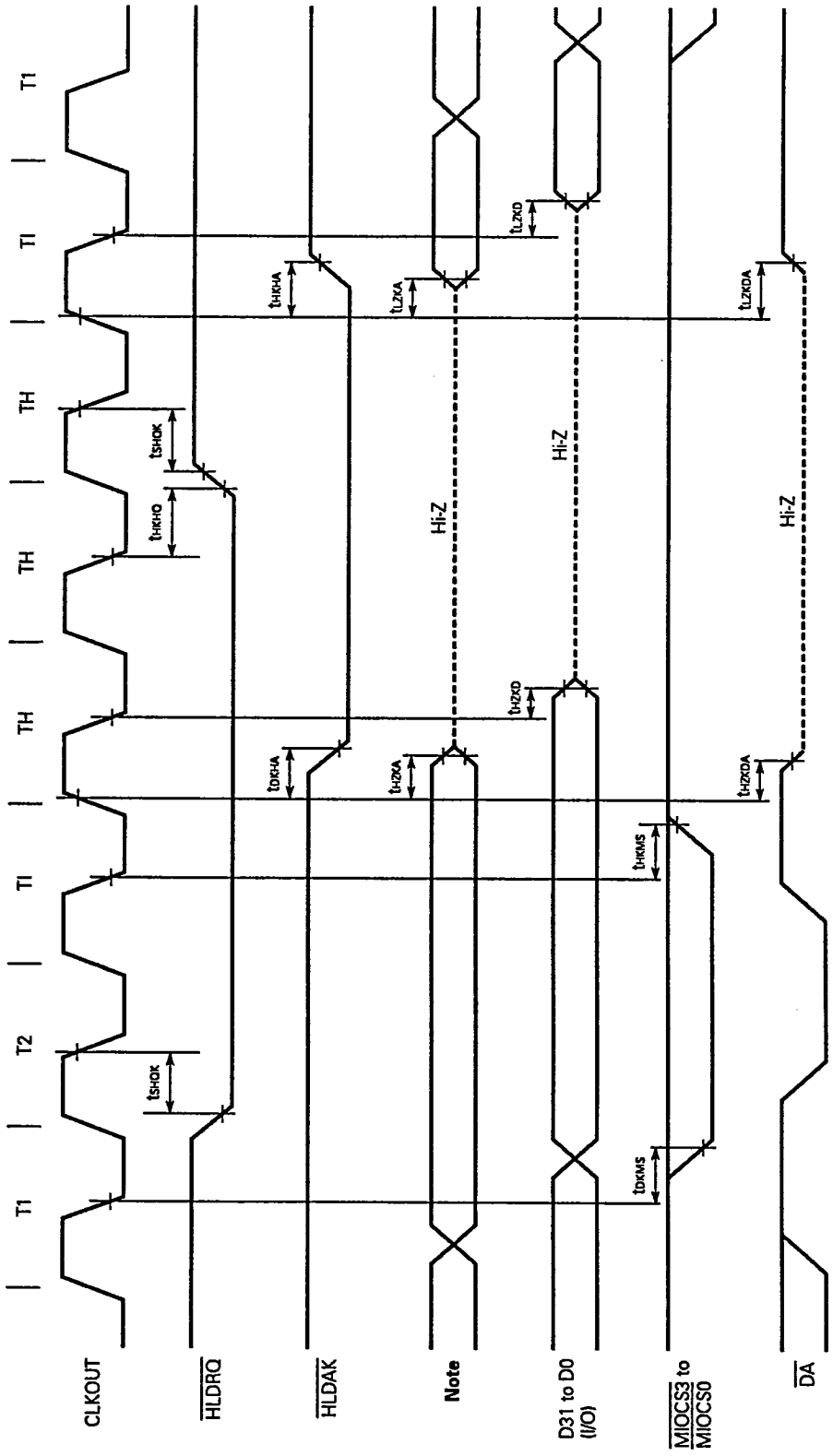
DYNAMIC BUS SIZING TIMING



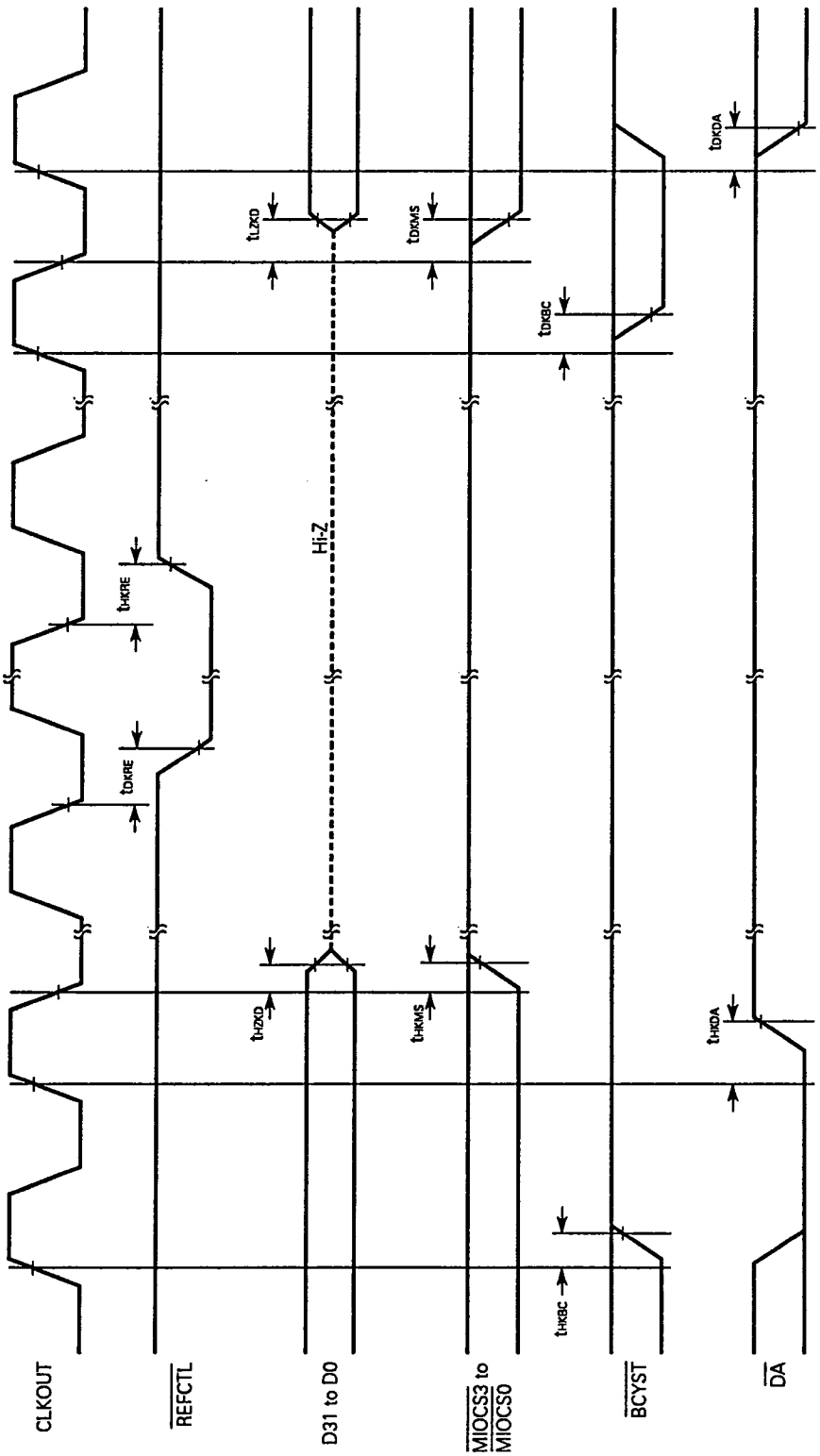
INTERRUPT TIMING



BUS HOLD TIMING



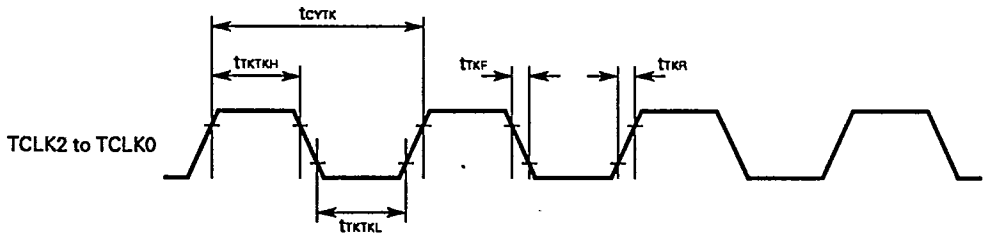
Note A31 - A1, $\overline{BE3}$ - $\overline{BE0}$, R/$\overline{W}$, $\overline{MRQ}$, ST1, ST0, XST1, XST0, $\overline{BCYST}$



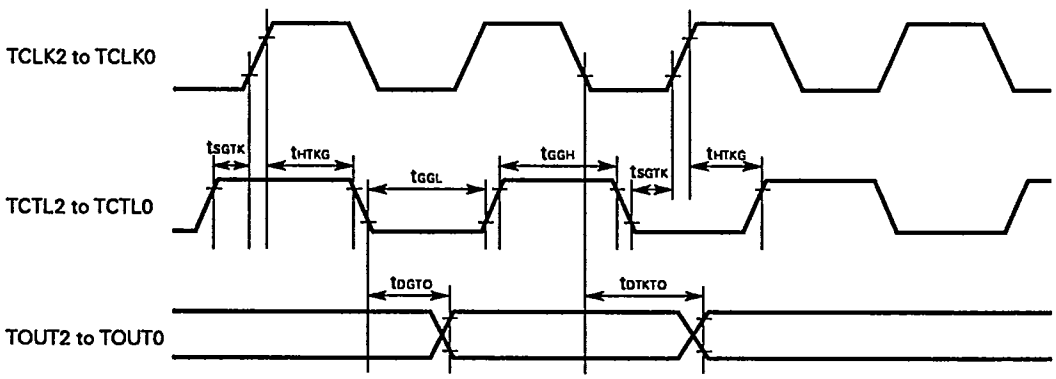
REFRESH TIMING

TCU TIMING

TCU Clock (TCLKn)

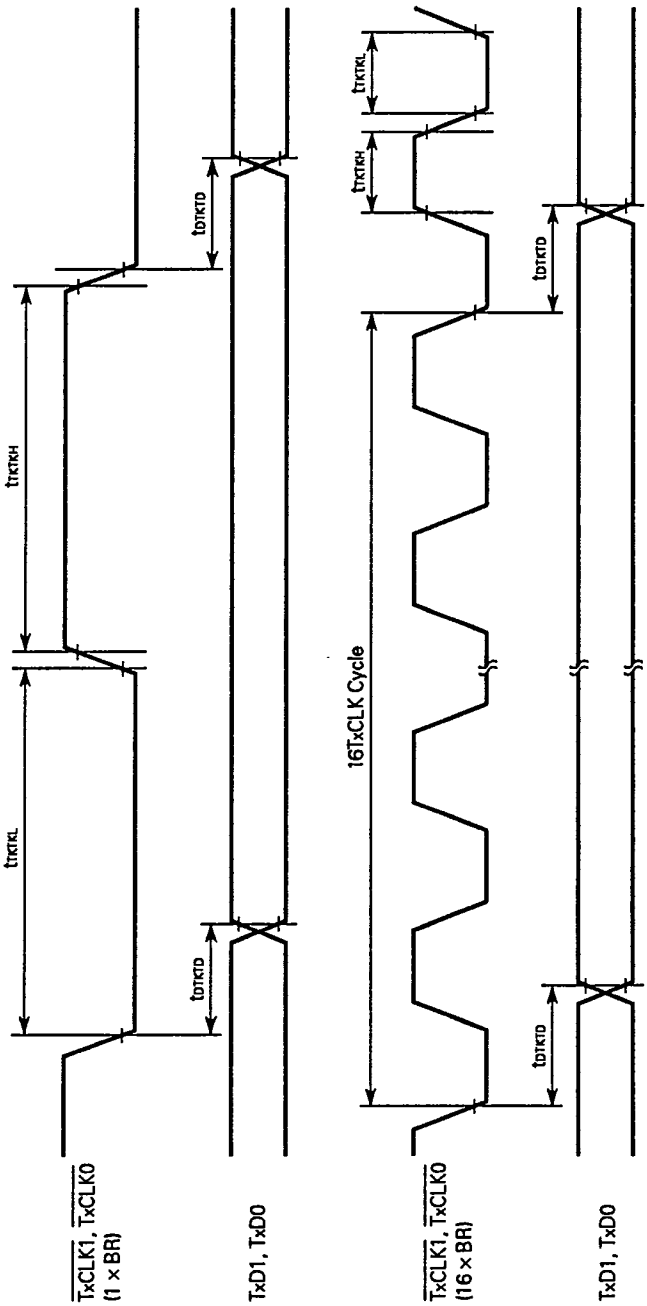


TCU Input/Output

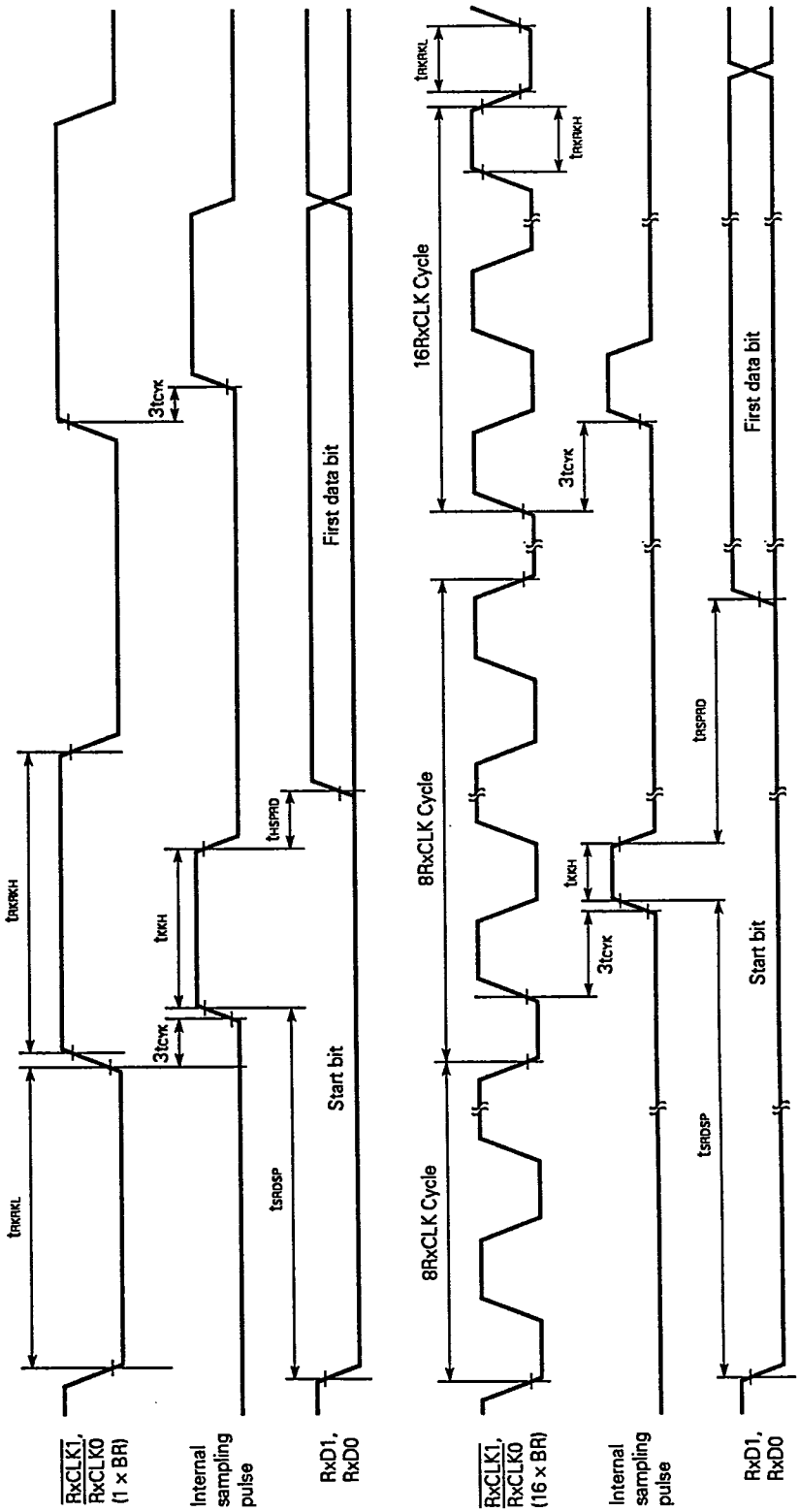


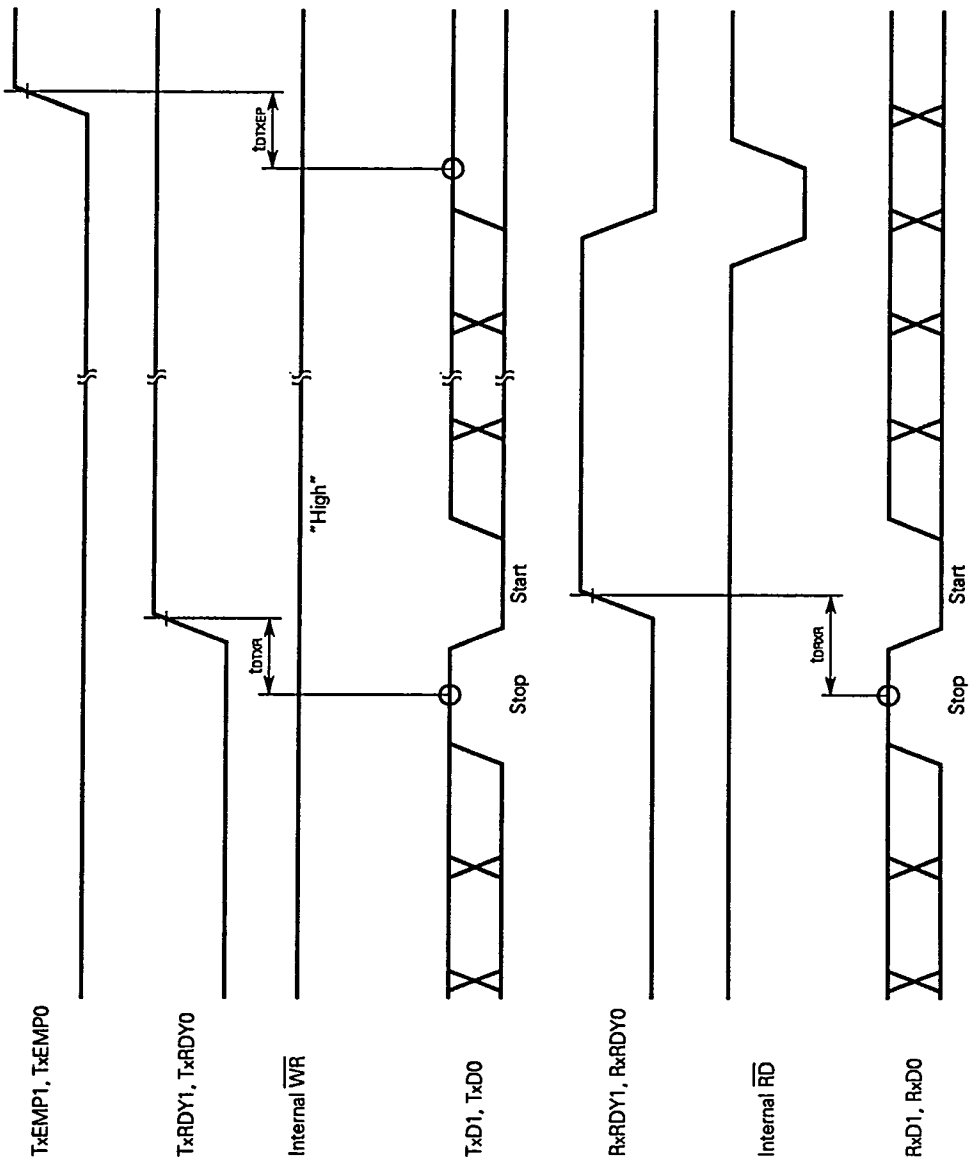
SCU TIMING

Transmitter Clock and TxDn



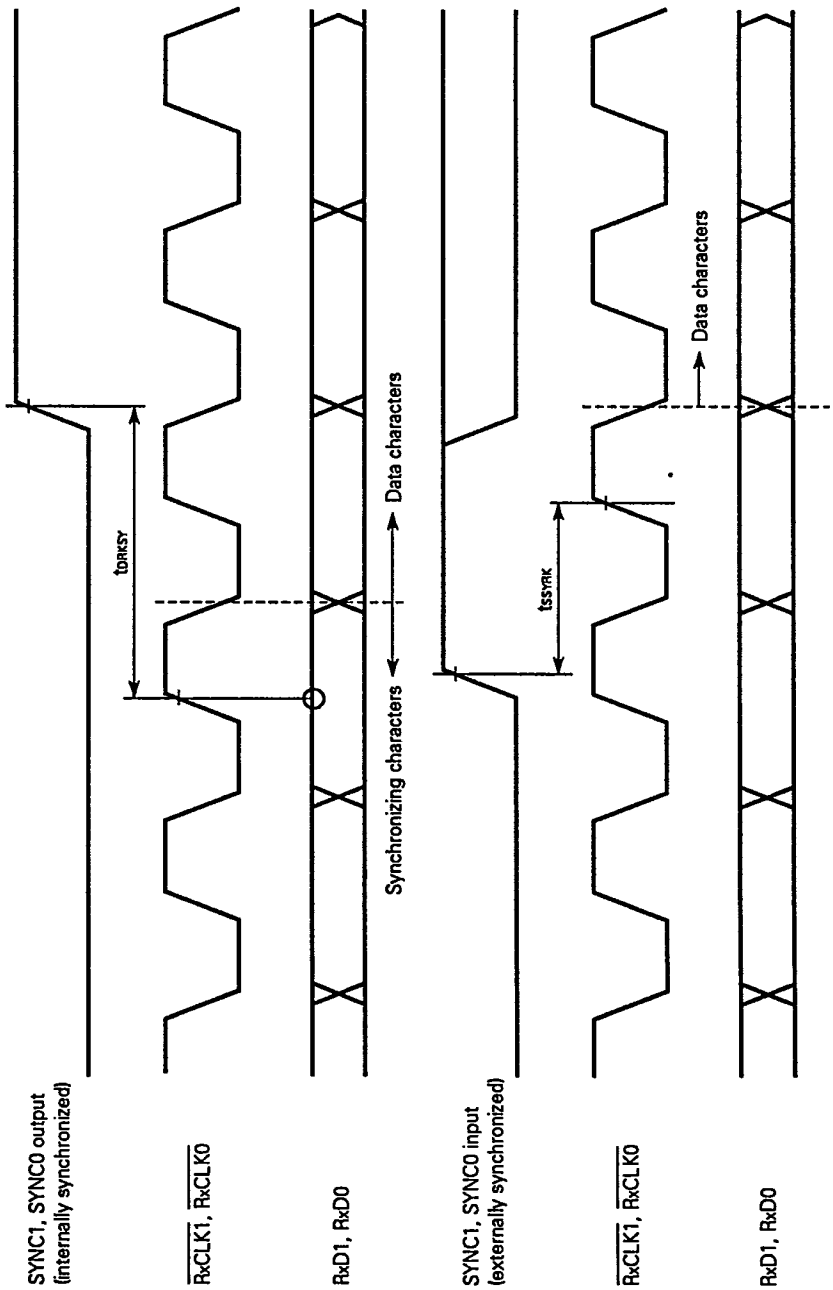
RECEIVER CLOCK AND RxDn

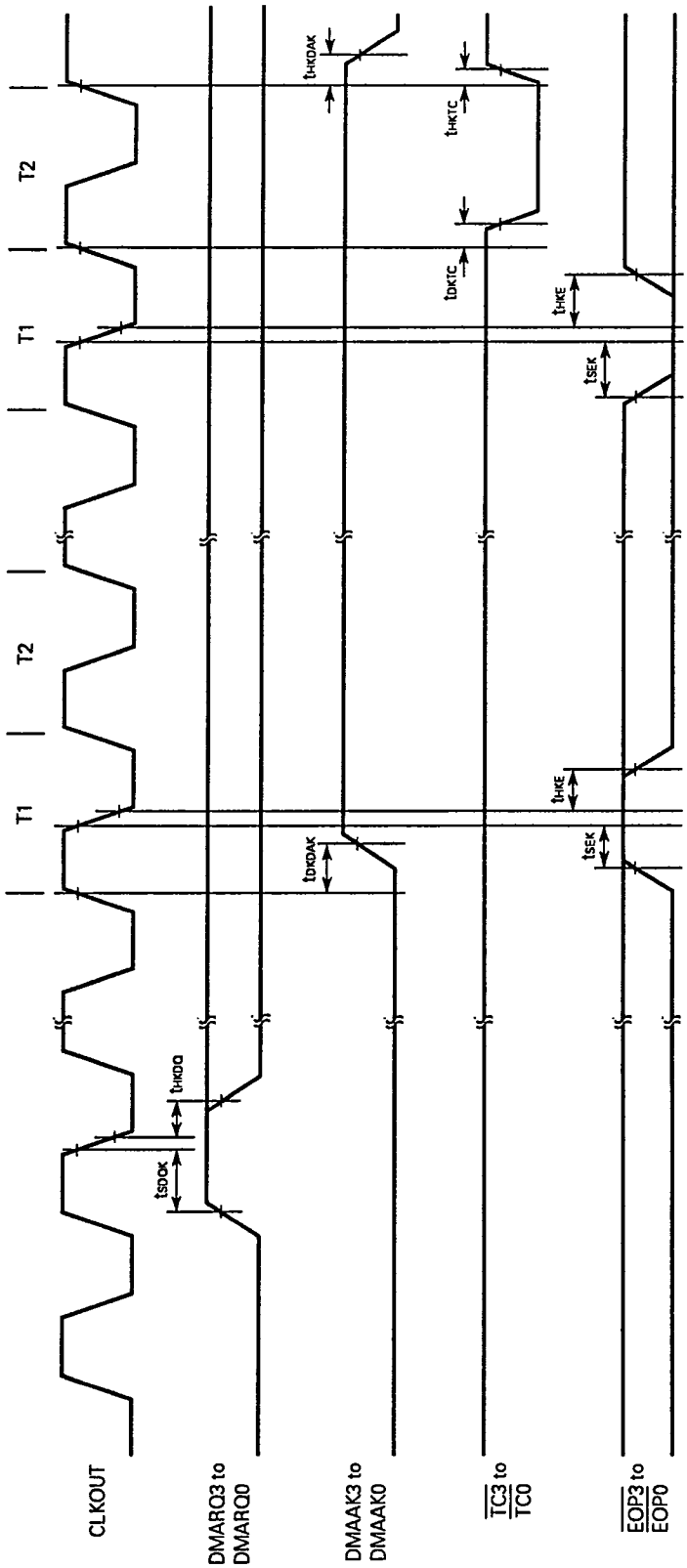




FLAG TIMING

RxDn AND SYNCn TIMINGS

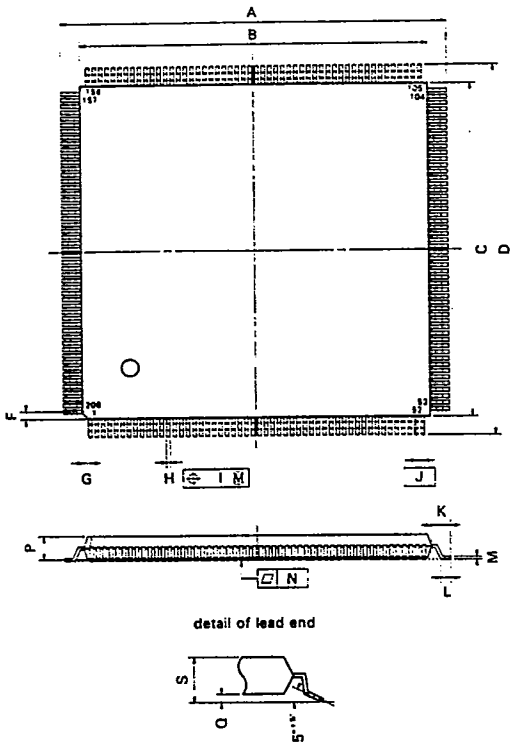




DMAU TIMING

9. PACKAGE DRAWINGS

208 PIN PLASTIC QFP(FINE PITCH)(□28)

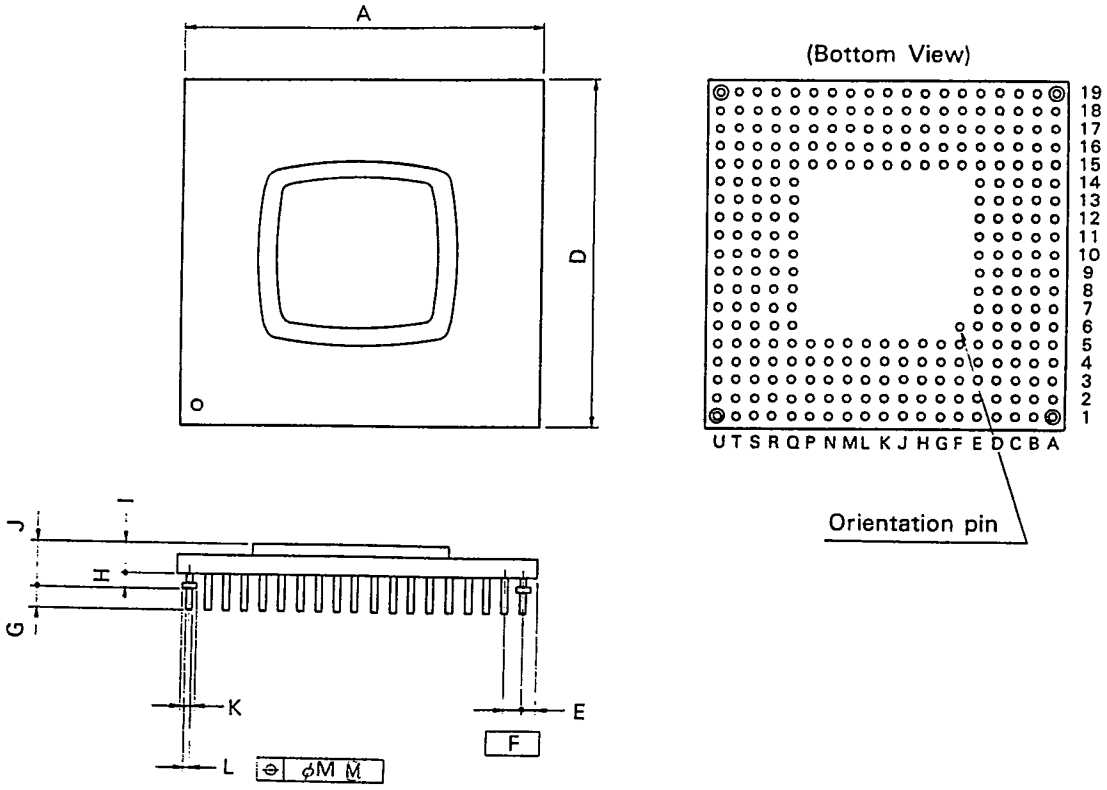


P208GD-50-LML. MML

NOTE
Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$30.6^{\pm 0.3}$	$1.205^{\pm 0.012}$
B	$28.0^{\pm 0.2}$	$1.102^{-0.009}_{-0.008}$
C	$28.0^{\pm 0.2}$	$1.102^{-0.009}_{-0.008}$
D	$30.6^{\pm 0.3}$	$1.205^{\pm 0.012}$
F	1.25	0.049
G	1.25	0.049
H	$0.20^{\pm 0.10}$	$0.008^{\pm 0.004}$
I	0.08	0.003
J	0.5 (T.P.)	0.020 (T.P.
K	$1.3^{\pm 0.2}$	$0.051^{\pm 0.008}$
L	$0.5^{\pm 0.2}$	$0.020^{-0.008}_{-0.009}$
M	$0.15^{\pm 0.05}$	$0.006^{\pm 0.002}$
N	0.1	0.004
P	3.2	0.126
Q	$0.4^{\pm 0.1}$	$0.016^{-0.004}_{-0.005}$
S	3.8 MAX.	0.150 MAX.

280PIN CERAMIC PGA



X280R-100A

NOTE
Each lead centerline is located within ϕ0.5 mm (ϕ0.020 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$48.26^{\pm 0.4}$	$1.900^{+0.016}_{-0.015}$
D	$48.26^{\pm 0.4}$	$1.900^{+0.016}_{-0.015}$
E	1.27	0.050
F	2.54 (T.P.)	0.100 (T.P.)
G	$2.8^{\pm 0.3}$	$0.110^{+0.012}_{-0.011}$
H	0.5 MIN.	0.019 MIN.
I	2.9	0.114
J	4.57 MAX.	0.180 MAX.
K	$\phi 1.2^{\pm 0.2}$	$\phi 0.047^{+0.008}_{-0.007}$
L	$\phi 0.46^{\pm 0.05}$	$\phi 0.018^{+0.002}_{-0.001}$
M	0.5	0.020

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.