Device type 01 inactive for new design as of 22 September 1978. Use M38510/31512B--.

REVISIONS

LTR	DESCRIPTION	DATE	APPROVED
C	Change maximum clock frequency (f_{MAX}), group A subgroups 10 and 11 at 15 pF from 20 MHz to 15 MHz and at 50 pF from 15 MHz to 13 MHz. Subgroups 10 and 11, t_{PHL2} at 15 pF from 35 ns to 38 ns max and t_{PLH2} at 15 pF from 31 ns to 34 ns max. Change to military drawing format. Editorial changes throughout. Add L_{CC} package. Remove vendors 27014, 07263, and 34335.	16 JUNE 1987	MLKoch

REV													
PAGE													
REV STATUS OF PAGES	REV	C	C	C	C	C	C	C	C	C	C	C	C
	PAGES	1	2	3	4	5	6	7	8	9	10	11	12

Defense Electronics Supply Center
Dayton, Ohio

Original date of drawing:
24 November 1976

AMSC N/A

PREPARED BY: Joe A. Kerby
CHECKED BY: Dan Di Cenzo
APPROVED BY: MLKoch

SIZE: A
CODE IDENT. NO.: 14933
REV: C

MILITARY DRAWING

This drawing is available for use by all Departments and Agencies of the Department of Defense

TITLE: MICROCIRCUITS, DIGITAL, LOW POWER SCHOTTKY TTL, COUNTER, MONOLITHIC SILICON

DWG NO. 76034

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5962-E253

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

76034	01	E	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54LS163	Synchronous 4-bit decade counter with synchronous clear

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
E	D-2 (16-lead, 1/4" x 7/8"), dual-in-line package
F	F-5 (16-lead, 1/4" x 3/8"), flat package
2	C-2 (20-terminal .350" x .350"), square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc at -18 mA to 5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) per device 1/	175 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Cases E and F	(See MIL-M-38510, appendix C)
Case 2	80°C/W 2/
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V_{IH})	2.0 V dc
Maximum low-level input voltage (V_{IL})	0.7 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short-circuit test (e.g., I_{OS}).
2/ When a thermal resistance is specified in MIL-M-38510, appendix C, that value shall supersede the value specified herein.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
High-level output voltage	V_{OH}	V_{CC} = 4.5 V; I_{OH} = -400 µA V_{IN} = 0.7 V or 2.0 V		1,2,3	2.5		V
Low-level output voltage	V_{OL}	V_{CC} = 4.5 V; I_{OL} = 4 mA V_{IN} = 0.7 V or 2.0 V		1,2,3		0.4	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V; I_{IN} = -18 mA T_C = +25°C		1		-1.5	V
High-level input current at data or enable P	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.7 V		1,2,3		20	µA
	I_{IH2}	V_{CC} = 5.5 V, V_{IN} = 5.5 V		1,2,3		100	µA
High-level input current at load, clock, enable T, or clear	I_{IH3}	V_{CC} = 5.5 V, V_{IN} = 2.7 V		1,2,3		40	µA
	I_{IH4}	V_{CC} = 5.5 V, V_{IN} = 5.5 V		1,2,3		200	µA
Low-level input current at data or enable P	I_{IL1}	V_{CC} = 5.5 V, V_{IN} = 0.4 V		1,2,3		-.40	mA
Low-level input current at load, enable T, or clear	I_{IL2}	V_{CC} = 5.5 V, V_{IN} = 0.4 V		1,2,3		-.80	mA
Low-level input current at clock	I_{IL3}	V_{CC} = 5.5 V, V_{IN} = 0.4 V		1,2,3		-1.2	mA
Short-circuit output current	I_{OS}	V_{CC} = 5.5 V 1/ V_{OUT} = 0.0 V		1,2,3	-15	-130	mA
Current supply	I_{CCH}	V_{CC} = 5.5 V		1,2,3		31	mA
	I_{CCL}	V_{CC} = 5.5 V		1,2,3		32	mA
Functional tests		See 4.3.1c		7			
Maximum clock frequency	f_{MAX}	V_{CC} = 5.0 V R_L = 2 kΩ ±5%	C_L = 15 pF ±10%	9	25		MHz
				10,11	15		MHz
			C_L = 50 pF ±10%	9	20		MHz
				10,11	13		MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Propagation delay time, high-to-low level output from clock to ripple carry 2/	t_{PHL1}	V_{CC} = 5.0 V, R_L = 2 kΩ ±5%	C_L = 15 pF ±10%	9		35	ns
				10,11		49	ns
			C_L = 50 pF ±10%	9		40	ns
				10,11		56	ns
Propagation delay time, low-to-high level output from clock to ripple carry 2/	t_{PLH1}		C_L = 15 pF ±10%	9		35	ns
				10,11		49	ns
			C_L = 50 pF ±10%	9		40	ns
				10,11		56	ns
Propagation delay time, high-to-low level output from clock (load input high) to any Q 2/	t_{PHL2}		C_L = 15 pF ±10%	9		27	ns
				10,11		38	ns
			C_L = 50 pF ±10%	9		32	ns
				10,11		42	ns
Propagation delay time, low-to-high level output from clock (load input high) to any Q 2/	t_{PLH2}		C_L = 15 pF ±10%	9		24	ns
				10,11		34	ns
			C_L = 50 pF ±10%	9		29	ns
				10,11		38	ns
Propagation delay time, high-to-low level output from clock (load input low) to any Q 2/	t_{PHL3}		C_L = 15 pF ±10%	9		29	ns
				10,11		49	ns
			C_L = 50 pF ±10%	9		34	ns
				10,11		48	ns

See footnotes at end of table.

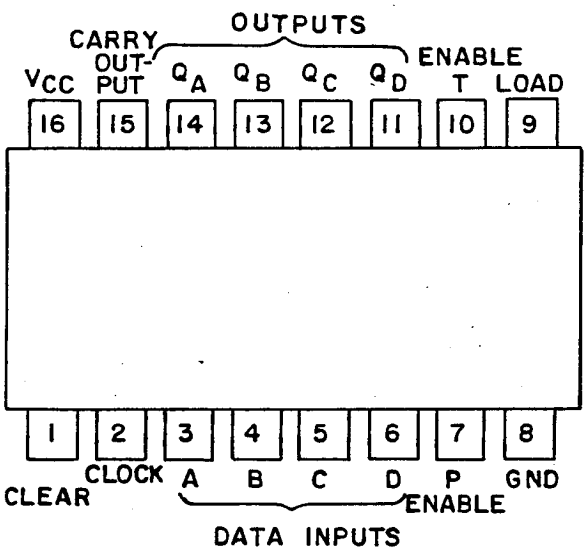
TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Group A subgroups	Limits Min	Limits Max	Unit
Propagation delay time, low-to-high level output from clock (load input low) to any Q 2/	t_{PLH3}	V_{CC} = 5.0 V, R_L = 2 kΩ ±5%	C_L = 15 pF ±10%	9		25	ns
				10,11		35	ns
			C_L = 50 pF ±10%	9		30	ns
				10,11		42	ns
Propagation delay time, high-to-low level output from enable T to ripple carry 2/	t_{PHL4}		C_L = 15 pF ±10%	9		16	ns
				10,11		22	ns
			C_L = 50 pF ±10%	9		21	ns
				10,11		29	ns
Propagation delay time, low-to-high level output from enable T to ripple carry 2/	t_{PLH4}		C_L = 15 pF ±10%	9		16	ns
				10,11		22	ns
			C_L = 50 pF ±10%	9		21	ns
				10,11		29	ns
Propagation delay time, high-to-low level output from clear to any Q 2/	t_{PHL5}		C_L = 15 pF ±10%	9		28	ns
				10,11		39	ns
			C_L = 50 pF ±10%	9		33	ns
				10,11		46	ns

1/ Not more than one output should be shorted at a time, and the duration of the short-circuit condition should not exceed one second.

2/ Propagation delay time testing and maximum clock frequency testing may be performed using either C_L = 15 pF or C_L = 50 pF. However, the manufacturer must certify and guarantee that the microcircuits meet the switching test limits specified for a 50-pF load.

Cases E and F



Case 2

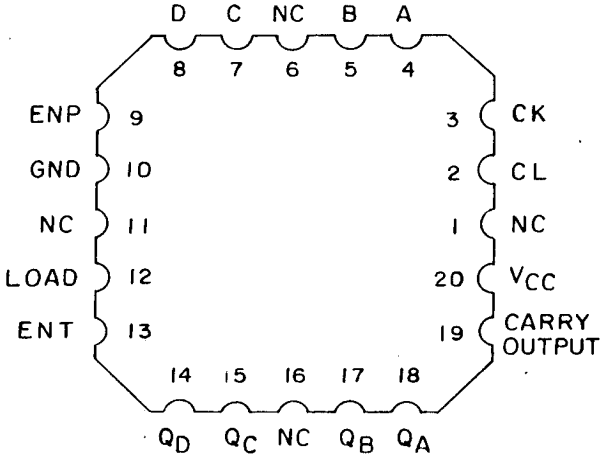


FIGURE 1. Terminal connections.

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Load	Enable T	Enable P	Action on the rising clock edge (⌠)
X	X	X	Reset (clear)
L	X	X	Load ($Data_n$ - Q_n)
H	H	H	Count (Increment)
H	L	X	No change (Hold)
H	X	L	No change (Hold)

H = High voltage level
L = Low voltage level
X = Don't care

FIGURE 2. Truth table.

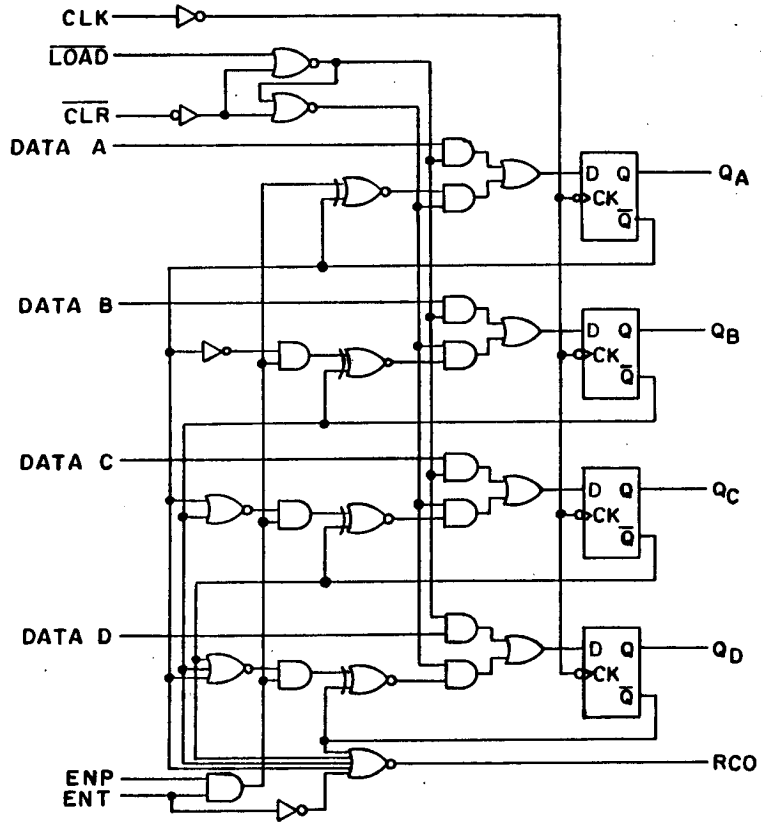

FIGURE 3. Logic diagram.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D, using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 7 tests shall verify the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 9 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/31512B--.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, OH 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
7603401EX 2/	01295 18324 04713	SNJ54LS163AJ 54LS163A/BEA 54LS163ABEXJC	M38510/31512BEX
7603401FX 2/	01295 18324 04713	SNJ54LS163AW 54LS163A/BFA 54LS163ABFXJC	M38510/31512BFX
76034012X 2/	01295 18324 04713	SNJ54LS163AFK 54LS163A/B2C 54LS163AM/B2XJC	M38510/31512B2X

1/ CAUTION. Do not use this number for item acquisition. Items acquired to the vendor similar part number only may not satisfy the performance requirements of this drawing.

2/ Inactive for new design. Use QPL-38510 product.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. P.O. Box 6448 Midland, TX 79701
18324	Signetics Corporation 4130 South Market Court Sacramento, CA 95834
04713	Motorola, Inc. 7402 S. Price Road Tempe, AZ 85283