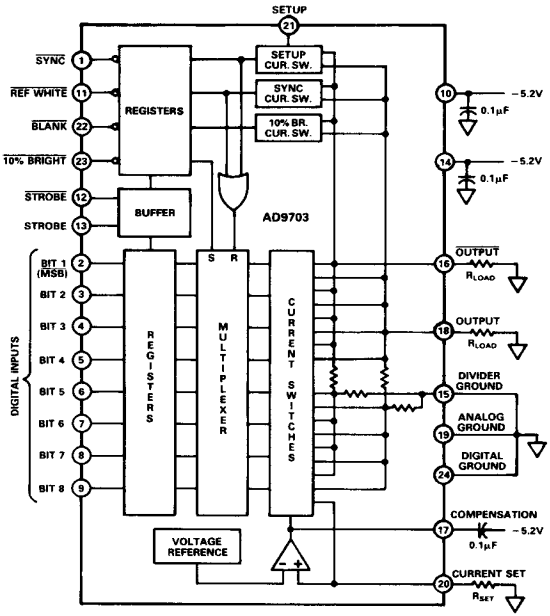
Monolithic Video D/A Converter

AD9703

FEATURES
Update Rates of 300MHz+
Ultra-Low Glitch Impulse
Synchronous Composite Functions
Raster Graphics Complete
Mil Spec Versions Available

APPLICATIONS
Radar/Raster Scan Displays
Color Graphics
Automated Test Equipment
2D/3D Workstations
FLIR/Heads-Up Displays
Medical Imaging

AD9703 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9703 D/A Converter is a state-of-the-art monolithic digital-to-analog converter capable of accepting 8 bits of digital data at update rates of 300MHz. It is designed specifically for ultra-high-performance, high-resolution raster graphics systems but can also be used for other applications which require low glitch, such as waveform generation.

It comes complete with synchronized composite functions including sync, blank, reference white, and 10% bright. The reference white input forces the analog output to the reference white level regardless of the data inputs. The 10% bright input can be used to generate a white cursor on a white background.

Synchronization of the inputs prevents short or missing pixels. Multiplexing video functions from synchronized inputs eliminates recovery times and the need to reset registers. This unique feature is different from most data input register designs and materially enhances the performance of the AD9703.

An on-board reference eases design effort by eliminating the need for external circuits. Input registers and a differential clock input minimize glitch impulse and clock feedthrough. The unit is housed in a 24-pin DIP and will operate in both 10KH and 100K ECL systems. The AD9703 dissipates 1.1 watts and is truly a "graphics ready" device.

Analog Devices' advanced technology produced the first hybrid converters which included composite capabilities; the AD9703 is one of a series of monolithic graphics DACs made by the company. (The AD9701 is an 8-bit 250MHz device; the AD9702 is a triple 4-bit 125MHz converter.)

SPECIFICATIONS (typical @ +25°C and nominal power supplies unless otherwise noted)

Model	AD9703BD/BW		AD9703TD/TDB
ABSOLUTE MAXIMUM RATINGS	Lower	Upper	
Supply Voltages			
Pins 10 and 14 (V_S)	−6V	0V	*
Power Dissipation (Continuous)	1.75W		*
Logic Inputs	$-V_S$	Ground	*
Current Set	1mA	4.5mA	*
Output Current	30mA		*
Setup	$-V_S$	Ground	*
Temperature			
Operating (Case)	−25°C to +85°C		−55°C to +125°C
Storage	−65°C to +150°C		*
Junction Temperature	+175°C		*
Lead (Soldering, 10sec)	+300°C		*

Parameter	Units	AD9703BD/BW	AD9703TD/TDB
RESOLUTION	Bits	8	*
LEAST SIGNIFICANT BIT (LSB) WEIGHT			
Voltage (Adjustable)	mV	2.5	*
Currrent (Adjustable)	μA	67	*
ACCURACY (GS = Gray Scale; FS = Full Scale)			
Differential Linearity	± % GS, max	0.2	*
Integral Linearity	± % GS, max	0.2	*
Zero Offset Voltage (Initial)	± mV, max	2	*
Monotonicity		Guaranteed	*
TEMPERATURE COEFFICIENTS			
Linearity	ppm/°C	7	*
Gain	ppm/°C	170	*
Zero Offset	μV/°C	5	*
DYNAMIC CHARACTERISTICS – GRAY SCALE OUTPUT			
Full-Scale Settling to 0.4% GS[1]	ns	6	*
Update Rate[2]	MHz (Guaranteed)	300 (250)	*
Rise Time (10%–90% GS)	ns (max)	1.2 (1.75)	*
Fall Time (10%–90% GS)	ns (max)	1.1 (1.75)	*
Glitch Impulse	pV-s (max)	45 (55)	*
Clock Feedthrough	mV	<10	*
DIGITAL DATA INPUTS			
Logic Compatability		100K and 10KH ECL	*
Coding		Complementary Binary (CBN)	*
Logic Levels			
"1"	V	−0.9	*
"0"	V	−1.7	*
Loading (Each Bit)		5pF and 50kΩ to −5.2V	*
STROBE INPUT(S)			
Logic Compatibility		100K and 10KH ECL	*
Coding		Complementary Binary (CBN)	*
Logic Levels			
"1"	V	−0.9	*
"0"	V	−1.7	*
Loading		5pF and 50kΩ to −5.2V	*
Setup Time (Data)	ns	0	*
Hold Time (Data)	ns, min	1	*
Propagation Delay			
(Strobe Input to Analog Output)	ns	1.2	*
10% BRIGHT, REFERENCE WHITE, COMPOSITE SYNC, AND COMPOSITE BLANKING INPUTS			
Logic Compatibility		100K and 10KH ECL	*
Coding		Complementary Binary (CBN)	*
Logic Levels			
"1"	V	−0.9	*
"0"	V	−1.7	*
Loading		5pF and 50kΩ to −5.2V	*
SPEED PERFORMANCE – CONTROL INPUTS[1]			
Settling Time to 10% of Final Value for:			
10% Bright	ns	6	*
Reference White	ns	6	*
Composite Sync	ns	6	*
Composite Blanking	ns	6	*
SETUP CONTROL			
Ground	mV (IRE Units)	0 (0)	*
Open	mV (IRE Units)	53.25 (7.5)	*
1k to −5.2V	mV (IRE Units)	71 (10)	*
−5.2V	mV (IRE Units)	142 (20)	*

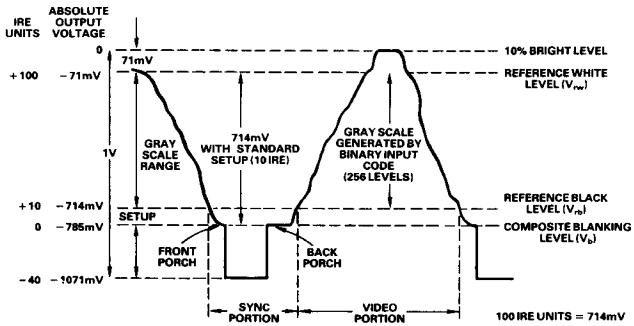
Parameter	Units	AD9703BD/BW	AD9703TD/TDB
ANALOG OUTPUT			
GS Current[3]	mA	0 to −17	*
GS Voltage[4,5]	mV	0 to −637.5	*
Compliance[6]	V	−1.2 to +3	*
Internal Impedance	Ω	800	*
REFERENCE WHITE[7]			
Current			
Logic "1"	mA	Normal Operation	*
Logic "0"	mA	0 or −1.9	*
Voltage			
Logic "1"	mV	Normal Operation	*
Logic "0"	mV	0 or −71.25	*
10% BRIGHT[8]			
Current			
Logic "1"	mA	−1.9	*
Logic "0"	mA	0	*
Voltage			
Logic "1"	mV	−71	*
Logic "0"	mV	0	*
COMPOSITE SYNC[8,9]			
Current			
Logic "1"	mA	0	*
Logic "0"	mA	−7.6	*
Voltage			
Logic "1"	mV	0	*
Logic "0"	mV	−285	*
COMPOSITE BLANKING[8,9]			
(Assumes Setup is Open, Which is Equivalent to 7.5 IRE Units)			
Current			
Logic "1"	mA	0	*
Logic "0"	mA	−1.42	*
Voltage			
Logic "1"	mV	0	*
Logic "0"	mV	−53.25	*
VOLTAGE REFERENCE TOLERANCE			
(Deviation from Nominal −1.26V)	mV (max)	±20 (±60)	*
POWER REQUIREMENTS			
−5.2V (Min/Max = −4.5V/−5.45V)	mA (max)	210 (275)	*
Power Supply Rejection Ratio	mV/V	1	*
Power Dissipation	W (max)	1.1 (1.43)	*
TEMPERATURE RANGE	°C	−25 to +85	−55 to +125
THERMAL RESISTANCE[10]			
Junction to Air, θ_{JA} (Free Air)	°C/W	29	*
Junction to Case, θ_{JC}	°C/W	12	*
MTBF[11]			
Mean Time Between Failures	Hours	3.04×10^5	*
PACKAGE OPTIONS[12]			
D-24		AD9703BD AD9703BW	AD9703TD AD9703TDB

NOTES
[1]Inherent register delay (50% points) is not included.
[2]Maximum update rate limited by input registers.
[3]FS Current = GS Current + Video Functions = 30mA maximum.
[4]LSB value of 2.5mV used for calibration. This causes Gray Scale output to be 637.5mV, rather than 643mV of idealized composite waveform shown elsewhere. $I_{OUT} = 4(1.26/R_{SET})$ when $R_{SET} = 300\Omega$.
[5]Output voltages based on $R_{LOAD} = 75\Omega \| R_{TERMINATION} = 75\Omega$.
[6]Divider Ground (Pin 15) must be at +3V for +3V compliance. (See text.)
[7]The effect on the analog output of logic "0" at Reference White input (Pin 11) depends on signal at 10% Bright input (Pin 23).
[8]10% Bright, Composite Sync, and Composite Blanking outputs add to analog output.
[9]Composite Sync and/or Composite Blanking signals override input registers. Neither of these signals should be operated simultaneously with Reference White.
[10]Maximum junction temperature is +175°C.
[11]Calculated using MIL HNBK-217; Ground; Fixed; +25°C Ambient.
[12]See Section 14 for package outline information.
Specifications subject to change without notice.

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	COMPOSITE SYNC	24	DIGITAL GROUND
2	BIT 1	23	10% BRIGHT
3	BIT 2	22	COMPOSITE BLANK
4	BIT 3	21	SETUP
5	BIT 4	20	CURRENT SET
6	BIT 5	19	ANALOG GROUND
7	BIT 6	18	I_{OUT}
8	BIT 7	17	COMPENSATION
9	BIT 8	16	$\overline{I_{OUT}}$
10	−5.2V	15	DIVIDER GROUND
11	REFERENCE WHITE	14	−5.2V
12	STROBE	13	STROBE

NOTE: CONNECT PINS 15, 19, AND 24 TOGETHER AND TO GROUND AS CLOSE TO CASE AS POSSIBLE.



Idealized Composite Output Waveform

USING AD9703 AS RASTER SCAN D/A

Refer to the block diagram of the AD9703. The digital input bits applied to Pins 2 through 9 represent the Gray Scale value of the 256 (2^8) discrete levels between Reference Black and Reference White in a composite video signal.

The (true and complementary) analog outputs are also affected by the 100K or 10KH ECL levels at the control inputs, and the level (in IRE units) of the control signal at SETUP, Pin 21.

STROBE and $\overline{\text{STROBE}}$ signal pulses clock the input registers to remove time skew from the digital input bits and minimize discontinuities or "glitches" in the analog output.

In the idealized waveform, the full-scale output is −643mV. Normal fullscale output of the AD9703, however, is −637.5mV because of using 2.5mV for the weight of the LSB during calibration of the unit. Both values are well within the tolerances of the output and the RS-170 standard.

The internal voltage reference shown in the block diagram is a bandgap type and eliminates the need for external circuits. Other benefits of the internal precision reference include superior power supply rejection and gain tempco.

The value of the internal reference is 1.26 volts (±20mV; ±60mV max), and that knowledge can be combined with information on Gray Scale output current to determine the value of the R_{SET} resistor. R_{SET} is approximately four times the value of the number which results when the reference voltage is divided by the Gray Scale current. Expressed mathematically:

$$R_{SET} \approx 4\left(\frac{1.26V}{I_{OUT}GS}\right)$$

Assume the user's desired Gray Scale voltage is 637.5mV; and the external load is 37.5 ohms. Dividing 637.5mV by 37.5 ohms sets Gray Scale current at 17mA. The reference voltage of 1.26 volts divided by 17mA, and multiplied by four, determines a (rounded) R_{SET} value of 296 ohms.

Full-scale current is Gray Scale current **plus** the video functions and is specified for a **total** of 30mA.

Using the value of R_{SET}, the user can calculate Gray Scale output voltage within 15% with the equation:

$$V_{OUT} = 4\left(\frac{1.26V}{R_{SET}}\right)\left(R_{LOAD} \parallel R_{INTERNAL}\right)$$

The resistance of the internal ladder is 800 ohms in parallel with the load resistor and is included in the above example.

APPLICATION HINTS

In the Specifications, data on $\overline{\text{COMPOSITE BLANKING}}$ assume the SETUP connection is open, equivalent to 7.5 IRE Units. Pin 20 connected to ground is equivalent to 0 IRE Units. Connecting to −5.2V through a 1kΩ resistor is 10 units; connecting to −5.2V directly is 20 units.

For some applications, additional by-pass capacitors for the −5.2V supply lines may be desirable. In addition to the ceramic 0.1μF capacitors shown on the block diagram, tantalum capacitors of 3.3 − 10μF may enhance the converter's performance in some designs. All by-pass capacitors should be connected as closely as possible to the supply pins of the converter.

If the user is driving a lighter load than a coaxial cable and needs lower power dissipation, doubling the value of R_{SET} halves the output current but still maintains useable drive.

Ground pins 15, 19, and 24 are normally connected together and to ground; these connections should also be made close to the unit. Divider Ground must be referenced to +3V to obtain +3V compliance. Figure 1 shows a method of doing this.

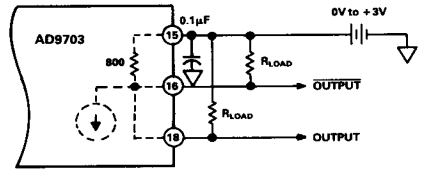


Figure 1. Connection for Positive Voltage Compliance

Values of up to +3V might be applied. Assume R_{LOAD} is 75 ohms. With +1V applied, the output would be ±1V; at +3V, the output would be +1V to +3V.

USING AD9703 AS STANDARD D/A

The AD9703 can also be used as a standard D/A converter capable of remarkable performance; it is attractive for that application because of the low value of glitch impulse.

Refer to Figure 2.

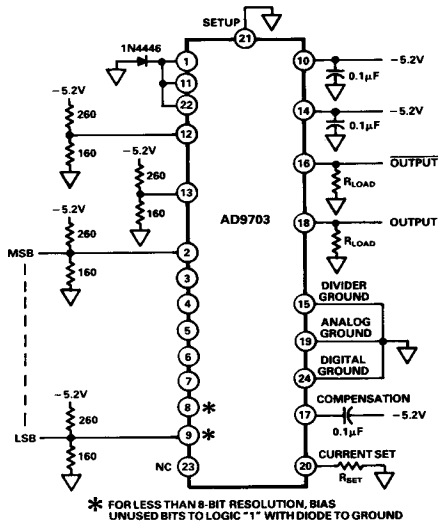


Figure 2. AD9703 as Standard D/A

As a standard D/A, unused control inputs are tied to ground via a diode as shown on Pins 1, 11, and 22. The $\overline{\text{10\% Bright}}$ input (Pin 23) is left open; and Setup (Pin 21) is tied directly to ground. For less than eight bits of data, unused input pins are also grounded via diodes.

ORDERING INFORMATION

Three versions of the AD9703 are available, all in ceramic DIP packages. The non-hermetic AD9703BW and hermetic AD9703BD operate over a temperature range of −25°C to +85°C. The hermetic AD9703TD and mil-processed AD9703TDB are for −55°C to +125°C.