

Features

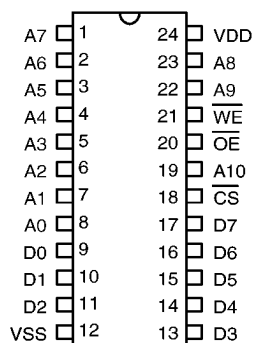
- Single 5V power supply
- Low power consumption
 - Operating: 400mW (Typ.)
 - Standby: 5μW (Typ.)
- 70ns (Max.) high speed access time
- Power down by pin CS
- TTL compatible interface levels
- Fully static operation
- Memory expansion by pin $\overline{\text{OE}}$
- Common I/O using tri-state outputs
- Pin-compatible with standard 2Kx8 bits of EPROM/MASK ROM
- 24-pin DIP/SDIP/SOP package

General Description

The HT6116-70 is a 16384-bit static random access memory. It is organized with 2048 words of 8 bits in length, and operates with a single 5V power supply. The IC is built with a high performance CMOS 0.8 μ m process in order to obtain a low standby current and high reliability. The IC contains six-transistor full CMOS mem-

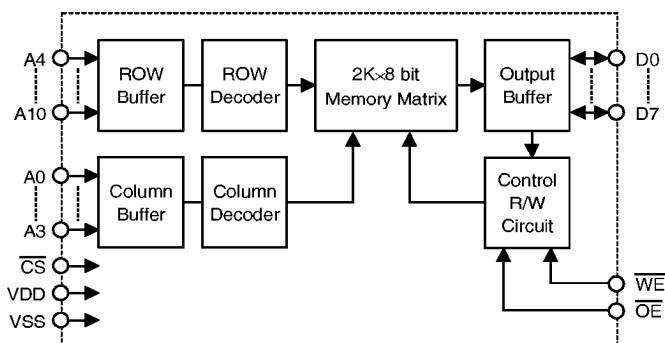
ory cells and TTL compatible inputs and outputs, which are easily interface with common system bus structures. The Data bus of the HT6116-70 is designed as a tri-state type. The IC is in the standby mode if the $\overline{\text{CS}}$ pin is set to "high".

Pin Assignment



HT6116-70
- 24 DIP/SDIP/SOP

Block Diagram



Pin Description

Pin No.	Pin Name	I/O	Description
8~1, 23, 22, 19	A0~A7 A8, A9, A10	I	Address inputs
9~11 13~17	D0~D2 D3~D7	I/O	Data inputs and outputs
12	VSS	I	Negative power supply, usually connected to the ground
18	$\overline{\text{CS}}$	I	Chip select signal pin When this signal is high, the chip is in the standby mode. The chip is in the active mode, if $\overline{\text{CS}}$ is low.
20	$\overline{\text{OE}}$	I	Output enable signal pin
21	$\overline{\text{WE}}$	I	Write enable signal pin
24	VDD	I	Positive power supply

Absolute Maximum Ratings*

Supply Voltage -0.3V to +7.0V Storage Temperature -50°C to +125°C
Input Voltage VSS-0.3V to VDD+0.3V Operating Temperature -40°C to +85°C

*Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

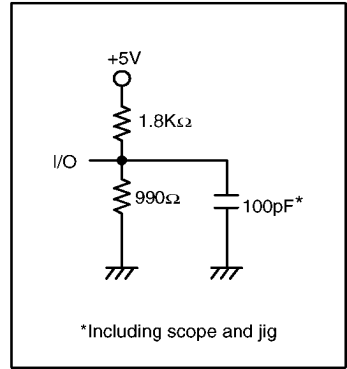
(Ta=25°C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD	Conditions				
VDD	Operating Voltage	—	—	4.5	5.0	5.5	V
ILI	Input Leakage Current	5V	VIN=0 to VDD	—	0.1	10	μA
ILO	Output Leakage Current	5V	VO=0 to VDD	—	0.1	10	μA
IDD	Operating Current	5V	VIH=2.2V, VIL=0.8V In write mode, tWC=1μs.	—	45	90	mA
		5V	VIH=2.2V, VIL=0.8V In read mode, tRC=1μs.	—	80	90	mA
ISTB	Standby Current	5V	VIH=2.2V, VIL=0.8V (TTL Input)	—	0.8	1.5	mA
		5V	VIH=4.8V, VIL=0.2V (CMOS Input)	—	0.1	3	μA

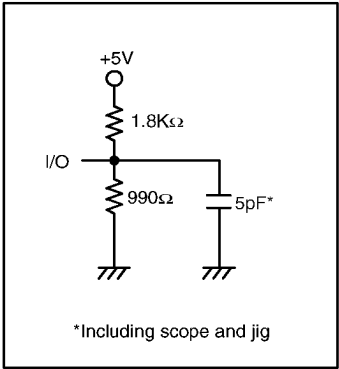
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
V _{IH}	Input Voltage	5V	—	2.2	2	5.3	V
V _{IL}		5V		−0.3	0.2	0.8	V
I _{OH}	Output Source Current	5V	V _{OH} =4.5V	−1.2	−6.2	—	mA
I _{OL}	Output Sink Current	5V	V _{OL} =0.5V	4.8	14.5	—	mA

A.C. Test Conditions

Item	Condition
Input pulse high level	V _{IH} =3V
Input pulse low level	V _{IL} =0V
Input and output reference level	1.5V
Output load	See Figures below



Output Load



Output Load for
t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{OW}

A.C. Characteristics

Read cycle

 $(V_{DD}=5V\pm 10\%, GND=0V, T_a=-40^{\circ}C \text{ to } +85^{\circ}C)$

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RC}	Read Cycle Time	70	36	—	ns
t_{AA}	Address Access Time	—	35	70	ns
t_{ACS}	Chip Select Access Time	—	35	70	ns
t_{OE}	Output Enable to Output Valid	—	12	40	ns
t_{OH}	Output Hold from Address Change	10	12	—	ns
t_{CLZ}	Chip Enable to Output in Low-Z	10	—	—	ns
t_{OLZ}	Output Enable to Output in Low-Z	10	—	—	ns
t_{OHZ}	Output Disable to Output in High-Z	0	—	30	ns
t_{CHZ}	Chip Disable to Output in High-Z	0	—	30	ns

Note: 1. A read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$

2. t_{CHZ} and t_{OHZ} are specified by the time when data out is floating

Write cycle

 $(V_{DD}=5V\pm 10\%, GND=0V, T_a=-40^{\circ}C \text{ to } +85^{\circ}C)$

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WC}	Write Cycle Time	70	36	—	ns
t_{DW}	Data Set up Time	20	18	—	ns
t_{DH}	Data Hold Time from Write Time	5	0	—	ns
t_{AW}	Address Valid to End of Write	50	15	—	ns
t_{AS}	Address Setup Time	20	14	—	ns
t_{WP}	Write Pulse Width	25	0	—	ns
t_{WR}	Write Recovery Time	5	—	—	ns
t_{CW}	Chip Selection to End of Write	35	—	—	ns
t_{OW}	Output Active from End of Write	5	—	—	ns
t_{OHZ}	Output Disable to Output in High-Z	0	—	40	ns
t_{WHZ}	Write to Output in High-Z	0	—	50	ns

Note: 1. A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$

2. $\overline{OE}$ may be both high and low in a write cycle

3. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last

4. t_{WP} is an overlap time of a low $\overline{CS}$ and a low $\overline{WE}$

5. t_{WR} , t_{DW} and t_{DH} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first

6. t_{WHZ} is specified by the time when DATA OUT is floating, not defined by output level

7. When I/O pins are data output mode, don't force inverse signals to those pins

Functional Description

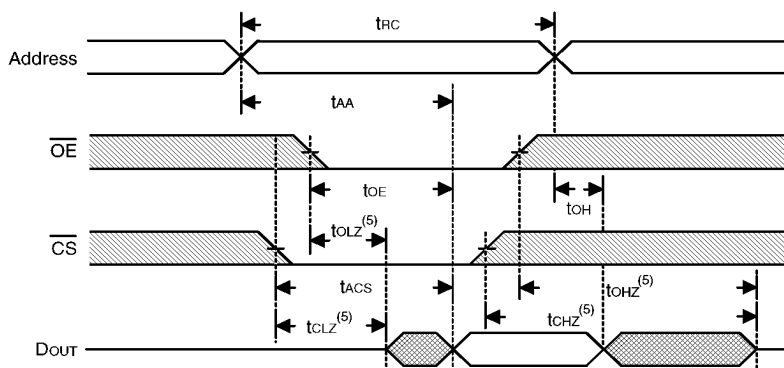
The HT6116-70 is a 2K×8 bit SRAM. When the $\overline{\text{CS}}$ pin of the chip is set to “low”, data can be written in or read from eight data pins; otherwise, the chip is in the standby mode. During a write cycle, the data pins are defined as the input state by setting the $\overline{\text{WE}}$ pin to low. Data should be ready before the rising edge of the $\overline{\text{WE}}$ pin according to the timing of the writing cycle. While in the read cycle, the $\overline{\text{WE}}$ pin is set to high and the $\overline{\text{OE}}$ pin is set to low to define the data pins as the output state. All data pins are defined as a three-state type, controlled by the $\overline{\text{OE}}$ pin. In both cycles (namely, write and read cycles), the locations are defined by the address pins A0~A10. The following table illustrates the relations of $\overline{\text{WE}}$, $\overline{\text{OE}}$, $\overline{\text{CS}}$ and their corresponding mode.

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	D0~D7
H	X	X	Standby	High-Z
L	L	H	Read	Dout
L	H	H	Read	High-Z
L	X	L	Write	Din

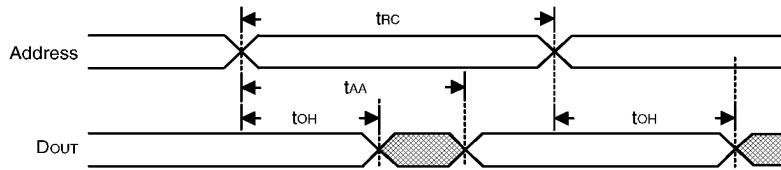
where X stands for “don’t care”.
H stands for high level
L stands for low level.

Timing Diagrams

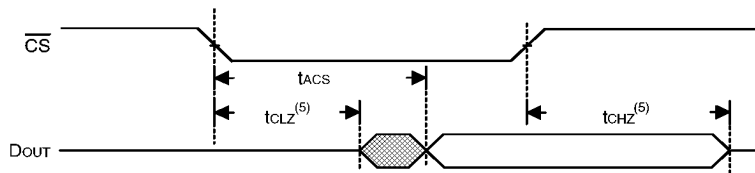
Read cycle ⁽¹⁾



Read cycle (1, 2, 4)



Read cycle (1, 3, 4)



- Notes:
- (1) $\overline{WE}$ is high during the Read cycle
 - (2) Device is continuously enabled, $\overline{CS}=V_{IL}$
 - (3) Address is valid prior to or coincident with the $\overline{CS}$ transition low.
 - (4) $\overline{OE}=V_{IL}$
 - (5) Transition is measured $\pm 500\text{mV}$ from the steady state.

The timing diagram illustrates the relationship between several signals during memory access operations. The signals shown are Address, OE (Output Enable), CS (Chip Select), WE (Write Enable), DOUT (Data Output), and DN (Data Input/Output). The diagram is divided into two main sections by vertical dashed lines, representing read and write cycles. Key timing parameters are indicated by arrows and labeled with text or numbers in parentheses:

- twc**: Address setup time before OE assertion.
- twr⁽³⁾**: Address hold time after OE deassertion.
- tcw**: CS setup time before WE assertion.
- taw**: CS hold time after WE deassertion.
- tas**: WE setup time before DOUT assertion.
- tohZ**: DOUT setup time before DN assertion.
- twp⁽²⁾**: WE hold time after DOUT deassertion.
- tw**: DN setup time before DN assertion.
- tbn**: DN hold time after DN deassertion.

Shaded regions indicate periods where signals are active or asserted. The diagram shows that CS and WE are active-low signals, while OE and DOUT are active-high signals. DN is a bidirectional signal that is active-low during write operations and active-high during read operations.

The timing diagram illustrates the sequence of signals for the 28C46. The Address bus shows two data transfers, each preceded by a t_{wc} delay. The CS signal is active-low and has a setup time t_{AS} before the first transfer and a hold time t_{AH} after the second. The WE signal is active-low and has a setup time t_{AW} before the first transfer and a hold time t_{WH} after the second. The DOUT bus shows the data output, with a setup time t_{wHZ} before the first transfer and a hold time t_{wH} after the second. The DN signal is active-low and has a setup time t_{dw} before the first transfer and a hold time t_{dH} after the second. Various timing parameters are labeled with numbers in parentheses, indicating their relationship to specific signal transitions.

- Notes:
- (1) $\overline{WE}$ must be high during all address transitions.
 - (2) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
 - (3) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
 - (4) During this period, I/O pins are in the output state, so the input signals of the opposite phase to the outputs must not be applied.
 - (5) If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.

- (6) $\overline{OE}$ is continuously low ($\overline{OE}=V_{IL}$).
- (7) D_{OUT} is at the same phase of the write data of this write cycle.
- (8) D_{OUT} is the read data of the next address.
- (9) If $\overline{CS}$ is low during this period, I/O pins are in the output state; then the data input signals of the opposite phase to the outputs must not be applied to them.
- (10) Transition is measured $\pm 500\text{mV}$ from the steady state.

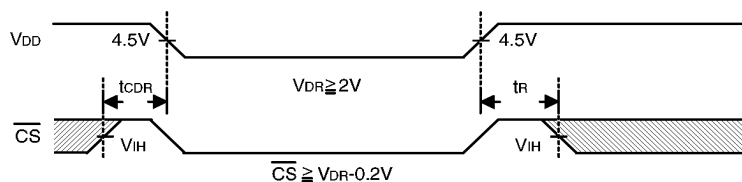
Data Retention Characteristics

($T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$)

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	$\overline{CS} \geq V_{DD}-0.2\text{V}$	2	5.5	V
I_{CCDR}	Data Retention Current	$V_{DD}=3\text{V}$, $\overline{CS} \geq V_{DD}-0.2\text{V}$ $V_{IN} \geq V_{DD}-0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$	—	50	μA
t_{CDR}	Chip Disable Data Retention Time	See Retention Timing	0	—	ns
t_R	Operation Recovery Time	See Retention Timing	t_{RC}^*	—	ns

* t_{RC} =Read Cycle Time

Low V_{DD} Data Retention Timing



Characteristic Curves

