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pLSI™ 1016
programmable Large Scale Integration

T-46-19-09

Features

- **PROGRAMMABLE HIGH DENSITY LOGIC**

  — Member of Lattice's pLSI Family
  — High Speed Global Interconnects
  — 32 I/O Pins, Four Dedicated Inputs
  — 96 Registers
  — Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  — Small Logic Block Size for Random Logic
  — Security Cell Prevents Unauthorized Copying

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**

  — f_{max} = 80 MHz Maximum Operating Frequency
  — t_{pd} = 15 ns Propagation Delay
  — TTL Compatible Inputs and Outputs
  — Electrically Erasable and Re-Programmable
  — 100% Tested

- **COMBINES EASE OF USE AND THE FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEX-IBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**

  — Complete Programmable Device can Combine Glue Logic and Structured Designs
  — 100% Routable at 80% Utilization
  — Three Dedicated Clock Input Pins
  — Synchronous and Asynchronous Clocks
  — Flexible Pin Placement
  — Optimized Global Routing Pool Allows Global Interconnectivity

- **pLSI/IspLSI™ DEVELOPMENT SYSTEM (pDS™)**

  — Boolean Logic Compiler
  — Automatic Place and Route
  — Manual Partitioning
  — PC Platform
  — Easy to Use Windows Interface

- **ADVANCED pLSI/ispLSI DEVELOPMENT SYSTEM**

  — Industry Standard, Third Party Design Environments
  — Schematic Capture
  — Fully Automatic Partitioning
  — Automatic Place and Route
  — Comprehensive Logic and Timing Simulation
  — PC and Workstation Platforms

Functional Block Diagram
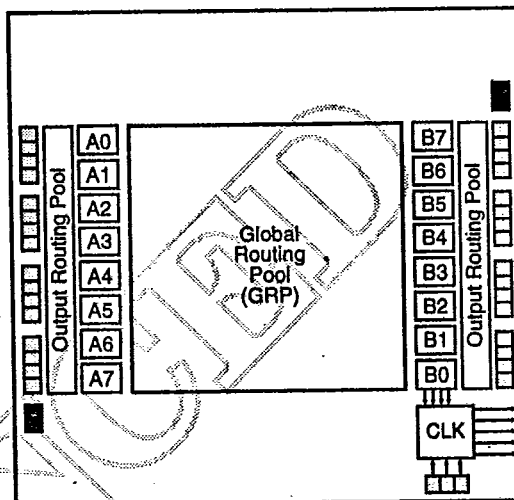
Description

The Lattice pLSI 1016 is a High Density Programmable Logic Device which contains 96 Registers, 32 Universal I/O pins, four Dedicated Input Pins, three Dedicated Clock Input Pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements.

The basic unit of logic on the pLSI 1016 device is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 ..B7, (see figure 1). There are a total of 16 GLBs in the pLSI 1016 device. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any other GLB on the device.

Functional Block Diagram

Figure 1. pLSI 1016

T-46-19-09

*Note:
Y1 and $\overline{RESET}$ are multiplexed on the same pin

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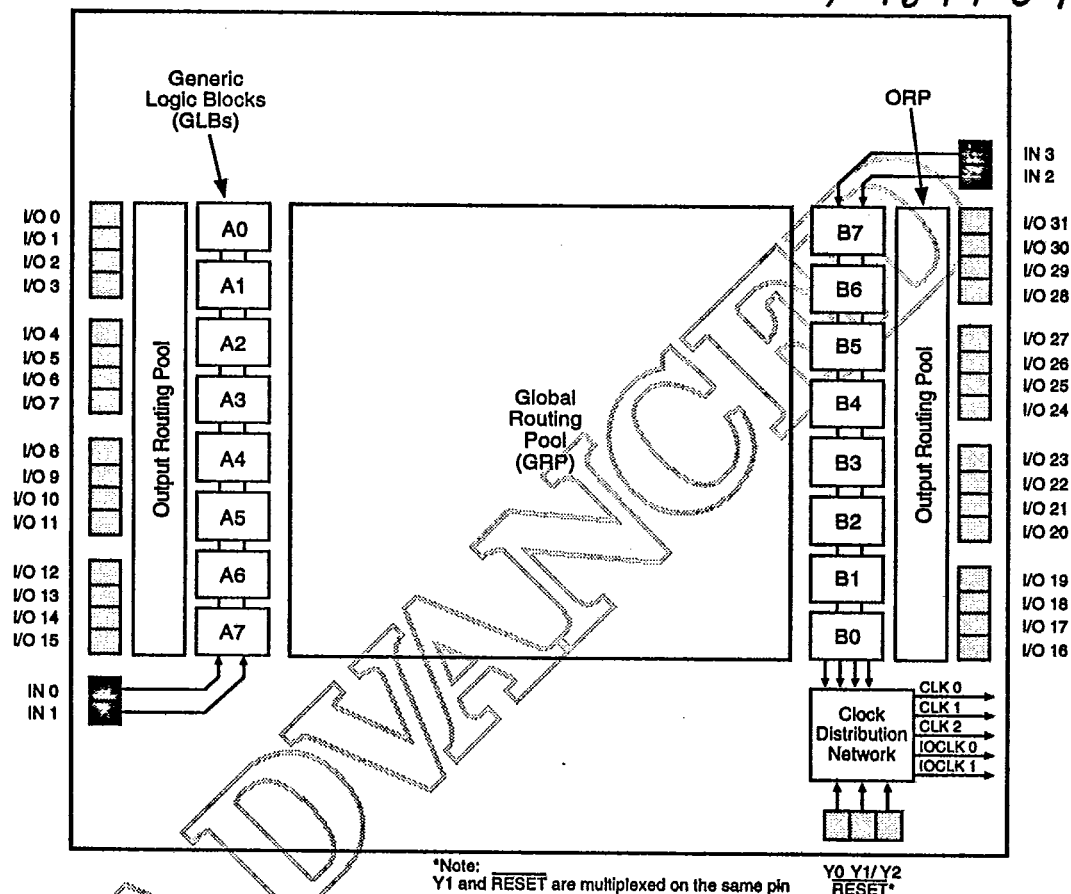
Description (continued)

The device also has 32 I/O Cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, registered input, latched input, output or bi-directional I/O pin with 3-state. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA.

The 32 I/O Cells are grouped into two sets of 16 each as shown in figure 1. Each of these I/O groups is associated with a logic Megablock through the use of the Output Routing Pool (ORP) and shares a common Output Enable (OE) signal.

Eight GLBs, 16 I/O Cells and one ORP are connected together to make a logic Megablock. The Megablock is defined by the resources that it shares. The outputs of the eight GLBs are connected to a set of 16 universal I/O cells by the ORP. The pLSI 1016 Device contains two of these Megablocks.

The GRP has as its inputs the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew and logic glitching.
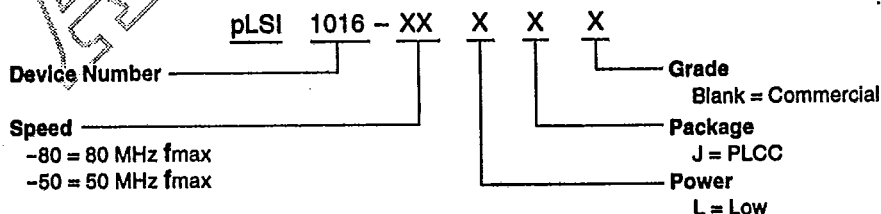
Clocks in the pLSI 1016 device are selected using the Clock Distribution Network. Three dedicated clock pins (Y0 to Y2) are brought into the distribution network, and five outputs (CLK 0 to CLK 2 and IOCLK 0, IOCLK 1) are provided to route clocks to the GLBs and I/O cells. The Clock Distribution Network can also be driven from a special GLB (B0 on the pLSI 1016 device). The logic of this GLB allows the user to create an internal clock from a combination of internal signals within the device.

The pLSI 1016 device is part of Lattice's programmable Large Scale Integration (pLSI) family. This family contains a range of devices from the pLSI 1016, with 96 registers, to the pLSI 1048 with 288 registers. The pLSI Family Product Selector Guide below lists key attributes of the devices along with the number of resources available.

pLSI Family Product Selector Guide

DEVICE	pLSI 1016	pLSI 1024	pLSI 1032	pLSI 1048
GLBs	16	24	32	48
Registers	96	144	192	288
I/O Pins	32	48	64	96
Dedicated Inputs	4	6	8	10
Pin Count	44	68	84	120

Ordering Information

pLSI   1016 – XX   X   X   X

Device Number — pLSI 1016

Speed
 –80 = 80 MHz fmax
 –50 = 50 MHz fmax

Grade
 Blank = Commercial

Package
 J = PLCC

Power
 L = Low

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Pin Description

Name	PLCC Pin Numbers	Description
I/O 0 - I/O 3 I/O 4 - I/O 7 I/O 8 - I/O 11 I/O 12 - I/O 15 I/O 16 - I/O 19 I/O 20 - I/O 23 I/O 24 - I/O 27 I/O 28 - I/O 31	15, 16, 17, 18, 19, 20, 21, 22, 25, 26, 27, 28, 29, 30, 31, 32, 37, 38, 39, 40, 41, 42, 43, 44, 3, 4, 5, 6, 7, 8, 9, 10	Input/Output Pins - These are the general purpose I/O pins used by the logic array.
IN 0 - IN 3	14, 24, 36, 2	Dedicated input pins to the device.
Y0	11	Dedicated Clock input. This clock input is connected to one of the clock inputs of all of the GLBs on the device.
Y1/$\overline{RESET}$	35	This pin performs two functions: – Dedicated clock input. This clock input is brought into the Clock Distribution Network, and can optionally be routed to any GLB and/or I/O Cell on the device. – Active Low (0) Reset pin which resets all of the GLB and I/O registers in the device.
Y2	33	Dedicated Clock input. This clock input is brought into the clock distribution network, and can optionally be routed to any I/O Cell in the device. This is a factory test pin and it should be left floating or tied to V_{cc}.
NC	13	This is a factory test pin and it should be left floating or tied to V_{cc}.
GND Vcc	1, 23 12, 34	Ground (GND) V_{cc}

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Absolute Maximum Ratings[1]

Supply Voltage V_{CC}. . . . .-0.5 to +7.0V

Input Voltage Applied. . . . .-2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied . . . . . .-2.5 to V_{CC} +1.0V

Storage Temperature . . . .-65 to 125°C

Ambient Temp. with Power Applied . . . .-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER	MIN.	MAX.	UNITS
T_A	Ambient Temperature	0	70	°C
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IL}	Input Low Voltage	0	0.8	V
V_{IH}	Input High Voltage	2.0	V_{CC}	V

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM[1]	UNITS	TEST CONDITIONS
C_1	Input Capacitance	8	pf	V_{CC}=5.0V, V_{IN}=2.0V
C_2	I/O, Y Capacitance	10	pf	V_{CC}=5.0V, VI/O, Y=2.0V

1. Guaranteed but not 100% tested.

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	YEARS
Erase/Reprogram Cycles	–	100	CYCLES

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Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

Figure 2. Test Load
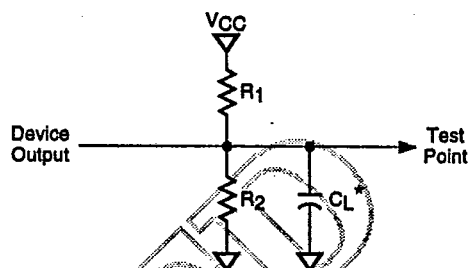
*C_L Indicates Test Fixture and Probe Total Capacitance.

Output Load Conditions (see figure 2)

Test Condition		R1	R2	CL
1		470Ω	390Ω	35pF
2	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
3	Active High to Z at V_{OH} - 0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} + 0.5V	470Ω	390Ω	5pF

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} =8 mA.	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} =-4 mA.	2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)	–	–	-10	μA
I_{IH}	Input or I/O High Leakage Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	–	–	10	μA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V	-60	–	-200	mA
I_{CC}[2]	Operating Power Supply Current	V_{IL} = 0.5V, V_{IH} = 3.0V F_{TOGGLE} = 20 MHz	–	–	–	mA

1. One output at a time for a maximum duration of one second. (Vout = 0.5V)
2. Measured at a frequency of 20 MHz using four 16-bit counters.

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External Switching Characteristics [1,2,3]   pLSI 1016-80

Over Recommended Operating Conditions

PARAMETER	TEST[6] COND.	#	DESCRIPTION	MIN.	TYP.	MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	12	15	ns
t_{pd2}	1	2	Data Propagation Delay	–	15	20	ns
t_{co1}[5]	1	3	External Clock to Output Delay, ORP bypass	–	8	11	ns
t_{co2}[5]	1	4	External Clock to Output Delay	–	9	14	ns
t_{co3}	1	5	Internal Synch. Clock to Output Delay	–	15	20	ns
t_{co4}	1	6	Asynchronous Clock to Output Delay	–	13	20	ns
t_{r1}	1	7	External Pin Reset to Output Delay	–	13	20	ns
t_{r2}	1	8	Asynchronous PT Reset to Output Delay	–	15	22	ns
t_{en}	2	9	Input to Output Enable	–	13	20	ns
t_{dis}	3	10	Input to Output Disable	–	13	20	ns

External AC Recommended Operating Conditions [1,2,3]   pLSI 1016-80

Over Recommended Operating Conditions

PARAMETER	TEST[6] COND.	#	DESCRIPTION	MIN.	TYP.	MAX.	UNITS
f_{max}[4]	1	11	Clock Frequency with Internal Feedback	–	100	80	MHz
f_{max} (External)	1	12	Clock Frequency with External Feedback	–	70	50	MHz
t_{su1}	–	13	Setup Time before External Synch. Clock, 4PT bypass	9	6	–	ns
t_{su2}	–	14	Setup Time before External Synch Clock	12	8	–	ns
t_{su3}	–	15	Setup Time before Internal Synch. Clock	9	3	–	ns
t_{su4}	–	16	Setup Time before Asynchronous Clock	9	4	–	ns
t_{h1}	–	17	Hold time after External Synchronous Clock, 4PT bypass	2	-1	–	ns
t_{h2}	–	18	Hold time after External Synchronous Clock	2	-1	–	ns
t_{h3}	–	19	Hold time after Internal Synchronous Clock	8	2	–	ns
t_{h4}	–	20	Hold time after Asynchronous Clock	8	1	–	ns
t_{rw1}	–	21	External Reset Pulse Duration	10	8	–	ns
t_{rw2}	–	22	Asynchronous Reset Pulse Duration	10	8	–	ns
t_{wh1}, t_{wl1}	–	23,24	External Synchronous Clock Pulse Duration, High, Low	6	5	–	ns
t_{wh2}, t_{wl2}	–	25,26	Asynchronous Clock Pulse Duration, High, Low	6	5	–	ns

1. External Parameters are tested and guaranteed.
2. See Timing Technical Note for further details.
3. Unless noted, all parameters use ORP, GRP fanout of four, PTSA, and are measured with 16 outputs switching.
4. Standard 16-bit counter implementation using GRP feedback.
5. Clock to output specifications include a maximum skew of 2 ns.
6. Refer to Switching Test Conditions section.

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Using I/O Cell

PARAMETER	TEST[4] COND.	#	DESCRIPTION	MIN.	TYP.	MAX.	UNITS
t_su5	–	27	Setup Time before External Synchronous Clock	5	0	–	ns
t_su6	–	28	Setup Time before Internal Synchronous Clock	0	-3	–	ns
t_h5	–	29	Hold Time after External Synchronous Clock	8	4	–	ns
t_h6	–	30	Hold Time after Internal Synchronous Clock	15	11	–	ns
t_wh3, t_wl3	–	31,32	Clock Pulse Duration, High, Low	6	5	–	ns

1. External Parameters are tested and guaranteed.
2. See Timing Technical Note for further details.
3. Unless noted, all parameters use ORP, GRP fanout of four, PTSA, and are measured with 16 outputs switching.
4. Refer to Switching Test Conditions section.

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External Switching Characteristics [1,2,3]   pLSI-1016-50

Over Recommended Operating Conditions

PARAMETER	TEST[6] COND.	#	DESCRIPTION	MIN.	TYP.	MAX.	UNITS
t_{pd1}	1	1	Data Propagation Delay, 4PT bypass, ORP bypass	–	16	20	ns
t_{pd2}	1	2	Data Propagation Delay, ORP	–	19	25	ns
t_{co1}[5]	1	3	External Clock to Output Delay, ORP bypass	–	12	16	ns
t_{co2}[5]	1	4	External Clock to Output Delay	–	15	20	ns
t_{co3}	1	5	Internal Synch. Clock to Output Delay	–	21	28	ns
t_{co4}	1	6	Asynchronous Clock to Output Delay	–	21	28	ns
t_{r1}	–	7	External Pin Reset to Output Delay	–	21	28	ns
t_{r2}	–	8	Asynchronous PT Reset to Output Delay	–	24	30	ns
t_{en}	2	9	Input to Output Enable	–	21	28	ns
t_{dis}	3	10	Input to Output Disable	–	21	28	ns

External AC Recommended Operating Conditions [1,2,3]   pLSI-1016-50

Over Recommended Operating Conditions

PARAMETER	TEST[6] COND.	#	DESCRIPTION	MIN.	TYP.	MAX.	UNITS
f_{max}[4]	1	11	Clock Frequency with Internal Feedback	–	70	50	MHz
f_{max} (External)	1	12	Clock Frequency with External Feedback	–	45	33	MHz
t_{su1}	–	13	Setup Time before External Synch. Clock, 4PT bypass	14	10	–	ns
t_{su2}	–	14	Setup Time before External Synch Clock	17	13	–	ns
t_{su3}	–	15	Setup Time before Internal Synch. Clock	13	9	–	ns
t_{su4}	–	16	Setup Time before Asynchronous Clock	13	9	–	ns
t_{h1}	–	17	Hold time after External Synchronous Clock, 4PT bypass	7	3	–	ns
t_{h2}	–	18	Hold time after External Synchronous Clock	7	3	–	ns
t_{h3}	–	19	Hold time after Internal Synchronous Clock	11	5	–	ns
t_{h4}	–	20	Hold time after Asynchronous Clock	11	5	–	ns
t_{rw1}	–	21	External Reset Pulse Duration	15	13	–	ns
t_{rw2}	–	22	Asynchronous Reset Pulse Duration	15	13	–	ns
t_{wh1}, t_{wl1}	–	23,24	External Synchronous Clock Pulse Duration, High, Low	10	8	–	ns
t_{wh2}, t_{wl2}	–	25,26	Asynchronous Clock Pulse Duration, High, Low	10	8	–	ns

1. External Parameters are tested and guaranteed.
2. See Timing Technical Note for further details.
3. Unless noted, all parameters use ORP, GRP fanout of four, PTSA, and are measured with 16 outputs switching.
4. Standard 16-bit counter implementation using GRP feedback.
5. Clock to output specifications include a maximum skew of 2 ns.
6. Refer to Switching Test Conditions section.

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Switching Characteristics[1,2,3]   **pLSI 1016-50**

Using I/O Cell

PARAMETER	TEST[4] COND.	#	DESCRIPTION	MIN.	TYP.	MAX.	UNITS
$t_{su}5$	–	27	Setup Time before External Synchronous Clock	10	5	–	ns
$t_{su}6$	–	28	Setup Time before Internal Synchronous Clock	0	-5	–	ns
t_h5	–	29	Hold Time after External Synchronous Clock	12	6	–	ns
t_h6	–	30	Hold Time after Internal Synchronous Clock	20	15	–	ns
$t_{wh}3$, $t_{wl}3$	–	31,32	Clock Pulse Duration, High, Low	10	8	–	ns

1. External Parameters are tested and guaranteed.
2. See Timing Technical Note for further details.
3. Unless noted, all parameters use ORP, GRP fanout
   of four, PTSA, and are measured with 16 outputs switching.
4. Refer to Switching Test Conditions section.

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The Generic Logic Block

The Generic Logic Block (GLB) is the standard logic block of the Lattice High Density pLSI Device. This GLB has 18 inputs, four outputs and the logic necessary to implement most standard logic functions. The internal logic of the GLB is divided into four separate sections (see figure 3). The AND Array, the Product Term Sharing Array (PTSA), the Reconfigurable Registers, and the Control Functions. The AND array consists of 20 product terms which can produce the logical sum of any of the 18 GLB inputs. Sixteen of the inputs come from the Global Routing Pool, and are either feedback signals from any of the 16 GLBs or inputs from the external I/O Cells. The two remaining inputs come directly from two dedicated input pins. These signals are available to the product terms in both the logical true and the complemented forms which makes boolean logic reduction easier.

The PTSA takes the 20 product terms and allocates them to the four GLB outputs. There are four OR gates, with four, four, five and seven product terms (see figure 3). The

output of any of these gates can be routed to any of the four GLB outputs, and if more product terms are needed, the PTSA can combine them as necessary. If the users' main concern is speed, the PTSA can use a bypass circuit with four product terms to increase the performance of the cell (see figure 4). This can be done to any or all of the four outputs from the GLB.

The Reconfigurable Registers consist of four D-type flip-flops with an Exclusive OR Gate on the input. The Exclusive OR gate in the GLB can be used either as a logic element or to reconfigure the D-type flip-flop to emulate a J-K, or T-type flip-flop (see figure 5). This greatly simplifies the design of counters, comparators and ALU type functions. The registers can be bypassed if the user needs a combinatorial output. Each register output is brought back into the Global Routing Pool and is also brought to the I/O cells via the Output Routing Pool. Reconfigurable registers are not available when the four product term bypass is used.

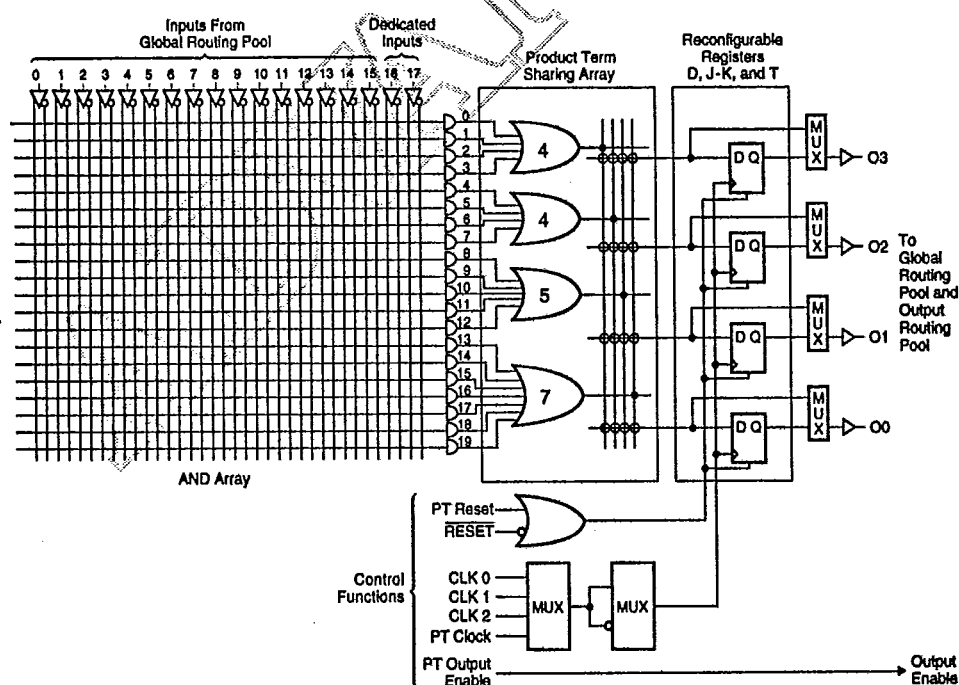### Figure 3. GLB: Product Term Sharing Array

Architectural Description
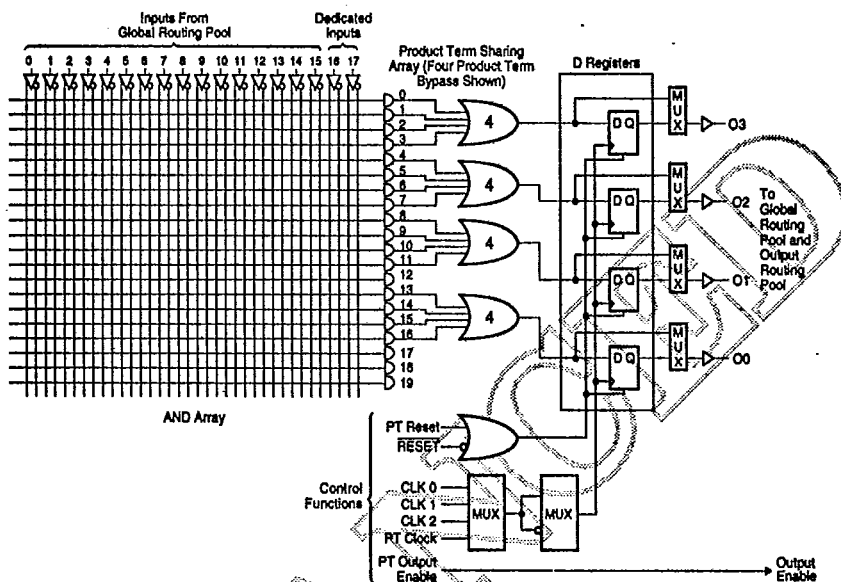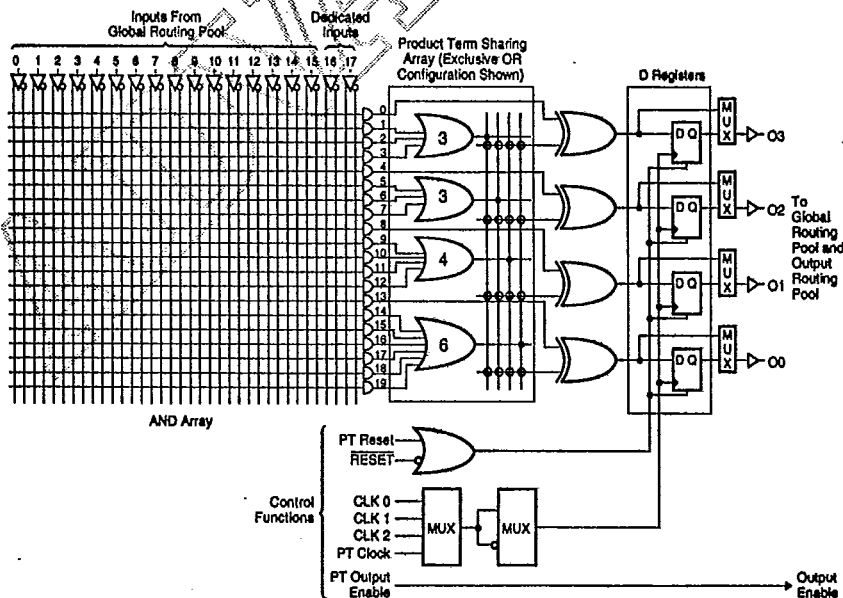
Figure 4. GLB: Four Product Term Bypass

Figure 5. GLB: Exclusive OR Gate

Architectural Description

The Generic Logic Block (continued)

The PTSA is flexible enough to allow these features to be used in virtually any combination that the user desires. In the GLB shown in figure 6, Output Three (O3) is configured using the XOR Gate and Output Two (O2) is configured using the four Product Term Bypass. Output One (O1) uses one of the inputs from the five Product Term OR gate while Output Zero (O0) combines the remaining four product terms with all of the product terms from the seven Product Term OR gate for a total of eleven (7+4).

Various signals which control the operation of the GLB are developed in the Control Function section. The clock for the registers can come from any of three sources developed in

the Clock Distribution Network (See Clock Distribution Network Section) or from a product term within the GLB. The Reset Signal for the GLB can come from the Global Reset pin or from a product term within the block. The Output Enable for the I/O cells associated with the GLB comes from a product term within the block. Use of a product term for a control function makes that product term unavailable for use as a logic term. Refer to the following table to determine which logic functions are affected.

There are many additional features in a GLB which allow implementation of logic intensive functions. These features are accessible using the hard Macros from the software and require no intervention on the part of the user.

Figure 6. GLB: Various Logical Combinations

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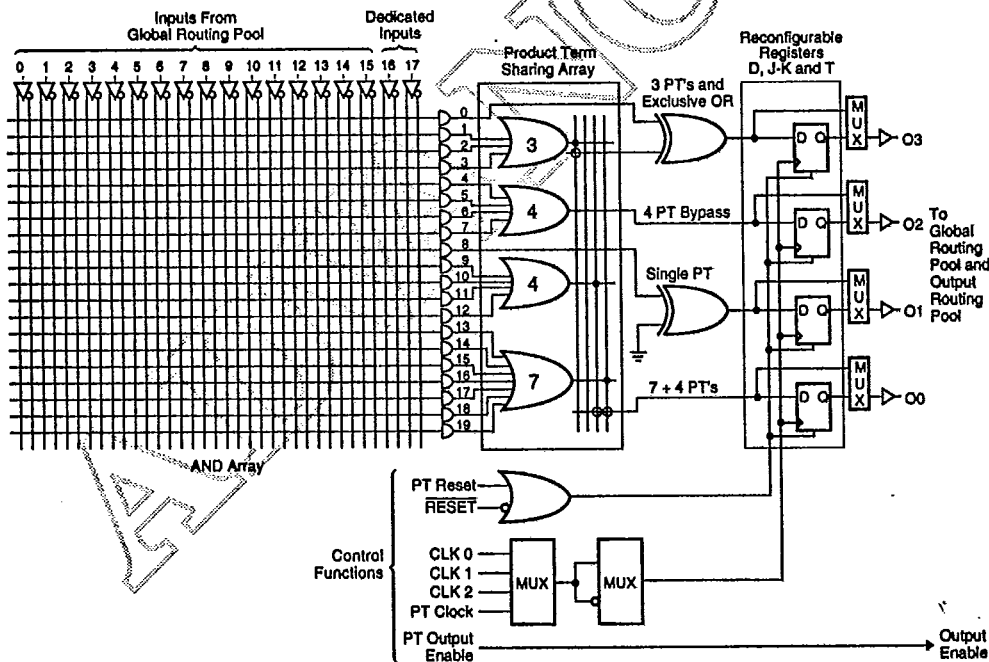
Architectural Description

Product Term Sharing Matrix

Product Term #	Standard Configuration Output Number				Four Product Term Bypass Output Number				Single Product Term Output Number				XOR Function Output Number								Alternate Function
	3	2	1	0	3	2	1	0	3	2	1	0	3	3	2	2	1	1	0	0	
0	■	■	■	■	■				■				■								
1	■	■	■	■	■									■							
2	■	■	■	■	■									■							
3	■	■	■	■	■									■							
4	■	■	■	■		■				■					■						
5	■	■	■	■		■										■					
6	■	■	■	■		■										■					
7	■	■	■	■		■										■					
8	■	■	■	■			■				■						■				
9	■	■	■	■			■											■			
10	■	■	■	■			■											■			
11	■	■	■	■			■											■			
12	■	■	■	■														■			■ CLK/Reset
13	■	■	■	■				■				■							■		
14	■	■	■	■				■												■	
15	■	■	■	■				■												■	
16	■	■	■	■				■												■	
17	■	■	■	■																■	
18	■	■	■	■																■	
19	■	■	■	■																■	■ OE/Reset

This matrix shows how each of the product terms are used in the various modes. As an example, Product Term 12 can be used as an input to the five input OR gate in the standard configuration. This OR gate under standard configuration can be routed to any of the four GLB outputs. Product Term 12 is not used in the four product term bypass mode. When GLB output one is used in the Exclusive OR (XOR) mode Product Term 12 becomes one of the inputs to the four input OR Gate. If Product Term 12 is not used in the logic, then it is available for use as either the Asynchronous Clock signal or the GLB Reset signal.

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Specifications *pLSI 1016*

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Architectural Description

The Megablock

The pLSI family is structured into multiple "Megablocks". A Megablock consists of 8 GLBs, an Output Routing Pool (ORP) and 16 I/O Cells. Each of these will be explained in detail in the following sections. These elements are coupled together as shown in figure 7. This logic structure is referred to as the Megablock. The various members of the pLSI family are created by combining from two to six Megablocks on a single device.

The Megablock shares two sets of resources. The eight GLBs within the Megablock share two dedicated input pins. These dedicated input pins are not available to GLBs in any other Megablock. These pins are dedicated (non-regis-

tered) inputs only and are automatically assigned by software. One Output Enable signal is generated within the Megablock and is common to all sixteen of the I/O Cells in the Megablock. The Output Enable signal can be generated using a product term in any of the eight GLBs within the Megablock (see the following section on the Output Enable Multiplexers).

Because of the shared logic within the Megablock, signals which share a common function (counters, busses, etc.) should be grouped within a Megablock. This will allow the user to obtain the best utilization of the logic within the device and eliminate routing bottlenecks.

Megablocks in Each Device

DEVICE	MEGABLOCKS	GLBs	I/O CELLS
pLSI 1016	2	16	32
pLSI 1024	3	24	48
pLSI 1032	4	32	64
pLSI 1048	6	48	96

Figure 7. The Megablock
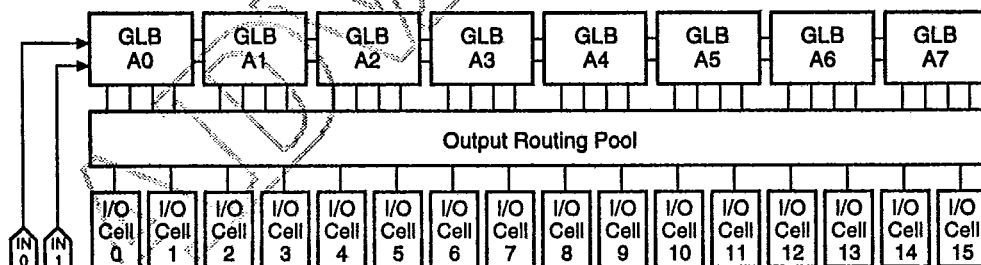
Note: The inputs from the I/O Cell are not shown in this figure, they go directly to the GRP.

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Architectural Description

The Output Enable Control

One Output Enable (OE) signal can be generated within each GLB using the OE Product Term 19. One of the eight OE signals from each GLB within a Megablock, is then routed to all of the I/O Cells within the Megablock (see figure 8). This OE signal can simultaneously control all of the 16 I/O cells which are used in 3-state mode. Individual I/O cells also have independent control for permanently enabling or disabling the output buffer (Refer to the I/O Cell Section). Only one OE signal is allowed per Megablock for 3-state operation. The advantage to this approach is that the OE signal can be generated in any GLB within the Megablock which happens to have an unused OE product term. This frees up the other OE product terms for use as logic.

Figure 8. Output Enable Controls

Architectural Description
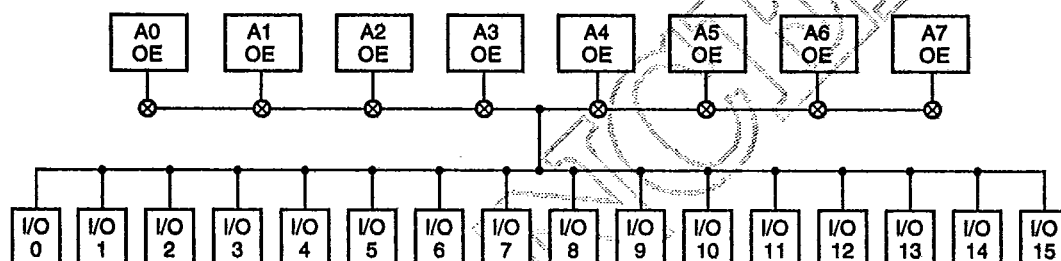
The Output Routing Pool

The Output Routing Pool (ORP) routes signals from the Generic Logic Block outputs to I/O Cells configured as outputs or bi-directional pins (see figure 9). The purpose of the ORP is to allow greater flexibility when assigning I/O pins. It also simplifies the job for the routing software which results in a higher degree of utilization.

By examining the programmable switch matrix in figure 9, it can be seen that a GLB output can be connected to one of four I/O Cells. Further flexibility is provided by using the PTSA, (Figures 3 through 7) which makes the GLB outputs

completely interchangeable. This allows the routing program to freely interchange the outputs to achieve the best routability. This is an automatic process and requires no intervention on the part of the user.

The ORP bypass connections (see figure 10) further increase the flexibility of the device. The ORP bypass connect specific GLB outputs to specific I/O Cells at a faster speed. The bypass path tends to restrict the routability of the device and should only be used for critical signals.

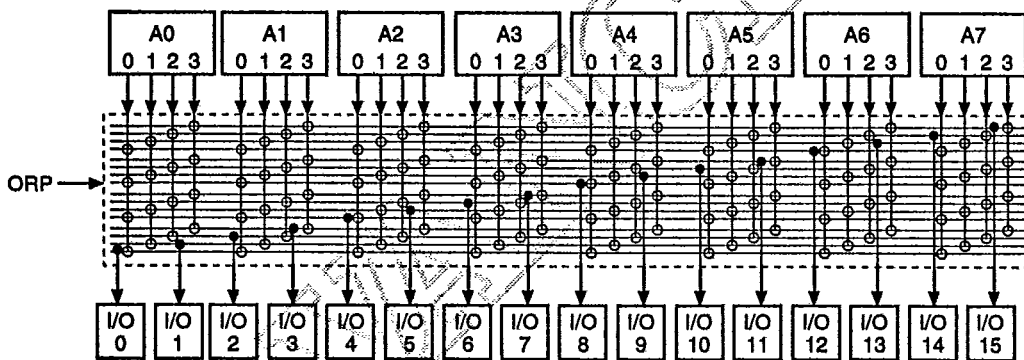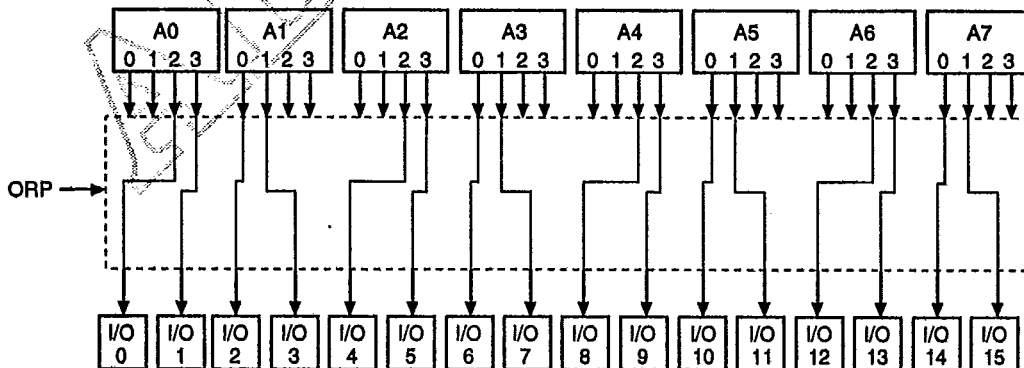### Figure 9. Output Routing Pool

Figure 10. Output Routing Pool showing Bypass

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Architectural Description

I/O Cell

The I/O Cell (see figure 11) is used to route input, output or bidirectional signals connected to the I/O pin. The two logic inputs come from the ORP (see figure 7). One comes from the ORP, and the other comes from the faster ORP bypass. A pair of multiplexers select which signal will be used, and its polarity.

The OE signal comes from the Output Enable. As with the data path, a multiplexer selects the signal polarity. The Output Enable can be set to a logic high (Enabled) when a straight output pin is desired, or logic low (Disabled) when a straight input pin is needed. The Global Reset (RESET) signal is driven by the active low chip reset pin. Each I/O Cell can individually select one of the two clock signals (IOCLK 0 or IOCLK 1). These clock signals are generated by the Clock Distribution Network.

Using the multiplexers, the I/O Cell can be configured as an input, an output, a 3-stated output or a bidirectional I/O. The D-type register can be configured as a level sensitive transparent latch or an edge triggered flip-flop to store the in-coming data. Figure 12 illustrates some of the various I/O cell configurations possible.

There is an Active Pullup resistor on the I/O pins which is automatically used when the pin is not connected. This prevents the pin from floating and inducing noise into the device or consuming additional power.
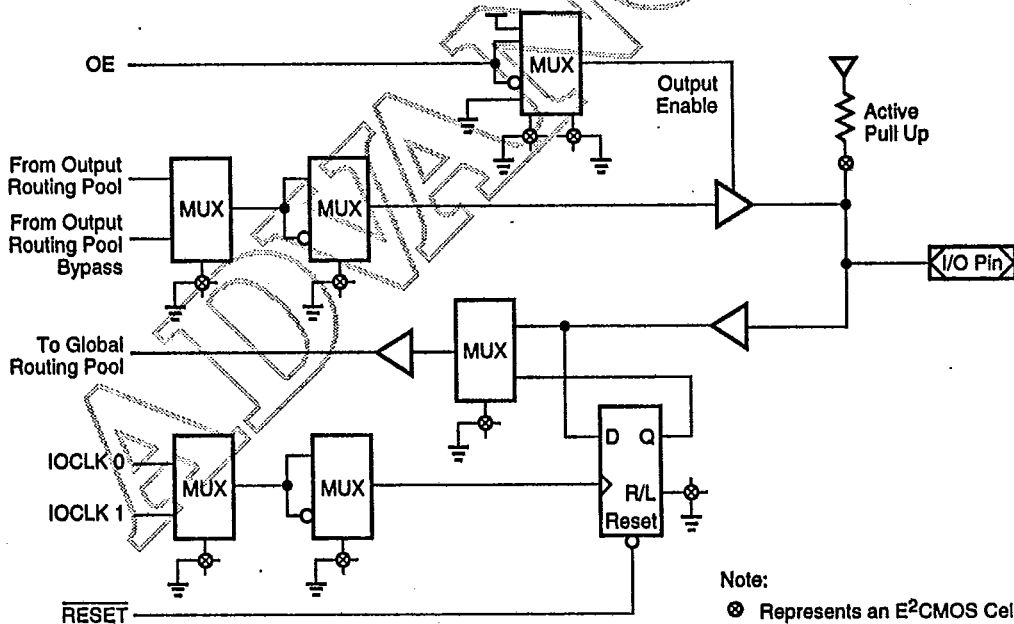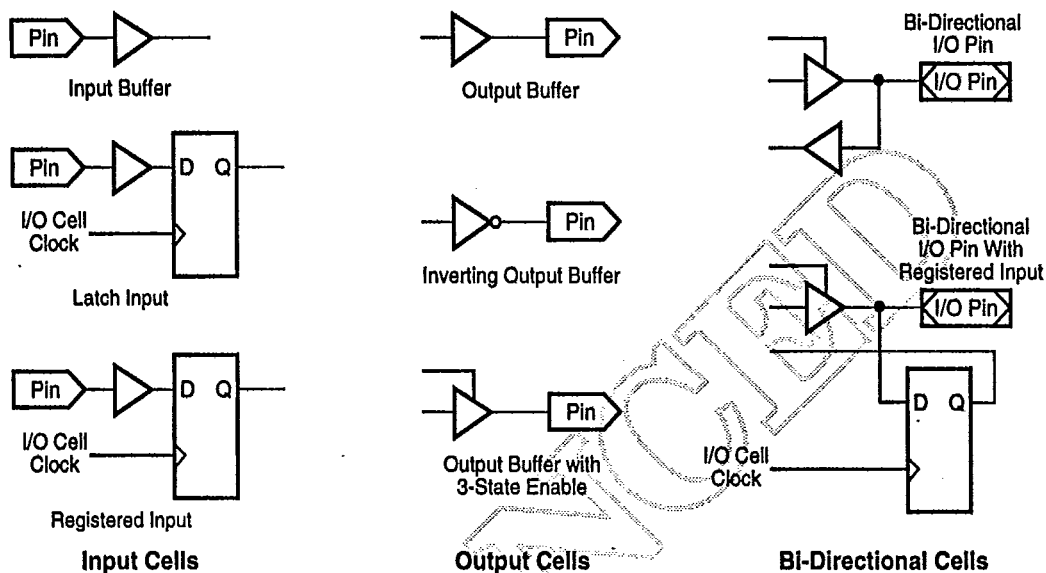
Figure 11. I/O Cell Architecture

Note:
⊗ Represents an E²CMOS Cell.

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Architectural Description

Figure 12. Example I/O Cell Configurations

Input Buffer

Latch Input

Registered Input

Input Cells

Output Buffer

Inverting Output Buffer

Output Buffer with 3-State Enable

Output Cells

Bi-Directional I/O Pin

Bi-Directional I/O Pin With Registered Input

Bi-Directional Cells

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Architectural Description

Clock Distribution Network

The Clock Distribution Network is shown in figure 13. It generates five global clock signals CLK 0, CLK 1, CLK 2 and IOCLK 0, IOCLK 1. The first three, CLK 0, CLK 1 and CLK 2 are used for clocking all the GLBs in the device. Similarly, IOCLK 0 and IOCLK 1 signals are used for clocking all of the I/O Cells in the device. There are three dedicated system clock pins (Y0, Y1, Y2) which can be directed to any GLB or any I/O Cell using the Clock Distribution Network. The other inputs to the Clock Distribution Network are the 4 outputs of a dedicated clock GLB ("B0" for pLSI 1016). These Clock GLB outputs can be used to create a user-defined internal clocking scheme.

Typically the clock GLB will be clocked using an external main clock pin Y0 connected to global clock signal CLK 0. The outputs of the clock GLB in turn will generate "divide by two" or "divide by four" phases of the CLK 0 which can be connected to CLK 1, CLK 2 or IOCLK 0, IOCLK 1 global clocks.
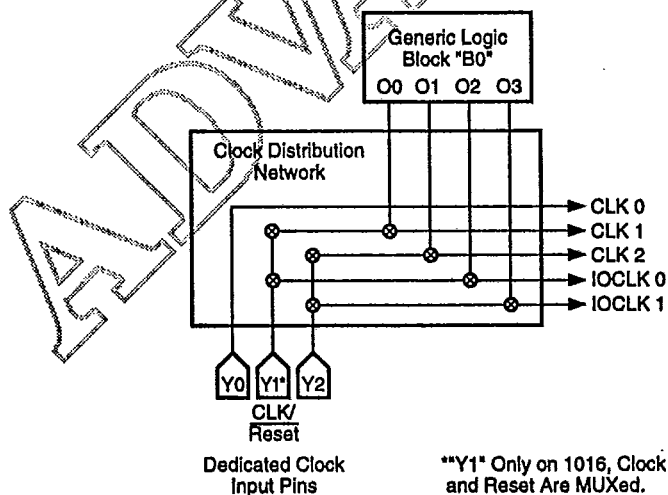
All GLBs also have the capability of generating their own asynchronous clocks using Product Term 12. CLK 0, CLK 1 and CLK 2 feed to their corresponding inputs on all the GLBs (see figure 3).

The two I/O clocks generated in the Clock Distribution Network IOCLK 0 and IOCLK 1, are brought to all 32 of the I/O cells and the user programs the I/O cell to use one of the two.

Global Routing Pool

The Global Routing Pool (GRP) is a Lattice proprietary interconnect structure which offers fast predictable speeds with complete connectivity. The GRP allows the outputs from the GLBs or the I/O cell inputs to be connected to the inputs of the GLBs. Any GLB output is available to the input of all other GLBs, and similarly an input from an I/O pin is available as an input to all of the GLBs. Because of the uniform architecture of the pLSI device, the delays through the Global Routing Pool are both consistent and predictable. However, they are slightly affected by fanout.

Figure 13. Clock Distribution Network

Generic Logic Block "B0"
O0 O1 O2 O3

Clock Distribution Network

CLK 0
CLK 1
CLK 2
IOCLK 0
IOCLK 1

Y0 Y1* Y2
CLK/
Reset

Dedicated Clock   **"Y1" Only on 1016, Clock
Input Pins   and Reset Are MUXed.

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Security Cell

A security cell is provided in the pLSI devices to prevent unauthorized copying of the array patterns. Once programmed, this cell prevents further read access to the functional bits in the device. This cell can only be erased by reprogramming the device, so the original configuration can never be examined once this cell is programmed.

Device Programming

pLSI devices are programmed using a Lattice-approved Device Programmer, available from a number of third party manufacturers. Complete programming of the device takes only a few seconds. Erasing of the device is automatic and is completely transparent to the user. In-system programming is available with ispLSI devices using Lattice programming algorithm.

Latch-up Protection

pLSI devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the internal circuitry to latchup. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.
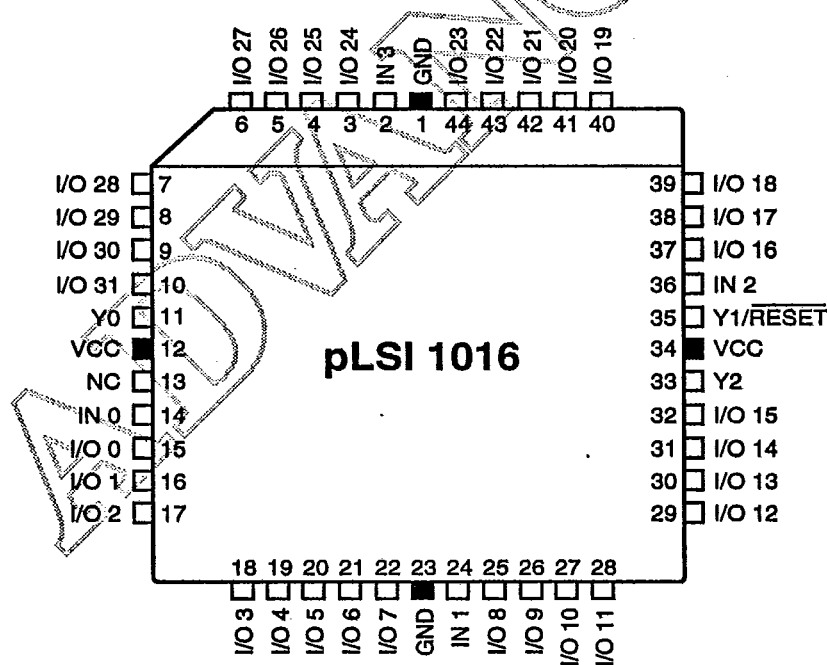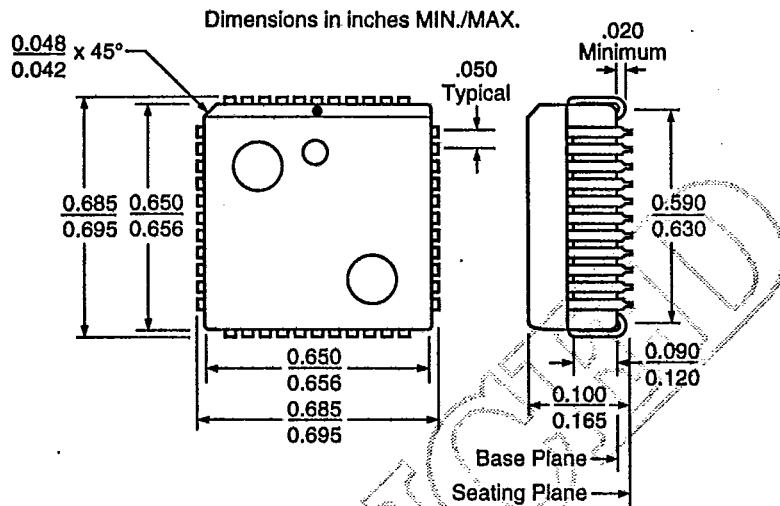
2

Pin Configuration

pLSI 1016 PLCC Pinout Diagram

2-51

44-Pin PLCC

Dimensions in inches MIN./MAX.

Package Diagrams

T-90-20

44-Pin PLCC

Dimensions in inches MIN./MAX.

0.048 / 0.042 x 45°

.020 Minimum

.050 Typical

0.685 / 0.695   0.650 / 0.656

0.590 / 0.630

0.650 / 0.656

0.685 / 0.695

0.090 / 0.120

0.100 / 0.165

Base Plane

Seating Plane

68-Pin PLCC

Dimensions in inches MIN./MAX.

0.048 / 0.042 x 45°

.020 Minimum

.050 Typical

0.985 / 0.995   0.950 / 0.958

0.890 / 0.930

0.950 / 0.958

0.985 / 0.995

0.090 / 0.120

0.100 / 0.165

Base Plane

Seating Plane

10-6

Package Diagrams

T-90-20

84-Pin PLCC

Dimensions in inches MIN./MAX.

$\frac{0.048}{0.042}$ x 45°

.050 Typical

.020 Minimum

$\frac{1.185}{1.195}$ $\frac{1.150}{1.156}$

$\frac{1.090}{1.130}$

$\frac{1.150}{1.156}$

$\frac{1.185}{1.195}$

$\frac{0.090}{0.120}$

$\frac{0.100}{0.165}$

Base Plane
Seating Plane

120-Pin PQFP

Dimensions in inches MIN./MAX.

$\frac{0.913}{REF}$

$\frac{0.0315}{REF}$

Detail A

Pin 1

$\frac{1.218}{1.238}$ $\frac{1.098}{1.106}$

$\frac{0.012}{0.018}$

$\frac{0°}{7°}$

$\frac{0.060}{0.095}$

$\frac{0.010}{0.013}$

$\frac{1.098}{1.106}$

$\frac{0.125}{0.144}$

$\frac{1.218}{1.238}$

Detail A

10

10-7