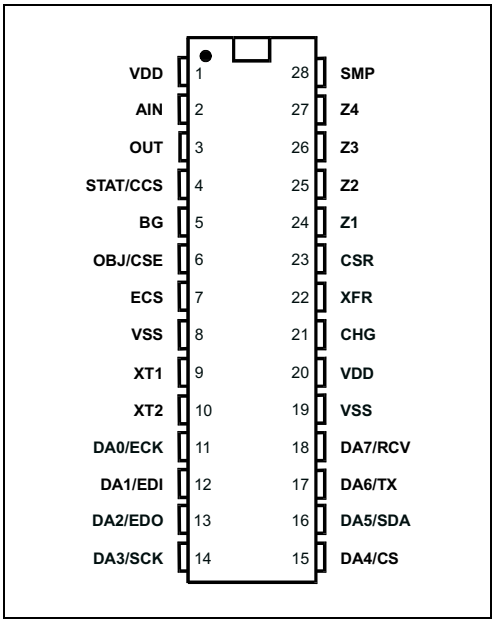
# QProx™ QT9701B2
## CHARGE-TRANSFER CAPACITANCE SENSOR IC

- **Auto calibration on demand**
- **Multistage internal digital filtering including median filter**
- **200µs minimum response time**
- **200ns to 1.4µs selectable drive pulse width**
- **4-stage charge cancellation for large load capacity**
- **Psuedorandom burst modes**
- **Programmable sensitivity, hysteresis, response time, digital filtering, detection mode, drift compensation**
- **Extensive post-detection processing**
- **Analog sample gate control line**
- **LED status indication**
- **Shorted electrode detection**
- **Uses cloned eeprom setups from E2SR board**
- **SPI and UART serial interfaces to 5MHz data rate**
- **AD7303 SPI DAC drive support for analog output**
- **5 volt single supply operation**




## APPLICATIONS

- **Fluid level sensing**
- **Security sensing**
- **Moisture detection**
- **Switch replacement**
- **Distance gauging**
- **Material properties analysis**
- **Human presence detection**
- **Collision avoidance**
- **Transducer drivers**

## DESCRIPTION

The QT9701B2 is an enhanced version of the QT9701B. It is both functionally and pin compatible with that device; the additional features of the 'B2' are fully transparent when the device is used in a 'B' circuit. Operation in the 'B' mode is referred to as 'Mode 1'; enhanced B2 functions are referred to as 'Mode 2'.

Enhancements over the QT9701B include an additional median filtering option, a 5MHz SPI serial port output, a bidirectional UART serial port, synthetic analog output capability, Setups cloning capability (both in and out), and reversible output and transfer-switch drives. Data transmitted can include raw or filtered analog, condition codes, reference level, or the detection integrator count. The UART serial port allows all the Setups of the device to be completely reprogrammed from an MCU. The serial protocol is the same as that used in the E2SR board, and the device is fully compatible with QTWinView™ PC software.

The QT9701B2 includes a fast onboard ADC for signal acquisition and incorporates high speed digital signal processing to deliver up to 200µs response times. Virtually all internal processing function can be enabled, disabled, or altered to suit a specific application by the simple addition of an inexpensive 8-pin serial $e^2$prom.

The QT9701B2 can perform a 'learn by example' autocalibration, where the object to be sensed is presented and ‘learned’ to create the proper threshold point. It is also possible to recalibrate the device remotely on demand via an external control line or over the serial port. The numerous autocal methods eliminate the need for potentiometer adjustments. Sophisticated threshold options allow detection on positive or negative signal swings, or both, and can incorporate preset time delays before final detection confirmation.

Applications include noninvasive continuous level sensing, displacement measurement, human proximity, moisture measurement, Robotic sensors, transducer interfaces, and switch replacement.

The device requires only a single +5 volt regulated supply, for example from a common 78L05 3-terminal regulator.

**AVAILABLE OPTIONS**

| $T_A$ | SOIC (S) |
|---|---|
| $0^0$C to $+70^0$C | QT9701B2-S |
| $-40^0$C to $+85^0$C | QT9701B2-IS |
| $-40^0$C to $+125^0$C | QT9701B2-ES |

# 1 - OVERVIEW

The QT9701B2 is a superset of the popular QT9701B QProx sensor IC. It adds enhanced filtering and I/O capabilities while remaining 100% backwards compatible with the QT9701B.

The QT9701B2 implements all charge-transfer (QT) control and signal processing functions necessary to make a highly sensitive and stable capacitance sensor. Only a few low cost external parts are required to make the unit fully functional; these can be readily selected for a specific range of capacitance detection.

A block diagram of the device is shown in Figure 1-1. Figure 10-4 shows a typical sensor circuit using the device.

## 1.1 BASIC OPERATION

The QT9701B2 is a burst mode QT controller. QT cycles are executed via bursts of pulses on control lines CHG and XFR. CSR is provided to reset the charge detection capacitor Cs, and line SMP is provided to permit analog sampling of the amplifier signal, to create a direct analog output if desired. The number of pulses per burst is controlled via an external $e^2$prom, or in the absence of an $e^2$prom, it is set to 64 / burst. Timing information is found in Figure 11-1.

With each XFR control pulse, charge accumulates on cap Cs. The more transfer pulses within a burst, the higher the gain, but also the higher the accumulation of charge due to stray Cx. More transfer pulses also produce an averaging effect, with Cs acting as an integrator to produce an average of all charge accumulated within a burst. The voltage on Cs may become large enough to produce a significantly nonlinear response; charge cancellation methods are used to 'buck' the accumulation of charge as described below.

At the end of each burst, the amplified signal from Cs is converted to digital in the device and further processed. Internally the device contains several selectable processing paths which may be employed to filter noise, compensate for signal drift, and create different sensing effects.

The sensor also provides a STAT pin which acts to indicate the current state of the sensor, and an OUT pin which provides the primary output when the signal reaches a predefined criteria such as exceeding a specified signal level. The device also features a bidirectional UART based interface which can both program the $e^2$prom and download data and status from the device in real time. It also has a synchronous SPI interface, running at a 5MHz transfer rate that can be used to off-load data.

## 1.2 BACKGROUND CX SUPPRESSION

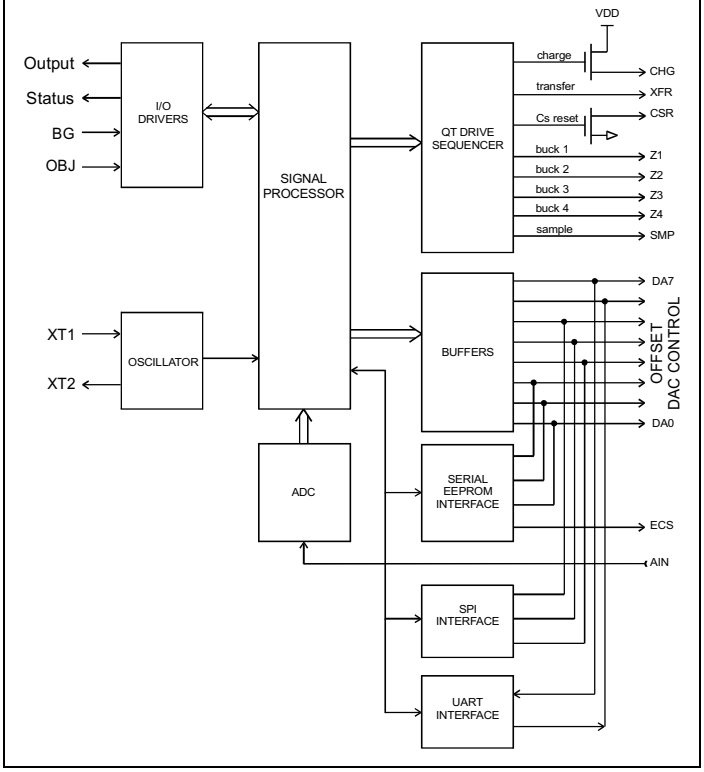
Stray background 'Cx' is an extremely important factor in many sensor systems. For example, an attempt to convey the capacitance effect to a remote object often requires a shielded cable which will add an offset capacitance. There are many other possible sources of such loading, for example the electrode itself, which may be in close proximity with another surface. In most cases background 'Cx' is vastly greater than the signal to be observed, and without some compensating mechanism can swamp the sensor.

The QT9701B2 employs two strategies for suppressing background Cx.

### 1.2.1 Cz Charge Cancellation

The first method of charge cancellation involves the use of external capacitors Cz1 through Cz4, and corresponding IC pins Z1 through Z4. Normally Z1...Z4 are held to Vcc while CSR clamps Cs to ground. During the course of a burst, CSR is released, and one or more of lines Z1..Z4 may be driven to ground in sequence. Each burst is composed of 4 'sub-bursts' as shown in Figure 1-2; if the charge that accumulates on Cs is larger than about 0.3 volts, one of the Z1..Z4 lines will transition down to provide a charge cancellation effect, by creating a negative-going step on Vcs. The amount of charge so canceled should not produce a downward step of more than 0.25 volts by design, otherwise it is possible to inadvertently create non-acquireable gaps in the sensing range; the ADC cannot sense negative voltages, and too large a bucking step will potentially place the resultant final signal into negative territory. Figure 1-2 shows a burst having 16 pulses contained in 4 sub-bursts of 4 pulses each; as the number of pulses per burst changes, the number of

**FIGURE 1-1 BLOCK DIAGRAM**



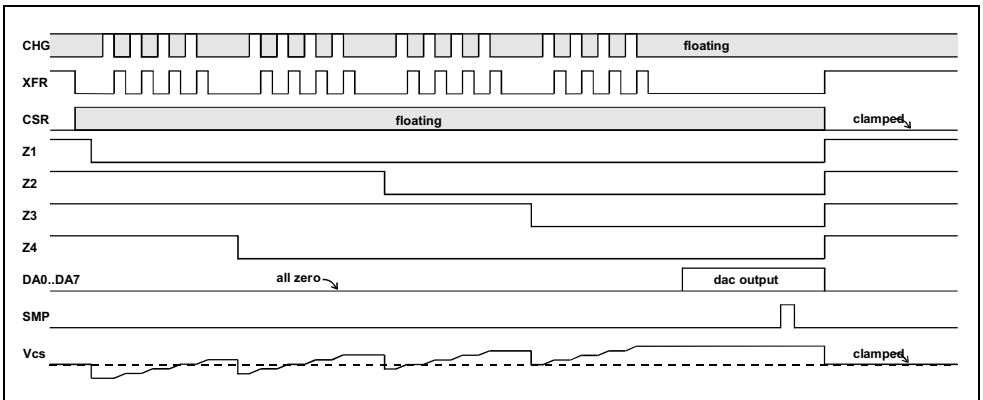




**FIGURE 1-2 BURST WAVEFORMS**

sub-bursts remains constant, while the number of pulses within each sub-burst is altered.

The amount of each bucking step is easily computed by the ratio of the values of Cz to total capacitance:

$$[1]\quad V_Z = \frac{-Vcc \cdot C_Z}{C_S + 4C_Z}$$

where all Cz's are equal.

Four Cz's are not always required, and in lightly loaded systems none at all may be needed. In certain applications the background load may be quite predictable or limited to a maximum value, and so the number of Cz caps can be held to a minimum. Adding Cz caps reduces system gain unless Cs is reduced to compensate.

#### 1.2.2 DAC Charge Offset Circuit

The second way background Cx is accommodated involves an R2R ladder DAC driven via pins DA0 - DA7 (in Mode 1 operation) or an AD7303 serial DAC (Mode 2). After a burst has completed, but before the ADC conversion begins, this DAC is driven to a level calculated to bring the amplified signal to within a suitable portion of the ADC's range. The DAC value required to do this is iteratively determined during the self-cal process.

During the self-calibration process, the device acts to find the optimum combination of Cz charge cancellation and DAC offset. It does so by first setting the DAC offset to a high value and then applying increasing amounts of Cz cancellation in successive steps until the signal is below 0.3 volts of Vcs, as required. Then, the value of the DAC offset is fine tuned to bring the analog signal into the desired range specified by the Reference Offset setting (Setup [2] - see Table 7-1).

Cz cancellation and the DAC offset are fixed while the sensor runs. If an e$^2$prom is installed, these values of cancellation and offset can be stored for reuse on successive power-ups, otherwise a recalibration on each power up will be performed.

# 2 - OPERATING MODES

## 2.1 MODE 1

Mode 1 is the QT9701B - compatible mode; it is engaged either by operating the device without an external e$^2$prom, or by having an e$^2$prom whose setting [U] is set to '0' (see Table 7-1). All data and operation pertaining to the QT9701B2 in Mode 1 can be found in the QT9701B data sheet.

The device offers three enhancements over the QT9701B in Mode 1: 1) An additional Median filter of length 9; 2) Selectable OUT and XFR polarities; 3) Ability to force default settings into the e$^2$prom on a cold restart if desired.

## 2.2 MODE 2

Mode 2 is the enhanced operating mode, and is entered by setting setup [U] to 1 or higher (see Table 7-1). The R2R ladder DAC must be replaced by an Analog Devices AD7303 dual 8-bit DAC for proper operation or an external CMOS shift register and an R2R ladder. No other circuit changes are required for Mode 2, although other circuit enhancements are supported. Refer to Figure 10-4 for a schematic of the E97S eval board which uses the enhanced hardware features.

#### 2.2.1 DAC Offset Circuit

The Mode 2 DAC must be an AD7303 dual 8-bit ADC, or a shift register connected to a parallel DAC for proper operation. Refer to Figure 5-1. The shift clock SCK is found on pin 14, data SDA on

## TABLE 1-1 PIN DESCRIPTIONS

***Functions available only in Mode 2**

| PINS | NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1, 20 | Vdd | Pwr | Power pin to +3 to +5 volts regulated. |
| 2 | AIN | I | Analog input from opamp, range Vss to Vdd. |
| 3 | OUT | O | Detection line output. *Active high or low depending on Setup [J]. |
| 4 | STAT/*CCS | O | Status line, intended primarily for driving an LED to give a visual indication of sensor health and state.<br>*Additional Mode 2 function: Secondary function is as an enable-high line to a 'clone in' eeprom temporarily connected to the circuit. |
| 5 | BG | I | Background calibration input line, active low. |
| 6 | OBJ/*CSE | I/O | Object calibration input line, active low.<br>*Additional Mode 2 function: Generates a negative framing pulse for an external SPI device to receive data from the 9701B2, of 8 or 16 bits length. |
| 7 | ECS | O | Eeprom enable line. To prevent startup transients from affecting the external eeprom it is advised to use a pull-down resistor of 10K to 20K ohms. Also issues a positive 1us pulse prior to each burst for diagnostic use. |
| 8, 19 | Vss | Pwr | IC negative supply (ground). |
| 9 | XT1 | I | Crystal or resonator input pin. If desired this pin can be driven from an external source, saving a part. If a crystal or resonator is used on XT1 / XT2, the pin should be loaded with a 20pf to 27pf capacitor to Vss. |
| 10 | XT2 | O | Crystal or resonator output pin. If desired this pin can also drive another device if lightly loaded or buffered. If a crystal or resonator is used, the pin should be loaded with a 20pf to 27pf capacitor to Vss. |
| 11-18 | DA0-DA7 | O | Outputs the DAC value for an external R2R ladder network to create an offset for the external amplifier chain. Note additional alternate functions below. |
| 11 | ECK | O | Clock output to the serial eeprom. |
| 12 | EDI | O | Serial data output line to serial eeprom |
| 13 | EDO | I | Serial data input line from serial eeprom |
| 14 | *SCK | O | *Mode 2: Serial SPI clock |
| 15 | *CS | O | *Mode 2: Chip select line to AD7303 DAC |
| 16 | *SDA | O | *Mode 2: SPI data output line to AD7303 / other SPI device(s) |
| 17 | *TX | O | *Mode 2: Transmit uart data from the device |
| 18 | *RCV | I | *Mode 2: Receive uart data to the device |
| 21 | CHG | O | Charge line to drive a sensor electrode |
| 22 | XFR | O | Control line to drive an external transfer fet |
| 23 | CSR | O | Control line to reset the Cs capacitor between bursts |
| 24-27 | Z1-Z4 | O | Charge cancellation control lines to drive Cz1 - Cz4 |
| 28 | SMP | O | Sampler control line to sample external analog signal |

16, and sync frame CS on 15. The data is shifted out using standard SPI protocol, and clocked into DAC_A of the AD7303 on the rising edge of SCK. Two bytes are transmitted to generate the control and data bitstream required by the AD7303.

#### 2.2.2 Synthetic Analog Output

Synthetic analog, of a type determined by Setup [U], is output on AD7303 DAC_B once shortly after each burst. The data is sent to the DAC using the SPI protocol and timings shown in Figure 5-2 or Figure 5-3, as framed by the CS line.

#### 2.2.3 External Data SPI Port

The same port used to drive the AD7303 can also be used to send data to an external circuit. After each burst, data is transmitted over SDA, clocked by SCK, and framed by a negative pulse on the OBJ line. OBJ is open-drain, and must be pulled high by a 2K to 2.2K resistor to create the framing pulse. OBJ function is not compromised by this dual-usage of pin 6. An external interface to OBJ should use an open-drain (or open-collector) drive to prevent interference with framing pulse. Both 8-bit and 16 bit transmissions are possible; in a 16 bit transmission the second byte framed by OBJ (the third actual byte in the sequence) is a Status codes byte. Figures 5-2 and 5-3 show the waveforms associated with these transmissions.

#### 2.2.4 UART Circuit

An interface to an external host MPU is possible using a full-duplex serial port running from 9600 to 115.2kbaud. The protocol is the same as that described in the E2SR manual, and the QT9701B2 is fully compatible with QTWinView software. There is no hardware handshaking. Both verbose and polled communications are possible; the baud rate and communications mode are determined by setup [G]. A MAX232-type interface driver circuit is all that is required to implement true RS232 communications. When interfacing directly to a host MCU, the MAX232 is not needed.

The RS232 interface should have its own voltage regulator, since these devices generate considerable switching noise on Vcc from their internal charge pumps and from the current transients generated from driving the capacitance of long cables.

# 3 - CIRCUIT OPERATION

## 3.1 QT DRIVE CIRCUITRY

The QT9701B2 allows for inverted transfer switch drive: this allows use with certain types of n-channel bus-switches known for having particularly low resistance and low charge injection. The polarity of the transfer switch drive is determined via setup [J].

#### 3.1.1 Using a Mosfet Transfer Switch

If using a mosfet transfer switch, it should be an n-channel enhancement device. The Philips BSN20 (smt) is reasonable for general purpose use. Lateral DMOS devices like the Calogic SST211 (smt) are better parts in general; they have very low amounts of charge injection, although their higher on-resistance which may limit their use with short pulsewidths in some cases.

#### 3.1.2 Using a 'Bus Switch' Transfer Switch

The 9701B2 is also capable of driving single-gate 'bus-switch' mosfets, like the Texas Instruments SN74CBT1G125 (single, SOT23-5) or Quality Semiconductor QS3125 (quad, SO14). These are low cost devices with low charge injection and excellent thermal stability. They are active-low enable, thus the polarity of the transfer drive must be selected as 'LOW' in Setups [J] .

#### 3.1.3 Shortening TPW Further

In some cases it is highly desirable to suppress the effects of moisture in and around the electrode, or to help ascertain the bulk properties of a substance without reacting much to moisture content. There are also times when external interference must be suppressed further than simple signal processing can achieve. Shortening the transfer time to below 200ns is possible with the aid of some external circuitry (Figure 3-1). This circuit will generate almost arbitrarily short transfer times, to the limits of the gate and switch propagation delays. Rt and Ct can be adjusted using an oscilloscope; a trimpot can be used for Rt if desired.

This circuit can be disabled by removing Rt, while jumpering Ct to ground. When using this circuit it is important to keep the width Setups at 200ns ( [4.0] ).

Transfer switch closure time should be long enough so that transfer efficiency does not suffer. Very short transfer times (<100ns) can produce unpredictable results if significant ground and signal lead inductances are present, or if the matter to be sensed is of varying electrical conductivity. In general, signal levels and gain will appear to drop with shorter transfer times due to the increasing inability of the field currents to settle before the end of the transfer period.

## 3.2 DAC REQUIREMENTS

An 8-bit DAC is required in most implementations to provide a subranging ADC system. The DAC is used to 'servo' the analog signal to a range within the input limits of the on-board 8-bit ADC.

**In Mode 1:** An inexpensive 8-bit R2R ladder DAC is used. The CMOS drive of the device functions to drive this R2R DAC, with no further buffering required. The R2R should be 50K ohms or higher in value. CTS's p/n 750-107R100K (SIP) is suitable for this function.

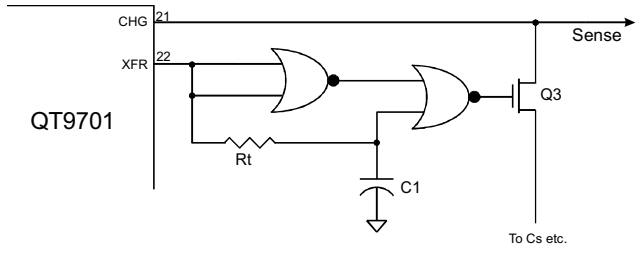
**In Mode 2:** An Analog Devices AD7303 dual SPI DAC can be used. The second half of this DAC can also be driven by the QT9701B2 to create a synthetic (signal processed) analog output. Alternatively, an 8-bit CMOS shift register can be coupled to the SPI port and used to drive an R2R ladder of the type described above.

## 3.3 AMPLIFIER REQUIREMENTS

The external amplifier can be almost any moderate speed rail-to-rail output and ground-sensing input CMOS or JFET input device having a 2MHz GBW or better. Bipolar input opamps are to be avoided due to their higher input currents. Amplifiers in the same class as the TI TLC2272 and Burr Brown OPA2340 are acceptable. Two gain stages should be cascaded for if desired total gain is above 25; attempting to achieve a very high gain in one stage can result in settling time problems. It is advisable to use opamp feedback resistor values of under 200K ohms to speed settling times, these should be placed very close to the opamp pins to reduce parasitic capacitances.

There is generally no problem in using the same Vcc supply for the opamp as for the QT9701B2, provided normal supply bypassing is performed.

**Figure 3-1 Circuit for Short Transfer Times**



## 3.4 EXTERNAL EEPROM; CLONING

The external 93LC46A (Microchip) e²prom should be used; its contents can be cloned in from an external source (Section 3.4).

Substitute devices should have both byte-access and streaming-access modes. Many variants of the 93LC46A are only word access or non-streaming and will not function. The e²prom's contents are described fully in Section 12. A plain blank e²prom will be ignored. Refer to Table 7-1 for the Setup modes which can be enabled and altered using the external e²prom.

### 3.4.1 Cloning-In of Setups

Cloning in from an external e²prom requires that the external e²prom's IO pins be free. An E2SR board running in its Setup mode does this, for example. The STAT line is used to enable the external e²prom being accessed. Also, after a successful clone-in the STAT line will flash 5 times in quick succession.

The QT9701B2 checks for the presence of an external cloning e²prom source during powerup, and also just after the OBJ line is asserted low momentarily and then released; if an external e²prom is found it will be read and copied in to the onboard e²prom. The clone source should be removed immediately after the STAT confirmation pattern begins.

It is also possible to force a clone function via the serial port, using a Forced Reset (Section 4.4.6) to cause the device to scan for an external e²prom.

### 3.4.2 Cloning-Out of Setups

Cloning out to another QProx product requires that the 93LC46A connected to the QT9701B2 have its control lines floating. This occurs only while the OBJ line is held low. It is possible to clone to another QT9701B2 circuit, for example, thus created a low-cost e²prom duplicator for moderate volume production use.

### 3.4.3 ECS Line

The ECS line (pin 7) enables the e²prom for reading and writing; it is active-high. It also produces a 1us positive pulse just prior to each burst for diagnostics; this pulse does not interfere with the operation of the e²prom. The ECS line should be pulled low with a 10K to 20K resistor to prevent power-up transients from causing false-writes to the e²prom.

## 3.5 OUT PIN

The OUT pin can be made active high or active low. The polarity of Out is determined by Setup [J].

OUT becomes active if the signal has crossed a threshold detection level and the appropriate Setups are engaged to allow OUT line to indicate detections. Setup functions are described in detail in Sections 7 and 8.

OUT can also become active if the CHG pin detects a short circuit to ground.

## 3.6 STAT PIN

STAT operates the same as in the QT9701B, but in the B2 it is also used to indicate the success of a clone-in operation. After a successful clone-in it will flash 5 times in quick succession. There is no indication for clone-out.

The STAT line acts as a multipurpose indicator that shows output state, error conditions, and input feedback. It is designed to drive an LED for meaningful operator feedback. STAT will output as follows depending on sensor state:

**Running and not detecting:** STAT outputs a positive 10ms pulse at a 10Hz rate (10% duty cycle); on an LED this generates a low, very noticeable flicker.

**Running and detecting:** STAT outputs a positive 90ms pulse at a 10Hz rate (90% duty cycle); on an LED this generates a bright but flickering output.

**When an input line (BG or OBJ) is evoked:** STAT is forced low for the duration the input line is held low.

**If BG or OBJ are evoked for >2secs:** After input release, STAT will go “solid high” for ¾ second before it enters the new mode.

**While calibrating:** STAT will be forced “solid low”; this usually takes well under a second.

**If CHG is shorted to ground while normally running:** STAT will go “solid high” for the duration of the short.

**On a calibration error:** STAT will output a repeating error code, provided that Output Error Code [E.a] is ‘on’:

| | |
|---|---|
| **Single repeating pulse:** | **CHG shorted to ground** |
| **Double repeating pulse:** | **Excess capacitive load** |
| **Triple repeating pulse:** | **Unstable signal, cannot calibrate** |

The device will repeatedly try to recalibrate between each set of ‘Morse code’ outputs. If [E.a] is off, the recalibration attempts will be much quicker, since the STAT codes are not output.

The repeating STAT code pulses are 250ms in duration with a 250ms dead time between pulses; between coded pulse groups there is a minimum 750ms dead time

## 3.7 SMP LINE

The SMP line is an active-high sample gate that can close a 74HC4066-type analog switch briefly at the end of each burst to sample-and-hold the resulting raw signal. The pulse is 4.2us wide.

## 3.8 BG / OBJ INPUTS

These control logic inputs are active low, and to use them should be pulsed low momentarily for at least the burst spacing duration; thus, if the burst spacing is 1ms, the line should be held low for at least 1ms. To engage the BG or OBJ “mode override” functions the line should be evoked for >1.6 seconds prior to release. Note that if only a simple BG or OBJ recal function is desired, it is important to not hold the line low so long that this override feature is engaged. Refer to Section 3.15 for more information about the BG and OBJ modes.

## 3.9 OSCILLATOR

Almost any 20MHz ceramic resonator will work. A quartz crystal will also function, but aside from a slight boost in accuracy, and longer startup time. The resonator should have two capacitors to ground on either side, of 15pF to 27pF. 3-pin devices having internal capacitors are available, saving considerable board space and cost.

An external oscillator having CMOS drive levels may also be used, by connecting the oscillator to pin 9 and leaving pin 10 open. The oscillator should have a 45% to 55% duty cycle.

Lower frequencies may be used if desired for reduced power consumption, however all timing functions are slaved to the oscillator and will thus slow down as well.

## 3.10 INPUT PROTECTION

The CHG drive and BG and OBJ lines are internally protected from ESD by clamp diodes, however, this should not be relied upon as a primary means of protection. It is highly recommended that any pins exposed to the outside world, including CHG, be clamped via two high speed, high conductance, low-C silicon diodes like type 1N4150 or BAV99 (smt), one from ground to the pin, and the other from the pin to Vcc or to a zener diode biased up to at least the level of Vcc, and that a resistor be placed between these clamp diodes and the CHG pin to further limit pin currents. See Figure 14-1.

Note that the QT9701B2 forces the XFR line high and clamps the CSR line low between bursts to self-clamp and dissipate ESD currents.

## 3.11 CHG SHORT CIRCUIT DETECTION

The QT9701B2 can sense shorts to ground on CHG. When a short is detected, the OUT and STAT lines are forced active for the duration of the short. Short detection operates by monitoring output current through the internal p-mosfet device; external ESD circuits that include a series resistance can limit this current artificially, thus rendering the short detection system ineffective. Operation of the short detection circuit is thus not guaranteed under all conditions and should only be relied upon as a backup detection method. Also, note that the device cannot determine open electrode conditions.

## 3.12 POWER SUPPLY AND PCB LAYOUT

The device requires a stable, noise-free power supply. A low cost 78L05 class regulator will work fine for virtually all applications, but it should not be shared with devices that can produce transients or erratic loading. Designs should use a regulator specifically for the QT9701B2 if possible; testing can determine if the regulator could be shared with other circuitry.

The 78L05 should be properly bypassed on its input and output. Its input supply should also be relatively stable and noise-free so as to minimize feedthrough noise components via its pass transistor. A 22µF tantalum or 100 µF low-Z aluminum capacitor is recommended on the output of the 78L05.

A PCB ground plane or copper pour area throughout the circuit is highly recommended. Other circuits, including any output driver transistors, should not allow their currents to flow through the sensor's circuit area; grounds should always be led back to a common tie point at the point near the entry of the supply onto the PCB in accordance with customary "sensitive analog" practice.

Sense lead clamp diodes should shunt ESD currents back to earth via the most direct route possible, without traversing the area of the circuitry; ESD return currents should also not share a common ground path with the sensor circuitry. These clamp diodes should shunt as directly to a board mounting hole (or other major ground tie point) as possible. Positive clamped ESD currents are often neglected in designs; they should be shunted via a high quality low inductance bypass capacitor and/or zener back to the same ground tie point.

Component location is relatively unimportant and non-critical, with the above noted exceptions, and the circuit can easily be implemented on a 2-layer PCB.

## 3.13 ANALOG OUTPUT VIA SMP LINE

An analog output may optionally be obtained using a sample and hold circuit. The QT9701B2 provides a sample pulse (SMP) which is a positive-drive pulse timed to coincide with a stable portion of the output of the signal amplifier chain.

The sample and hold can be made of a 74HC4066 type switch and a 1nF ceramic capacitor, followed by a CMOS buffer amplifier.

When using a S/H circuit to obtain an analog output, avoid using a quad opamp shared also as the main gain amplifier, instead of two separate packages. The slew rate and loading of the S/H buffer can produce major disturbances in other opamps on the same die.

The SMP line should never be routed near the Cs sample cap or the amplifier opamp chain, as this pulse can easily superimpose a severe transient on the signal at the exact moment where it should be stable.

## 3.14 - SENSOR RESOLUTION

The sensor's overall sensitivity is a function of several factors, including:

1. Total sampler capacitance, Cs + (Cz1 ... Cz4) = $C_T$
2. Burst length, N
3. Total amplifier gain, Av
4. ADC resolution, bits, n
5. Power supply voltage, Vs

Differential gain at the output of the operational amplifier is determined by:

[2] $$\frac{N\,Vs\,A_V}{C_T}$$ {volts / Cx}

The ADC resolution is defined in terms of volts per level, resulting in the following overall sensitivity equation:

[3] $$\text{Sensitivity} = \frac{\text{ADC resolution}}{\text{differential gain}}$$

$$= \frac{V_S / (2^n - 1)}{N\,V_S\,A_V / C_T}$$

$$= \frac{C_T}{N\,A_V (2^n - 1)}$$ {Cx per ADC level}

Given: Ct = 0.056 µF + 4 x 0.0047 µF = 0.0748 µF

N = 64, Av = 284, n = 8 bits

Then the overall sensitivity is about 16 femtofarads per ADC level. This can easily be adjusted by altering any of three parameters: N, which can be altered in the $e^2$prom setups, amp gain Av, and total sampler capacitance Ct.

Note that supply voltage Vs conveniently drops out of the equation - thus, the sensor is largely immune to slow changes in supply voltage, although it can be sensitive to transient supply excursions which do not equally affect all aspects of the acquisition process.

## 3.15 BG, BG/OBJ, AND OBJ MODES

The QT9701B2 operates in either of two primary calibration modes:

1. **'Normal' mode:** sensor makes use of the setting of Detect Threshold. This mode is the factory default setting. Evoking BG in 'normal' mode simply causes a recalibration to occur, that is, the reference point is recentered and with it the threshold level(s). 'Normal' mode is BG mode and is referred to as BG mode.
2. **'Learn' mode:** The sensor ignores Detect Threshold, and 'learns by example'. There are two variations of 'Learn' mode: BG/OBJ, and OBJ.

**Switching modes:** These modes can be entered into at will by the use of the BG and OBJ control lines as explained below.

**Making the mode permanent:** The selected BG, BG/OBJ or OBJ mode can be stored "permanently" into the external $e^2$prom if present, but only if Data Locking [F.b] is on. The mode can be changed at any time and is automatically stored again into the $e^2$prom, overwriting the prior mode. If Data Locking is set to 0 or 9, or if the $e^2$prom is absent, the unit will always power up in BG mode and immediately perform a full calibration after startup.

**Mode manipulation over the UART port:** The BG, OBJ, and BG/OBJ modes can be modified at will via serial (UART) commands. A serial command operates exactly like a port pin assertion, with the exception that a 'long' assertion is replaced by a capital letter command. For example, To assert a BG command, the lowercase letter 'b' is sent to the device. To assert a BG override command, the letter 'B' is sent. The OBJ command is accomplished via the letters 'o' and 'O'. Refer to Section 4 and Table 4-1 for details.

### 3.15.1 When to Use Each Mode

Mode selection depends on the sensing effect desired.

**BG:** BG mode is designed to allow advanced processing functions like “prox trap” while also permitting drift compensation. BG only requires a single command to calibrate to the background level, but the threshold level must be set via the e²prom and cannot be ‘learned’. BG will also permit maximized sensitivity with background reference drift tracking at all times. It will also permit ‘motion’ detection processing, where motion in either direction will cause a detection. OBJ and BG/OBJ cannot provide these functions.

**OBJ:** Use for detecting objects that generate large signals, where little processing finesse is required. Evoking OBJ will trigger a “learn by example” and set the threshold automatically, and store that setting into the e²prom if present. If no e²prom is present, this mode must be entered and recalibrated after each power up by evoking OBJ. This is a simple fixed threshold point without knowledge of the background reference level.

**BG/OBJ:** For “learn by example” calibration with continuous background drift compensation. This mode can be thought of as a hybrid between the ‘pure’ BG and OBJ modes. It requires two input commands, one first on the BG line, then one on OBJ. If no e²prom is present, BG/OBJ must be entered and recalibrated after each power up.

The BG input is first used to set the background reference signal calibration point; then, the object to be sensed is introduced to the sense field, and the OBJ line is toggled. The sensor then 'learns' the signal from the object to create a threshold point, but it also still 'knows' the background reference level (hence, 'BG/OBJ'). With the knowledge of the background level, the sensor can compensate for drift when the object is absent.

### 3.15.2 BG Mode Details

In BG mode the threshold level(s) are taken from Detect Threshold [0], while hysteresis is defined by [1]. There are also some further issues related to Data Locking:

I**f Data Locking [F.b] is off** or e²prom absent, the unit will power up and perform a background calibration to set its initial reference point; the unit will always start out in BG mode if Data Locking is off or the e²prom is absent.

**If Data Locking [F.b] is on**, unit will use stored e²prom cal settings on powerup and not perform a BG cal. If the BG cal point has changed, it will be necessary to evoke the BG line to recalibrate, or wait until a Max On-Duration expires (if enabled and if a detection is in progress), or wait until drift compensation catches up to the error (if enabled).

Evoking BG (or sending the letter 'b' or 'B' via UART) if already in BG mode causes a full background recalibration; the unit will remain in BG mode. If Data Locking is on, evoking BG will cause the resulting cal data to be stored for reuse on next powerup.

Evoking BG (or sending the lowercase letter 'b' via UART) if in BG/OBJ mode causes a background reference point recalibration, but the prior learned threshold levels will not be altered and BG/OBJ mode will remain in force. See “BG/OBJ Mode Details”, below.

If Data Locking is on, the calibration settings resulting from a prior BG evoke will be stored in the e²prom for retrieval on any subsequent powerup.

**Forcing to BG mode from OBJ mode:** Evoking BG (or sending the letter 'b' or 'B' via UART) if the device is in OBJ mode will take the device out of OBJ mode and put it into pure BG mode, triggering a BG recal as well.

**Forcing to BG mode from BG/OBJ mode:** If device is in BG/OBJ mode and it is desired to change the mode to “pure BG” mode, evoke the BG line for >1.6 seconds (or send the uppercase letter 'B' via UART). After the BG line is released high, the STAT line will go “solid high” for ¾ second and the device will then recal. At this point it will be in “pure BG” mode. If STAT does not go “solid high”, the line was not evoked long enough.

### 3.15.3 OBJ Mode Details

OBJ mode is entered by the following process:

**Device has just powered up and is not in BG/OBJ mode:** With a target signal present (target placed at the point of desired detection) evoke OBJ (or sending the letter 'o' or 'O' via UART). Unit learns the correct threshold from the current signal level and enters OBJ mode.

**If device already in BG or BG/OBJ mode:** With a target signal present at the edge of the desired range, evoke OBJ for >1.6 seconds to clear out the BG mode and also to prevent the BG/OBJ mode from being entered (or send the uppercase letter 'O' via UART). Unit enters OBJ mode and learns the correct threshold level.

**If device already in “pure OBJ” mode:** Evoking OBJ (or sending the letter 'o' or 'O' via UART) will cause a new detection threshold point to be learned at the current signal level; unit remains in OBJ mode.

If in doubt, evoke OBJ for >1.6 seconds (or send the letter 'O' via UART). The STAT line will go “solid high” for about ¾ second and then the device will recal in pure-OBJ mode. If STAT does not go “solid high”, the line was not evoked long enough.

**Hysteresis in OBJ Mode:** The hysteresis value is taken from the value of the Detect Threshold setup, or can be forced to zero hysteresis if Hysteresis setting [1] is set to [1.3] (0 hysteresis) via the e²prom. If the e²prom is absent, the hysteresis is set to 8 counts of signal by default. For example, if the Detect Threshold is set to [0.6], and Hystersis is set to [1.1], the actual hysteresis used in OBJ mode is fixed at 11 counts of signal.

If the hysteresis is too large for the signals encountered, ‘sticking’ can occur; the sensor will detect an object (usually immediately after evoking OBJ) and not release. If expected signal levels are small, BG/OBJ mode is a better option than pure OBJ because BG/OBJ will set an amount of hysteresis proportionate to the signal level.

OBJ mode has no knowledge of the background reference level, and so cannot drift compensate for background level changes. OBJ sets a rigidly fixed trip point at an absolute signal level.

OBJ will only work with Detection Mode [D] set to [D.0] or [D.8]. All other settings of [D] are ‘truncated’ to [D.0] or [D.8], whichever is closest in Table 7-1. Setting [D.8] can make the sensor respond to departing objects (an “absence detector”).

If Data Locking is enabled, the resulting OBJ setting and trip point will be stored in the e²prom for retrieval on subsequent powerup. Then, when the unit powers up it will use the stored e²prom settings and immediately run without recalibrating.

Evoking OBJ mode with only a background level of signal present will usually cause the sensor to stick ‘on’, and is not advised.

### 3.15.4 BG/OBJ Mode Details

To enter BG/OBJ mode:

1. Following a powerup, evoke BG (or send the lowercase letter 'b' via UART) when the known background signal level is present (object to be detected is absent). Evoking BG will make the device recalibrate and finds its new background reference level.
2. Then, with a target signal present (target object placed at the furthest distance of desired detection) evoke OBJ (or send the lowercase letter 'o' via UART). Unit then learns the correct threshold and sets the correct hysteresis levels.

## TABLE 4-1 - POLLED MODE ASCII COMMAND SET

| ASCII Code | Hex Code | Action |
|---|---|---|
| < | 0x3c | Reduces Pulse Width by one Setting to a limit of 200ns. The new setting is written to e$^2$prom, but unit does not recalibrate thus allowing comparative signal strength analysis. |
| > | 0x3e | Increases Pulse Width by one Setting to a limit of 1400ns. The new setting is written to e$^2$prom. The new setting is written to e$^2$prom, but unit does not recalibrate. |
| B | 0x42 | Performs the BG function (identical to asserting BG line, long) and overrides any BG/OBJ or OBJ mode. |
| b | 0x62 | Performs the BG function (identical to asserting BG line, short). |
| h | 0x68 | Returns hysteresis value (binary value, range 0..255). |
| l (lower case L) | 0x6c | Returns last received character |
| O (capital O) | 0x4f | Performs OBJ function (identical to asserting OBJ line, long); overrides any BG or BG/OBJ mode. |
| o (lower case O) | 0x6f | Performs the OBJ function (identical to asserting OBJ line, short). |
| p | 0x70 | Puts device into 'pure' Polled mode. See 'v' below and Sections 4.3, 4.4. |
| r | 0x72 | Resets the sensor. The command must be repeated within 90ms. See Section 4.4.6. |
| s | 0x73 | Places unit into Setups mode, and halts sensing. See 'w' below, and Section 4.4.1. |
| t | 0x74 | Returns signal threshold value (binary value, range 0..255). |
| v | 0x76 | Puts into Enhanced Verbose mode. See 'p' above and Sections 4.3, 4.4. |
| V | 0x56 | Returns part version. The returned byte is 0x21. |
| w | 0x77 | Write e$^2$prom with new Setups; 's' string must end in 'w'. See 's' above, and Section 4.4.1. |
| 0…8 | 0x30-0x38 | Returns binary data per Data Evoke Code (Table 4-2). See Section 4.4.3. |
| ^a…^w | 0x01-0x17 | Returns current Setups value in range 0…9 (0x30…0x39) of the Select item chosen (^a corresponds to Select [0], ^w corresponds to Select [U], where ^a means 'Alt-a' on a PC keyboard). |

If Data Locking is on (and e$^2$prom is present), the resulting cal data will be stored for retrieval on any subsequent powerup. Then, when the device subsequently powers up again it will use the stored e$^2$prom settings and immediately run with them, without performing a recalibration of any sort.

If the device is already in BG/OBJ mode, step 1 will not take the unit out of BG/OBJ mode; instead, step 1 will simply cause a recal of the reference point, leaving the differential threshold value from a prior step 2 alone. A subsequent step 2 can then set a new threshold level if desired.

If the device is already in BG/OBJ mode, evoking OBJ thereafter (repeating step 2) will cause the unit to establish a new 'learn by example' BG/OBJ threshold, leaving the reference level alone. Thus, once BG/OBJ mode is entered via the above 2-step process, you do not necessarily have to repeat step 1 to do a threshold recalibration; after evoking OBJ again it will remain in BG/OBJ mode and just properly recalibrate its threshold level.

If the device is in OBJ mode, it is cleared in step 1; evoking BG when in pure OBJ mode will always put unit into "pure BG" mode.

BG/OBJ mode can be used only with settings 0, 1, 8, or 9 of Detection Mode [D]. If settings other than these are programmed into the e$^2$prom in error, the erroneous settings will be 'moved' to one of these legal numbers when the BG/OBJ mode is entered.

### 3.15.5 Data Locking & Drift Store

Data locking allows the sensor to store reference calibration and threshold settings, as well as BG/OBJ and OBJ mode settings. If Data Locking is off (or the e$^2$prom is absent), the device will forget its prior settings when power is interrupted, including the fact that it might have been in a BG/OBJ or OBJ mode. BG/OBJ and OBJ modes require that fixed information be saved to operate, and so need to be manually restored after each powerup if Data Locking was not enabled.

Data locking operates seamlessly with BG, BG/OBJ, and OBJ modes; once Data Locking is specified via the e$^2$prom setups nothing else needs to be done. The unit will save all calibration data whenever BG or OBJ are evoked or whenever an automatic recalibration (due to a Max On-duration timeout, for example) occurs.

Drift Store mode makes the QT9701B periodically save to e$^2$prom the drift compensated reference level, so that if the unit is unpowered it will remember its last known reference when next powered up. The Drift Store save operation can be specified to occur periodically, from one minute to 10 minutes of spacing. Note that e$^2$proms have a limited cycle life; this may have an impact on selection of the e$^2$prom update rate.

The Drift Store operation takes 5 milliseconds to execute and interrupts sensing, but does not occur at all if the reference level has not changed. Thus, even with this mode enabled, in OBJ mode or if Drift Rate is set to "off", no e$^2$prom save will ever occur.

Setting to [F.1] allows Data Locking but prevents Drift Store from occurring on a timed basis.

Motion mode disables both Data Locking and timed Drift Store. Motion mode is a purely transient mode.

# 4 - UART OPERATION

There are two serial port data output options available on the QT9701B2: UART and SPI. Several variations of each can be selected such as baud rate and data type. Section 5 deals with SPI operation.

The UART serial modes exist primarily to transmit signal data to a destination such as a host controller. All data is output as 8 bits of binary.

Instead of signal data, the QT9701B2 can also be made to output a status byte, the detection integrator counter, or the internal reference level. The reference level is useful as an alternative representation of the signal, as it reflects the long-term average of

the signal level, and can be made to change very slowly via the adjustable drift compensation mechanism [8].

## 4.1 HARDWARE AND DATA RATES

The UART employs standard NRZ coding with no or software handshaking depending on the selected mode of [G]. Buffering with an interface device such as a MAX232 is required for operation with standard RS232 ports. Direct connection to a host device, such as an MCU, is possible without buffering.

UART modes are specified by Setup [G] in Table 7-1. UART data has the following format:

**Baud rate:** 9600, 19.2K, 57.6K, or 115.2K
**Length:** 8 bits
**Stop Bits:** 1
**Parity:** None

In addition, a special 'slow mode' is available at 9600 baud, with transmissions spaced 100ms apart to allow use with slow host equipment [G.6].

## TABLE 4-2 - EVOKE CODE RESPONSES

| EVOKE (ASCII) | EVOKE (HEX) | DATA TRANSMITTED |
|---|---|---|
| **0** | 0x30 | Signal (0..255) |
| **1** | 0x31 | Signal - Reference (0..255) |
| **2** | 0x32 | Reference (0..255) |
| **3** | 0x33 | Amplifier Offset (0..255) |
| **4** | 0x34 | Charge Cancellation (0..4) |
| **5** | 0x35 | Detect Integrator Counts (0..200) |
| **6** | 0x36 | Any item selected by Setup [U] |
| **7** | 0x37 | Status bits - see Table 4-3 |
| **8** | 0x38 | Error Code: See Section 4.5 |

## TABLE 4-3 - STATUS BYTE (H.7)

See Section 4.3

| BITS | MEANING |
|---|---|
| **0** | 1 = negative detection |
| **1** | 1 = positive detection |
| **2** | 1 = unit is busy (in calibration or startup) |
| **3** | 1 = an error has occurred |
| **4** | 1 = BG input detected |
| **5** | 1 = OBJ input detected |
| **6, 7** | unused |

## TABLE 4-4 - STATUS BYTE (U.8)

See Section 5.2

| BITS | MEANING |
|---|---|
| **0, 1** | Error code, value range 0..3 (see Table 4-5) |
| **2** | 1 = negative detection |
| **3** | 1 = positive detection |
| **4** | 1 = OUT pin is active |
| **5** | 1 = unit is busy (in calibration or startup) |
| **6** | 1 = OBJ input detected |
| **7** | 1 = BG input detected |

## TABLE 4-5 - ERROR CODE (H.8)

See Section 4.5

| VALUE | MEANING |
|---|---|
| **0** | No error |
| **1** | Short circuit suspected |
| **2** | Excess capacitive load |
| **3** | Unstable readings, cannot calibrate |

## 4.2 'NATIVE' VERBOSE SERIAL MODE

'Native' Verbose serial mode is specified by setting [G] to [G.5] or higher.

In this mode the device transmits data continuously. The data item sent from the UART is selected by Setup [H], Verbose Data.

Native Verbose mode is useful to send to the host a continuous data stream of one item, without the complexity of a bidirectional link. With this mode the selected data is transmitted on a continuous basis from the moment the unit powers up.

Verbose data is in the form of raw hex code. There are no headers or data blocks; data is merely a continuous stream of 8-bit hex code of the internal QProx data. Host receive protocol need not include anything for data synchronization; every character received will be a self-contained data point. No CR or LF codes are sent. Native Verbose mode begins immediately upon power up if setup [G] is set to [G.5] or higher.

## 4.3 UART DATA IN VERBOSE MODE

In Verbose mode (either 'Native Verbose' mode, set by [G.5] and up) or 'Enhanced Verbose' mode (polled mode in which the letter 'v' has been sent to the 9701B2) the device will transmit back a continuous stream of data. In Native Verbose mode the data sent is that specified by [H]. These data types reflect that found in the E2SR board, thus maintaining compatibility, and can be summarized as follows (see also summary Table 4-2):

0. **Synth** outputs filtered (synthetic) data, at the end of all enabled filter stages. It is an unsigned 8-bit signal value.
1. **Synth - Ref** returns the difference between the filtered signal and the current reference. The data is 2's complement binary: If the signal dips below the reference level, the data becomes negative.
2. **Ref** returns the current signal reference level.
3. **Offset** returns the current DAC offset value being fed to the amplifier chain (Out_A of the AD7303).
4. **Cancellation** returns the current charge cancellation value, from 0 to 4, representing the number of Cz capacitors being used to provide charge cancellation.
5. **DI** returns the current value of the Detect Integrator (see notes related to [B] in the QT9701B data sheet).
6. **From U** returns the value specified by the current setting of Select [U].
7. **Status** returns the current Status Byte according to Table 4-3. Note that the Status Byte of [U.8] is not the same.
8. **Err Code** returns the current error code (see Section 4.5).

In 'Enhanced Verbose' mode, any of the above items can be selected 'on the fly' by sending any one of ASCII characters '0' through '8' corresponding to one of the above data items. The resulting continuous datastream will persist until a differing character is sent to the 9701B2.

## 4.4 POLLED UART MODE

Polled UART mode is specified by setting [G] to a setting between [G.1] to [G.4].

In this mode the device waits for an ASCII 'Evoke Code' from the host before sending data back. In this mode the device can also be put into an "Enhanced Verbose' mode temporarily. The data character sent back to the host is sent immediately after receipt of the Evoke Code. In Enhanced Verbose mode, the data is identical to regular Verbose mode, however the data stream can be altered 'on the fly' repeatedly to different parameters by sending new Evoke Codes in the range 0..8.

Polled mode allows Verbose mode too, plus a number of added features including remote Setups programming, forced calibration (including both BG and OBJ), and QT width changing on the fly. Polled mode also lets you examine the current Setups.

Table 4-1 shows the polled-mode ASCII command set. Evoke codes 0..8 return data according to Table 4-2. Error codes are described in Table 4-5.

### 4.4.1 Programming Setups to New Values

The 9701B2 can have its Setups reprogrammed by a host device. This reprogramming mode is initiated by sending the lowercase character 's', which halts sensor operation and places the device into its programming mode; the device then receives program information as pairs of address and data codes. Any combination of the Setups during the course of an 's' session can be remotely programmed this way. There is no time limit during which this has to be performed, so long as the device is powered throughout. The sequence must terminate in the lowercase letter 'w' which writes the new Setups to e$^2$prom and causes the device to sense again.

After the 'w' is sent to the device, and after the e$^2$prom is successfully reprogrammed, the part will transmit back to the host an uppercase 'A' (hex 0x41) as a means of confirmation.

Following the transmission of the initiating 's', two-byte Setup Pairs of codes must be sent:

(1) A Select code, from hex 0x01 (1 decimal) to 0x17 (23 decimal) which corresponds to the keyboard control characters ^a through ^w (control-a ... control-w). 0x01 corresponds to Select Item 0; 0x17 corresponds to Select Item 'U'. See Table 4-6. This acts as an address into the e$^2$prom locations.

(2) a Setting code from ascii '0' through '9' (hex 0x30 ... 0x39).

Each pair will alter the corresponding Select item to be the new Setting code, from 0 through 9.

As many pairs as required may be sent, even to overwrite prior pairs sent in the same session if a mistake is made. NO CR/LF CODES should inadvertently be sent after pair characters, or at any time. CR/LF codes correspond to codes 0x0d and 0x0a, which are valid Select codes during Remote Setups. (CR = Carriage Return, LF = Line Feed; these are often accompanied automatically by many programs when data is sent, and as such should ALWAYS be suppressed in any interaction with the 9701B2).

A typical Remote Setup session might look like (unit already set to Polled Mode):

**s ^a 9 ^i 1 ^d 5 ^s 1 ^a 8 w**
**<pause while unit recalibrates, then...> 1 v**

Note that ^s (control-'s', same as Select item 'J') is often intercepted by terminal programs and may not actually be sent from the host when so desired. There are usually ways around this. 'w' programs the e$^2$prom and recalibrates the sensor before running (unless in Instant Start mode, in which case the sensor just runs again). Note also that the second ^a pair (^a 8) overrides the first one; thus, Detect Threshold is set to '8' (6 counts of threshold level as shown in Table 7-1). After the recalibration, the unit is placed back into Enhanced Verbose mode and then sends a stream of data item '1' (signal - reference), following the 1 v sequence.

Table 4-6 shows the equivalence between the 's' Setups codes and Function Setup Table 7-1.

### 4.4.2 Recalibration after Remote Setups

Remote Setup does not cause the QT9701B2 to recalibrate. This permits alteration of critical parameters without disturbing the sensing function, allowing dynamic alteration of basic operating parameters 'on the fly' without disturbing the data stream or calibration point.

If recalibration is desired after a Remote Setups sequence, for example after altering the device's Burst Length, any of the 'B', 'b', 'O', or 'o' commands can be sent afterwards to induce the desired recalibration.

### 4.4.3 UART Evoke Data in Polled Mode

In polled mode the QT9701B2 will return any data item described for Verbose Mode in Section 4.2. The host device must send an evoke character from ASCII '0' through '8' to cause the device to respond with the corresponding data item (see also Table 4-2). Only one byte is returned after each evoke code, with no terminating CR or CR/LF.

### 4.4.4 Last-Command Evoke

In polled mode, the host can interrogate the device to see if the last command sent was properly received using the character 'l' (Lower case L, ASCII code 0x6c). This is useful to obtain positive feedback that a command was received from the host.

In cases where a sequence of identical commands are issued, such as a string of 'b' commands, a nonfunctional dummy

## TABLE 4-6 - REMOTE SETUP CODES (refer also to Table 7-1)

| Select | Description | ASCII | Hex | | Select | Description | ASCII | Hex |
|---|---|---|---|---|---|---|---|---|
| **0** | Detect Threshold | ^a | 0x01 | | **C** | Max On-Duration | ^m | 0x0D |
| **1** | Hysteresis | ^b | 0x02 | | **D** | Detection Mode | ^n | 0x0E |
| **2** | Reference Offset | ^c | 0x03 | | **E** | Calibration Control | ^o | 0x0F |
| **3** | *unused* | ^d | 0x04 | | **F** | Drift Store, Data Locking | ^p | 0x10 |
| **4** | Width Pots | ^e | 0x05 | | **G** | Serial Modes | ^q | 0x11 |
| **5** | Burst Length | ^f | 0x06 | | **H** | Verbose Data | ^r | 0x12 |
| **6** | Burst Spacing | ^g | 0x07 | | **J** | Polarities | ^s | 0x13 |
| **7** | Randomize | ^h | 0x08 | | **L** | Output Stretch | ^t | 0x14 |
| **8** | Drift Rate | ^i | 0x09 | | **N** | *unused* | ^u | 0x15 |
| **9** | Median Filter | ^j | 0x0A | | **P** | *unused* | ^v | 0x16 |
| **A** | Boxcar Average | ^k | 0x0B | | **U** | Mode / SPI Data Output | ^w | 0x17 |
| **B** | Detect Integrator | ^l | 0x0C | | | | | |

character can be sent to the device (such characters are also mirrored back to the host; See 4.4.7 below) to act as a separator, ensuring that the Last-Command byte returned in fact relates to the immediately prior byte sent to the device, and not a byte sent earlier in the sequence. Any ASCII code not shown in Table 4-1 will work as a separator.

#### 4.4.5 Remote Setup of Serial Mode / Baud Rate

Programming via Remote Setup of [G] is treated as a special case. To facilitate continued communication after a baud rate or serial mode change, the device will only begin the new serial setting after it is reset. This can be accomplished by unpowering the device, or by executing a Reset command 'r' (see below).

**FIGURE 5-1 - SPI OFFSET TIMING TO DAC A**

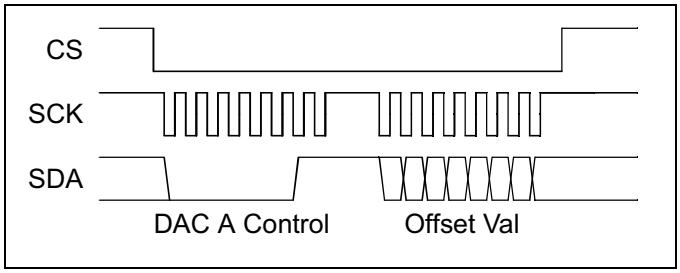
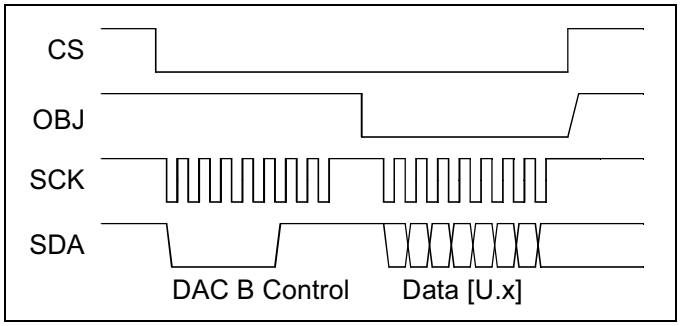



**FIGURE 5-2 - SPI DATA OUT, 8-BIT MODE**




#### 4.4.6 Forced Reset Command

The QT9701B2 can be forcibly reset by sending it the ASCII letter 'r' (lower case R) twice in succession. After the first 'r' is received, the device will mirror back the letter 'r' over the serial port. After it has received the second 'r', it will transmit the letter 'R' (capital R). The two Forced Reset command characters must be sent within a 90ms timespan otherwise the command is canceled. Also, the host should receive the first returned 'r' back before sending the second 'r' to prevent the possibility of a comm overrun in the 9701B2. If full duplex communications are not possible, a 'safety' delay of at least 20ms but less than 90ms can be used to ensure that the second 'r' is properly received.

#### 4.4.7 Unknown Character Mirroring

If the QT9701B2 receives a character it does not recognize as valid, it will transmit that character back to the host immediately. Otherwise the device will be silent or will report back with the selected polled data item.

### 4.5 ERROR CODE REPORTING

The Error code reported by Evoke Code '8', or via [H.8] in either Verbose mode, is shown in Table 4-5. There are 4 possible values with the meanings shown.

Value = 1 indicates a very low signal, possibly due to a short circuit or a failed transfer mosfet or other circuit fault.

Value = 2 indicates excessive signal, more than can be calibrated against; it can also indicate that the mosfet is defective, for example due to heavy internal leakage.

Value = 3 usually indicates a very unstable signal due to substantial amounts of noise or violent signal swings.

These codes are reported after each calibration attempt, except Value 1 which can be detected at any time if a short circuit to ground occurs on the CHG pin. Note that the device will attempt to recalibrate in a manner dependent on Setup [E] if the error was found during a recalibration process; if a short was sensed during normal running, the device takes no further action. Refer to the QT9701B datasheet for further details on [E].

## 5 SPI OPERATION

### 5.1 SPI CLOCKING AND FRAMING

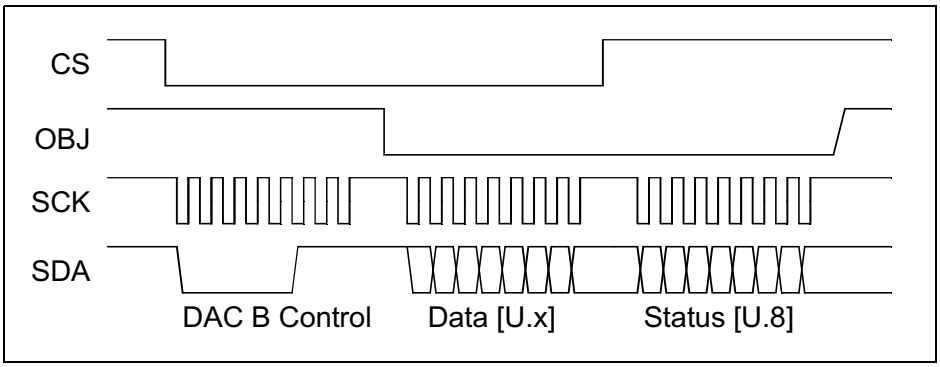
The SPI port uses an 8 or 16 bit clocking scheme; data is clocked out on the falling edge of the SCK signal; the receiving device must be configured to accept data on the rising edge of SCK.. There is only one SPI port that is shared by both the AD7303 and the external world, but the port is framed by two different lines so as to separate the data streams for their respective destinations. The AD7303 contains two independent 8-bit DACs called DAC A and DAC B. DAC A is used to generate the offset voltage for the amplifier chain, and DAC B is used to create a processed 'synthetic' analog output.

The data rate is 5MHz (200ns clocking). SPI framing is provided by two sources:

#### 5.1.1 CS Framing to the Dual DAC

CS (pin 15) provides negative-going frame pulses for shifts of data to parts 'A' and 'B' of an AD7303 dual DAC. Two shifts of data occur during each burst cycle. In both cases the first byte sent is a control byte for the AD7303 used to direct the data byte to its internal part A or B DAC, and is of no particular value to the

**FIGURE 5-3 - SPI DATA OUT, 16-BIT MODE**



external world. In both cases the second byte contains the actual data of interest.

Figure 5-1 shows timing waveforms of the data shifts to part A used to drive the offset node of the external amplifier chain; this transmission occurs just prior to each burst.

Figure 5-2 shows the timing waveforms of data shifts to part B of the AD7303; this is commonly used to supply an analog output which can be one of several different types, depending on Setup [U]. The 'B' transmission occurs just after all internal signal processing has completed, between bursts. The position of this shift will vary depending on the amount of signal processing being performed.

There can also be a third byte transmitted as part of the DAC B shift process if [P.1] is selected, but this third byte is not framed by CS and is thus always ignored by the AD7303 (Figure 5-3).

### 5.1.2 OBJ Framing to an External Device

OBJ (pin 6) frames SPI data to the external world, separate from the DAC framing provided by CS. It encompasses the second or second and third bytes sent as part of the DAC B send to the AD7303. An external receiver of data from the device will thus not receive the DAC control byte portion of the transmission but will receive the relevant data specified by [U.x]. Since the transmission is partly shared with DAC B it is not possible to send separate data to DAC B and an external device.

If [P.0] is selected (8-bit data mode), OBJ frames just the single 8-bit data element chosen by Setups [U.x] (Figure 5-2).

If [P.1] is selected (16-bit data mode, Figure 5-3), OBJ frames first the data element specified by [U.x] and also secondly a byte containing the Status bits described in Table 4-4. Note that only the last two are framed by OBJ; the AD7303 receives data framed by the CS line, namely only the first two bytes of the sequence.

The OBJ line must be pulled high with a resistor, e.g. 2.2K 5% to operate properly, and should not be loaded with external capacitance to ensure a crisp risetime. The dual-use of OBJ does not interfere with the normal functioning of the OBJ input line, but an external contact closure from OBJ to ground may prevent a slave SPI port from receiving the correct data.

## 5.2 SPI DATA MODES [U]

Setup [U.x] specifies the type of data being output by the SPI port in Mode 2. All data returned is unsigned 8 bits, unless mode [P.1] is selected in which case 16 bits are transmitted, the last 8 of which are Status [U.8] (see Section 5.1 and Table 4-4).

**[U.1] Raw** outputs directly acquired, unfiltered data, regardless of any internal filtering that might be enabled.

**[U.2] Synth** outputs filtered (synthetic) data, at the end of all enabled filter stages.

**[U.3] +Synth** returns the positive difference between the current filtered signal and the current reference. If the signal dips below the reference level, the data is truncated to zero.

**[U.4] -Synth** returns the negative difference between the current filtered signal and the current reference. If the signal rises above the reference level, the data is truncated to zero. The value returned is the absolute value of the difference.

**[U.5] |Synth|** returns the absolute value of the difference between the current filtered signal and the current reference, whether above or below the reference level.

**[U.6] Reference** returns the current internal reference value. This may be of value as a form of ultra-slow filtered signal.

**[U.7] DI** returns the value of the Detection Integrator.

**[U.8] Status** returns a status byte composed of bits with meanings as shown in Table 4-4.

Serial SPI data is updated after each burst. Data is output after a burst and after the burst data is fully filtered (if any filtering is enabled).

## TABLE 7-1 - QT9701B2 SETUPS BOLD BOXES DENOTE DEFAULT SETTINGS IF BLANK OR NO EEPROM FOUND

| SELECT | DESCRIPTION | SETTING | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | **0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** |
| 0 | **Detect Threshold, counts** | 62 | 40 | 32 | 25 | 19 | 14 | 11 | **8*** | 6 | 4 |
| 1 | **Hysteresis, % of Threshold** | 50 | **25*** | 12.5 | 0 | | | | | | |
| 2 | **Reference Offset (hex / decimal)** | 0x10 / 16 | 0x20 / 32 | 0x40 / 64 | 0x60 / 96 | **0x70 / 112*** | 0x80 / 128 | 0xA0 / 160 | 0xC0 / 192 | 0xE0 / 224 | 0xF0 / 240 |
| 3 | **unused** | | | | | | | | | | |
| 4 | **Pulse Width - ns** | 200 | 400 | 600 | 800 | **1,000*** | 1,200 | 1,400 | | | |
| 5 | **Burst Length, pulses** | 4 | 8 | 16 | 24 | 32 | 40 | 48 | 56 | **64*** | ‡ |
| 6 | **Burst Spacing** | 200µs | 500µs | 1ms | **2ms*** | 5ms | 10ms | 20ms | 50ms | 100ms | ‡ |
| 7 | **Randomize Bursts, %** | **off*** | 12.5% | 25% | 50% | ‡ | | | | | |
| 8 | **Drift Rate, seconds/bit** | off | 100 | 50 | 20 | 10 | **5** | 2 | 1 | 0.5 | 0.2 |
| 9 | **Median Filter, length** | off | **5*** | 9 | | | | | | | |
| A | **Boxcar Average, length** | off | 2 | 4 | 8 | 16 | **32*** | 64 | ‡ | | |
| B | **Detect Integrator, counts** | off | 1 | 2 | 5 | **10*** | 20 | 50 | 100 | 200 | ‡ |
| C | **Max On-Duration, seconds** | infinite | 100 | 50 | **20*** | 10 | 5 | 2 | 1 | 0.5 | 0.2 |
| D | **Detection Mode** | | | | | | | | | | |
| D.a | Output on positive signals | **X*** | X | X | X | X | X | | | | |
| D.b | Output on negative signals | | | | | X | X | X | X | X | X |
| D.c | Max On-Duration engages on +/- crossing | **+*** | + | +/- | +/- | +/- | +/- | +/- | +/- | - | - |
| D.d | Drift compensation during detect | | X | | X | | X | | X | | X |
| E | **Calibration control** | | | | | | | | | | |
| E.a | output error code if cal error | off | on* | off | on | | | | | | |
| E.b | recal if ref drifts into boundary | on | on* | off | off | | | | | | |
| F | **Drift Store / Data Locking / Motion** | | | | | | | | | | |
| F.a | Drift store interval, minutes between saves | **off*** | off | 1 | 2 | 5 | 10 | 15 | 30 | 60 | motion |
| F.b | Data locking | **off*** | on | on | on | on | on | on | on | on | off |
| G | **Serial Modes / UART Rate** | **Off*** | **9.6P*** | 19.2P | 57.6P | 115P | 9.6V | 9.6VS | 19.2V | 57.6V | 115V |
| H | **Verbose Data** | **synth** | synth-ref | ref | offset | canceltn | DI | from U | status | err code | |
| J | **Polarities** | | | | | | | | | | |
| | OUT pin: Active = | **High*** | Low | High | Low | | | | | | |
| | XFR pin: Drive = | **High*** | High | Low | Low | | | | | | |
| L | **Output Stretch, seconds** | **0** | 0.1 | 0.2 | 0.5 | 1 | 2 | 3 | 5 | 7 | 10 |
| N | **unused** | | | | | | | | | | |
| P | **SPI Format** | **8 bits** | 16 bits | | | | | | | | |
| U | **Mode / SPI Data Output** | **Mode_1*** | Raw | **Synth*** | +Synth | -Synth | \|Synth\| | Ref | DI | Status | |

*** Settings when 'forced defaults' are engaged. Setups G and U are autodetected depending on circuit configuration. Refer to Section 7.1.**

# 7 - SETUP TABLE NOTES

## 7.1 FORCED SETUP

The device can be made to revert to default settings as shown by the outlined boxes in Table 7-1. Forced Setup is accomplished by simultaneously holding the BG and OBJ lines low before and during powerup, and keeping them held low for at least 500ms after power has been applied, then releasing them high. After this, the device will operate normally with the default settings, but may require recalibration using BG and/or OBJ depending on how the Setups have changed.

**Mode 1 defaults:** With an R2R ladder installed, the device will autodetect and select G.0 and U.0 for its Serial and Mode defaults.
**Mode 2 defaults:** Without an R2R ladder installed, the device will autodetect and select G.1 and U.2 for its Serial and Mode defaults.

The Forced Setups feature allows a blank e$^2$prom to be programmed with settings suitable for basic communications over the UART channel in Mode 2, through which additional changes can thereafter be programmed. The serial mode, Polled / 9600 Baud, is also the default mode for QTWinView software.

## 7.2 DEFAULT SETTINGS

If no e$^2$prom is found, the device will use the default Mode 1 parameters shown in Table 7-1 in outline, using G.0 and U.0. Thus, for Mode 2 operation an e$^2$prom must be installed.

If a blank e$^2$prom is found and Forced Setups are not employed to initialize it, the e$^2$prom will be programmed to contain the default Mode 1 settings. If a Mode 2 circuit is used, follow the procedure in Section 7.1 to initialize the e$^2$prom to Mode 2.

## 7.3 TIMING LIMITATIONS

The QT9701B2 does not perform limit checks on the timing compatibility of the Setups. Certain combinations of QT pulsewidths, burst length, filtering, and post-processing require more time to execute than allowable by a chosen Burst Spacing [6]. It is up to the user to prevent these combinations of Setups from being chosen. The following table shows the basic timings required for given burst lengths and pulse widths:

### TABLE 7-2 - BASIC QT BURST TIMINGS

*Table entries shown in microseconds. No filtering or detection options enabled.*

| | | Charge / Transfer Width [4.X] | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | **[4.0] 200ns** | **[4.1] 400ns** | **[4.2] 600ns** | **[4.3] 800ns** | **[4.4] 1000ns** | **[4.5] 1200ns** | **[4.6] 1400ns** |
| **Burst Length [5.X]** | [5.0] 4 | 170 | 171 | 172 | 172 | 173 | 175 | 189 |
| | [5.1] 8 | 178 | 178 | 180 | 179 | 182 | 185 | 201 |
| | [5.2] 16 | 194 | 192 | 196 | 194 | 199 | 206 | 225 |
| | [5.3] 24 | 210 | 207 | 212 | 208 | 217 | 227 | 249 |
| | [5.4] 32 | 226 | 221 | 228 | 222 | 235 | 248 | 273 |
| | [5.6] 40 | 242 | 236 | 244 | 237 | 252 | 268 | 297 |
| | [5.7] 48 | 258 | 250 | 260 | 251 | 270 | 289 | 321 |
| | [5.8] 56 | 274 | 264 | 276 | 266 | 288 | 310 | 345 |
| | [5.9] 64 | 290 | 279 | 292 | 280 | 305 | 331 | 369 |

If a selected combination of [4] and [5] results in a table entry greater than the selected Burst Spacing [6], then the device will fall out of specification as to its burst timing. For example, if the Burst Spacing is set to [6.0], (200us), and the Width is set to [4.3] (800ns), and the Burst Length is set to [5.4], the total timing required will be 222us, which is greater than the chosen Burst Spacing. However, the device will function fine if the Burst Spacing is set to 500us instead of 200us. Additional features that are enabled add time to the basic burst cycle timing as follows:

### TABLE 7-3 - BURST TIMING ADDERS

*Add these timings to the basic timings of Table 7-2 if enabled.*

| **This Setup...** | **...if set to** | **...yields additional required time** |
|---|---|---|
| [9] Median Filter | 5 | 61us |
| | 9 | 122us |
| [A] Boxcar Averager | 1..6 | 21us |
| [B] Detect Integrator | 1..8 | 16us |

At a burst spacing of 500us, all functions can be enabled at once except at burst lengths above 48 with a QT transfer time of 1.4us. Burst Randomization [7], if enabled, also requires additional inter-burst spacing time. Randomization alters the spacing between bursts by a psuedo-random amount that is more or less than the nominal setting of Burst Spacing [6]. In effect, randomization requires an effective adder for inter-burst timing. The effective adder should be added to the timings of Table 7-2.

### TABLE 7-4 - BURST RANDOMIZATION TIMING ADDERS

*Add these timings to the basic timings of Table 7-2 if enabled.*

| Randomize [7] | Burst Spacing [6] 200us | 500us | 1ms | 2ms | 5ms | 10ms | 20ms | 50ms | 100ms |
|---|---|---|---|---|---|---|---|---|---|
| **off** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| **12.5%** | {1} | 63us | {2} | {2} | {2} | {2} | {2} | {2} | {2} |
| **25%** | {1} | 125us | {2} | {2} | {2} | {2} | {2} | {2} | {2} |
| **50%** | {1} | 250us | 500us | {2} | {2} | {2} | {2} | {2} | {2} |

{1} Do not use these settings
{2} Randomization can be freely used on these settings regardless of other Setups

# 8 - FUNCTION DESCRIPTIONS

The following describes processing function enhancements and changes over and above the QT9701B part.

**[0] DETECT THRESHOLD**

This is one of 4 items that can affect sensitivity (others are Burst Length, amplifier gain, and under certain conditions Drift Rate). Threshold establishes the 'trip point' above (or below, in the case of negative thresholds) which a detection is determined. During calibration the unit establishes a reference level; deviations from this reference are compared against a level based on the reference plus (and/or minus) Detect Threshold. Setting 9 represents the highest sensitivity since only 4 counts of signal deviation are then required to trip. If negative signal detection is in effect (see Detection Mode), the negative threshold is the mirror image of the positive one (e.g. a setting of '6', value '11', can create a positive threshold at +11 and another at -11 from the reference).

In OBJ mode, the Detect Threshold value may be used instead to create hysteresis, and is not used for threshold purposes; In OBJ mode, the threshold is determined at the time of the button push and is an arbitrary value corresponding to the current signal level at the time OBJ is evoked. See OBJ Mode (Section 3.15.3) for details.

**[1] HYSTERESIS**

The sensor has several hysteresis options. In conventional signal detection mode, a hysteresis of 50, 25, or 12.5% of threshold value can be selected, which applies to positive and negative thresholds alike (depending on which are active: see [D], Detection Mode). Thus if Hysteresis is set to 25%, a detection at a signal deviation of +8 will be released only when the signal falls below +6. Hysteresis is only applied after the Detection Integrator has concluded there is a valid detection. If the Detection Integrator function is switched off, no detection will be performed and the Hysteresis setting becomes irrelevant.

In OBJ mode the Hysteresis setting is ignored, unless set to '3' (0 hysteresis); after the OBJ button push the hysteresis is taken from the table value of Detect Threshold, and the signal threshold is obtained from the recording of the actual signal level at that time. See OBJ Mode (Section 3.15.3) for details.

**[2] REFERENCE OFFSET**

Reference Offset determines where the sensor establishes a calibration point. The offset numbers are given in Table 7-1 both as hexadecimal ("0x20") and decimal ("32"). Normally, centering the reference at mid-scale of the 8-bit (0 - 255) ADC range is a reasonable location to calibrate, as this will allow an equal amount of headroom both above and below the reference to accommodate long term drift and signal swings. However, in many situations signal and/or drift swings are largely unilateral, e.g. positive, and so maximum headroom in the positive direction is desired. In this case, Reference Offset might be set to a low number, like 0x10 or 0x20. Conversely, largely negative excursions would indicate a need for a high value of Offset, for example when 'missing mass' is being detected (example: detecting gas bubbles or voids in a fluid within a tube or pipe, theft detection, or as a web break detector).

In OBJ mode the reference offset will be forced to 0x70 (setting 4) when the OBJ button is pushed.

**[4] PULSE WIDTH**

These settings are digitally synthesized and can be selected as shown. Pulse Width applies equally to both the charge and transfer times. Alternate pulse widths (for example, below 200ns) can be generated with external timing circuitry (Section 3.1.3). When using short pulse widths, be careful of inductive signal lead and ground ringing effects which can cause anomalous behavior.

### [5] BURST LENGTH

Affects the number of QT cycles within a burst (Section 1.1). Bursts occur at a rate determined by Burst Spacing. Burst length can be set from 4 to 64 pulses per burst; the larger burst length is the more sensitive the sensor becomes, in direct proportion, but the less its ability to compensate for and suppress background capacitance loading. Higher Burst Lengths produce more intrinsic averaging for a given desired sensitivity level, and thus can help suppress electrical noise effects, provided the Threshold value is desensitized proportionately to compensate for the increased gain.

At 200µs and 500µs burst spacings this setting may need to be reduced; see Section 7.3. No conflict resolution is performed internally, so erroneous operation in the form of timing errors will occur if the limitations described in Section 7.3 are violated.

### [6] BURST SPACING

Affects the timing between successive bursts. Longer time equates to lower sample rates, and hence slower response time. At short spacings (200µs and 500µs) the burst length may need to be reduced; see Tables 7-2 through 7-4 in Setup Notes, and comments in [5] above. Longer burst spacings are useful in the presence of strong alternating electric fields, for example power line interference, especially in conjunction with Median filtering [9] and Averaging [A] in order to suppress the interference. Longer burst spacings also reduce average emitted RFI and can help with emissions issues, especially when large free-space electrodes are used.

Burst Spacing can also be randomized to skip around interfering noise impulses. See [7] below for more information on this feature.

### [7] RANDOMIZE

Sets the degree to which the Burst Spacing is randomized. Percentages shown in the table are percents of burst spacing time; thus, randomization of 25% at a burst spacing of 1ms will cause bursts to be spaced anywhere from 750µs to 1.25ms apart. Bursts are randomized using a psuedo-random number generator. Randomness helps to spectrally spread RF emissions, and reduces the chance of false detections due to correlated electrical noise. Randomization literally 'skips around' repetitive noise and greatly reduces the odds that a long string of acquisition bursts will sample repeatedly on repetitive noise pulses. The use of Median filtering [9] and Averaging [A] will act to suppress the effects of any remaining corrupted bursts.

Note the limitations on Randomize described in Section 7.3; randomization is not possible at all combinations of burst spacing, burst length, and pulse width.

### [8] DRIFT RATE

Drift Rate, or perhaps more accurately Drift Compensation Rate, sets the rate at which the sensor's baseline reference point can track slow ambient changes (drift) in signal level. In many sensing environments the signal will fluctuate due to varying moisture levels, temperature, dirt accumulation, or other uncontrollable variables. Such fluctuations can ordinarily cause the sensor to lose its calibration point, resulting in the sensor appearing to gain or lose sensitivity, or cause false detections. The drift compensation process operates by permitting the reference level to increment or decrement by 1 signal count every 'X' seconds in the direction of the signal deviation; 'X' is the setting of Drift Rate shown in Table 7-1.

Drift Rate should be set to as slow (leftwards in Table 7-1) a rate as possible; fast drift compensation may cause the sensor to track real objects and thus appear to lose sensitivity.

As a rule, drift compensation should occur only when a detection is not being made, i.e. when the OUT line is inactive; drift compensation should occur only when not detecting, otherwise the baseline reference will accumulate an error which can cause problems with future object detections. However, Detection Mode [D] can also be set to permit drift compensation during detections, so the user can if required break this 'rule'.

Drift compensation is not permitted at all in OBJ mode and will be disabled when the OBJ button is pushed; see Section 3.15.3, OBJ Mode Details for further information.

If the reference level drifts towards the boundary of the 8-bit signal window so that [reference + threshold] exceeds the valid signal range, one of two things can happen:

1. Drift ceases, if "*recalibrate if reference drifts into boundary*" (see [E.b] ) is off.
2. The unit performs a recalibration to reset the signal "window", if "*recalibrate if reference drifts into boundary*" [E.b] is on. This automatic recalibration will attempt to reset the signal's reference point so that it conforms to the setting of [2], Reference Offset.

**Analog Output and Drift Compensation:** Since the pure analog output (if implemented) is split from the sensor prior to signal processing, drift compensation cannot be made to apply to it. However the synthesized analog output can be made to drift compensate if set to any Delta mode (+synth, -synth, |synth| ).

## [9] MEDIAN FILTER

This filter strongly reduces electrical impulse noise errors. A median filter selects the median, or center value of an odd group of sample data. The QT9701B2's median filter uses either 5 or 9 pipelined signal samples. Because it takes the center value, impulse induced spurious signals are eliminated from further processing within the signal path, no matter how erroneous. If enabled, this filter is the first digital filter in the signal path.

Median filtering is best explained by showing its effects on a data stream. Given the data set:

105, 101, 93, 99, 223 (where the 'real' signal = 100)

The average if the above set is (105+101+93+99+223) / 5 = 124.2. The median is the center value of the set, or 101, which is a much more accurate representation of the 'real' signal. Because they can be very effective on short data sets and act as hard-limiters, median filters are more efficient than linear filters.

The median filter is based on a pipeline of data length 5 or 9; after every burst new data is shifted in, the oldest is discarded, and the median of the resulting pipe of data is taken; this ensures the fastest update rate possible, i.e. one update after every QT burst. Section 7.3 describes timing limitations on Median filtering when used with various combinations of pulse width, burst length, and burst spacing.

## [A] BOXCAR AVERAGING

This is a simple linear digital FIR (finite impulse response) filter which follows the median filter. It performs a boxcar average of length 'n'. In general for every doubling of length, noise is suppressed by 3dB or by 0.71 in amplitude. Thus a boxcar averager of length 16 shows a noise improvement of about 12dB or a reduction to 0.25 in amplitude over no filtering. Averaging's downside is a slowdown in response time, which is more evident with long (slow) Burst Spacings. Averaging compounds with the intrinsic sample averaging which occurs naturally in the sample process, as set by Burst Length. Averaging can be used alone or following the Median Filter, in which case it acts to clean up residual low level noise.

The boxcar averager is based on a pipeline of length 'n' (where 'n' is from 2 to 64); after every burst new data is shifted in, the oldest is discarded, and the average of the resulting pipe of data is taken; this ensures the fastest update rate possible, i.e. an one result after every QT burst.

## [B] DETECTION INTEGRATOR

This post-detection filter acts to integrate or count the duration of a detection event prior to an actual output. This allows the sensor to suppress large transient events caused by real objects, as well as noise induced transients; thus, it can also be used to supplement the actions of the Median and Boxcar filters.

The DI is implemented as an up/down counter controlled by the threshold comparator. If a detection is in progress, the DI will count up once after every burst in which an event has been detected. When no detection event is in progress, the DI counts down again. If the DI reaches the prescribed count level as defined in the Setups, a 'real' detection is finally assumed and the Out line is activated.

*Important Note:* If the DI is set to zero, it is disabled and Out cannot turn on, and [C], [D], and [L] have no effect. If set to 1 count, Out activation occurs after a single threshold detection. The DI can also be seen as a continuous-time 'majority vote' filter, since over a period of time there needs to be a greater than 50% detection 'hit' rate for the DI to reach its count limit.

Turning [B] off is useful to suppress detections for test purposes, or if an analog output is all that is required of the sensor.

## [C] MAX ON-DURATION

After an interval of continuous detection, the device can be made to perform an automatic recalibration. The interval is programmable in seconds, according to [C].

There are two recalibration methods which can be selected via Setup [F]:

1) Default - the sensor performs a full recalibration involving both coarse and fine offsets;

2) Motion - the sensor keeps coarse and fine offsets the same, and merely resets the reference level to whatever the current signal strength happens to be at that moment.

Option 2 is selected by setting [F] to 9 ('Motion'). All other settings of [F] are slower but safer from the standpoint of establishing a true reference level; although faster to respond, 'Motion' [F.9] can lock up the Out line for the duration that the signal strength falls outside the ADC's 8 bit signal range.

Detection Mode [D] can be set to permit Max On-Duration to start timing towards recalibration even if Out is inactive. This can occur if a threshold level is crossed even if that threshold level is set to not activate Out. Example: if [D] is set to [D.2], an active Out will occur if the signal exceeds the positive threshold; however, [D.2] also establishes a negative threshold (symmetrically spaced across the Reference level from the positive one), and signal excursions below the negative threshold will not, in the case of [D.2], generate an active Out, however such excursions <u>will</u> cause Max On-Duration to start to run. This negative threshold appears to act as a 'phantom threshold', and when the Max On-Duration counter times out, a recalibration will be performed - even though Out has been inactive the entire time.

'Infinite' setting disables Max On-Duration, and no timeout will occur.

The duration counter of [C] is reset to zero any time a detection ceases, or if the signal polarity changes (crosses from + to - or vice versa even if a detection appears to be continuous, for example in a 'window' detection threshold mode, e.g. [D.4] ).

In OBJ mode Max On-Duration is effectively switched to infinite; the actual setting of [C] is ignored.

Max On-Duration is fully operable in BG/OBJ mode.

If [B], the Detect Integrator, is set to 'off', [C] is ignored; also, if [B] is off, drift compensation will occur continuously at the rate specified by [8].

## [D] DETECTION MODE

Defines what constitutes a detection, and determines what happens to some other functions during a detection. [D] can allow the detection of signals that are increasing and/or decreasing; it can also allow Drift Compensation [8] to occur during a detection event or not, and can permit the Max On-Duration timer [C] to run even if the Out pin is inactive but a 'hidden' threshold level has been crossed.

In particular note the interaction with Drift [8] and Max On-Duration [C] functions; see also the explanations of these interactions in notes for these functions, above.

***[D.a]: Output on positive signals -*** If [D.a] is set to a setting with an 'X' in the box, the sensor will generate an Out activation if the filtered signal rises above the upper threshold level, and [B] is set to [B.1] or higher.

***[D.b]: Output on negative signals -*** If [D.b] is set to a setting with an 'X' in the box, the sensor will generate an Out activation if the filtered signal falls below the lower threshold level, and [B] is set to [B.1] or higher. Setting to [D.4] or [D.5] will create a detection 'window' that will activate Out if the signal deviates enough from the reference level in either the + or - directions.

***[D.c]: Max On-Duration engages on +/- signal crossing -*** See [C] for further information on Max On-Duration. Boxes denoted by (+) will cause the Max On-Duration timer to count towards a timeout if the signal rises above the positive threshold level. Boxes denoted by (-) will cause the Max On-Duration timer to count towards a timeout if the signal falls below the negative threshold level. The (+) or (-) threshold levels do not necessarily need to generate an activation of Out, and can instead be 'phantom' threshold(s) whose only purpose is to trigger the [C] timer.

***[D.d]: Drift compensation during detect -*** An 'X' in the selected box will cause the drift compensation mechanism of [8] to operate even if a detection is in process. A detection is defined as a crossing of the (+) or (-) thresholds, as enabled in [D.c], (*not* [D.a] or [D.b]) provided also that the Detect Integrator {B] is enabled (set to at least [B.1]). Conversely, if an 'X' is not present in the selected box, Drift Compensation will be disabled during a detection (usually the most desirable mode).

[D.0] is the most common mode associated with prox sensors.

[D.4] and [D.5] are useful for creating a 'prox trap' where an object that is in the sense field when the unit calibrates will create a detection no matter whether it is moved closer or further away. A demonstration of this is to set up the sense electrode with an object (like your hand) close by, then let the device calibrate on it via the BG pin. Any movement towards or away from the electrode will cause a detection. The width of the detection window is governed by the sensor's overall gain (see Burst Length [5]) and the Detect Threshold setting [0]). This type of detection will work in both the BG or BG/OBJ modes, but not OBJ mode.

Note that 'hidden' detections can be created that will make the Max On-Duration counter run towards a Max On-Duration recalibration timeout, without generating an actual activation of the Out pin. This is useful in clearing a "stuck sensor" condition quickly, for example if a stationary 'background' object near the electrode is removed, creating a large, fast, and undesirable negative signal swing. If set to [D.2] and the device is in BG or BG/OBJ mode, this negative swing can be made to trigger a full recalibration after the Max On-Duration period has timed out, without causing an actual Out activation.

**In OBJ mode:** Detection Modes other than [D.0] or [D.8] are ignored; the closest setting, either [D.0] or [D.8], is used instead.

## [E] CALIBRATION CONTROL

There are two options under Calibration Control:

***[E.a]: output error code if calibration error -*** This controls whether the STAT line will output an error code if during a calibration the sensor detects an error. Since this 'Morse code' takes time to output and slows up the QT9701B2's ability to automatically try to recalibrate, it may be desirable to disable this.

***[E.b]: recalibrate if reference drifts into boundary -*** Controls what happens when sensor drift compensation (see [8]) moves the reference level enough so that it runs into the edge of the allowable signal range. If this happens, it may be desirable to recalibrate the sensor completely to achieve a better centering of the signals within the 8-bit signal range. Turning this 'on' allows this form of recalibration.

The allowable reference range is that required to accommodate the reference level plus the threshold level(s), (+) and (-), within the 8-bit ADC range. For example, if the threshold is set to 14 counts, and positive detection is enabled via [D.c], then the signal space is limited on the positive side to:

255 - 14 - 1 = 240

The '-1' is required to allow the signal to exceed the threshold by one count for detection purposes.

## [F] DRIFT STORE / DATA LOCKING / MOTION MODE

[F] controls three things:

1. Whether the sensor will store calibration data in e$^2$prom (if installed) for reuse on subsequent power-ups, thus preventing the need for another recalibration;
2. Whether the sensor will also store the reference drift data if Drift Rate is enabled;
3. Whether the sensor processes in 'motion' mode, whereby recalibration occurs very quickly but does not involve altering the charge cancellation amount (via Cz's) or the DAC offset value.

***[F.a] = 2...8: Drift store interval -*** If [F.a] is set in the range 2...8, reference drift data will be saved to the e$^2$prom at the intervals shown (in minutes). Note that [F.a] is irrelevant in OBJ mode or if Drift Rate [8] is off. OBJ does not make use of a reference level, and so there is nothing to store. If set to Motion ([F.a] = 9) no store to e$^2$prom is made since Motion mode is transient in nature.

***[F.a] = 9: Motion mode -*** Motion mode will recalibrate very quickly, in a single burst interval, after a detection interval defined by Max On-Duration [C] expires. No storage of cal data or drift compensation information occurs if motion mode is enabled. Motion mode recalibration only occurs within the boundaries of the current signal window as defined by the Coarse and Offset parameters, unless [E.b] is set 'On', in which case a full recalibration occurs. If [E.b] is Off, the Out line will go active for the duration of the signal excursion if Setup [D] permits it.

***[F.b]: Data Locking -*** [F.b] is useful in all modes except 'motion' mode. [F.b] stores the calibration data into e$^2$prom every time there is a full calibration. If [F.a] is enabled from 2...8, the calibration data from [F.b] will be incrementally updated into the e$^2$prom at the indicated intervals.

## [G] SERIAL MODES

9 settings of baud rate and communications mode have been added. The first four settings govern the 'Polled' mode of operation; the last five govern 'Verbose' operation. Polled mode requires that the host send an initiating character to the QT9701B2 to evoke a response. Verbose mode allows the device to transmit a continuous stream of data without interruption. See Section 4 for complete details.

Setting [G.6] allows a special slow-mode of Verbose operation, to allow compatibility with slow host devices unable to accept a fast, continuous stream of verbose data. The data rate in this special 9600VS mode is 100ms spacing between transmits at 9600 baud.

All data is sent as 8 bits, one stop, no parity.

## [H] VERBOSE DATA

The [H] Setup permits the selection of one of 9 different data sources from within the 9701B2, for transmission in either of the normal or enhanced 'Verbose' serial modes. The data types are:

| | |
|---|---|
| **Synth** | Outputs filtered (synthetic) data, at the end of all enabled filter stages. It is an unsigned 8-bit signal value. |
| **Synth - Ref** | Returns the difference between the filtered signal and the current reference. The data is 2's complement binary: If the signal dips below the reference level, the data becomes negative. |
| **Ref** | Returns the current signal reference level. |
| **Offset** | Returns the current DAC offset value being fed to the amplifier chain (Out_A of the AD7303). |
| **Cancellation** | Returns the current charge cancellation value, from 0 to 4, representing the number of Cz capacitors being used to provide charge cancellation. |
| **DI** | Returns the current value of the Detect Integrator (see notes related to [B] in the QT9701B data sheet). |
| **From U** | Returns the value specified by the current setting of Select [U], thus effectively expanding the number of available data options. |
| **Status** | Returns the current Status Byte according to Table 4-3. Note that the Status Byte of [U.8] is not the same as this. |
| **Err Code** | Returns the current error code (see Section 4.5). |

**[J] POLARITIES**

This item controls the polarities of both the OUT pin and the XFR pin; all four possible combinations are possible. Inverted polarity of the XFR pin is useful when driving bus-switch type mosfets, which have internal charge-injection compensating mechanisms built in (example: Quality Semi QS3125 and similar devices from TI and Pericom).

**[L] OUTPUT STRETCH**

The Out pin can be made to 'stretch' when active longer than normal using [L]. After a signal detection ceases, the output can be prolonged by the number of seconds indicated in Table 7-1. Setting to zero prevents stretch entirely and lets the output behave normally. Note also that settings of Detection Integrator [B] can also make outputs appear to stretch, but [B] also causes a delay in the *onset* of output activation.

'Stretch' has no effect on activations made due to a detected short circuit on the CHG pin.

**[P] SPI FORMAT**

Controls the length of the SPI data transmission to an external device, as framed by the OBJ line. When set to [P.0] the data sent is a single 8-bit byte containing the item selected by [U].

When set to [P.1] the data sent is two 8-bit bytes, the first of which is the data selected by [U], the second being the Status byte noted in Table 4-4. It is possible to send the Status byte twice in the same transmission by setting [P.1] and [U.8], although there is no particular reason to do this. If [P.1] is selected, the OBJ line will frame both bytes together with a single uninterrupted logic-low frame pulse, thus creating a unitary 16-bit transmission.

**[U] SPI Data Output**

If this Setup is set to [U.1] or higher, the device is forced into Mode 2 operation which includes all serial port functions (SPI and UART). Otherwise, the device defaults to Mode 1, and behaves identically in-circuit as a QT9701B part. [U.1] and above specify the type of data being output over the SPI port that is framed by the OBJ line (and by CS, which is fed normally to an Analog Devices AD7303).

All data returned is unsigned positive-going data. Refer to Table 7-1.

**Raw** will output directly acquired, unfiltered data, regardless of any internal filtering enabled.

**Synth** will output filtered synthetic data, at the end of both filter stages if both are enabled. The data output in 'Synth' is simply the straight 8-bit signal value.

**+Synth** returns the positive difference between the current filtered signal and the current reference. if the signal dips below the reference level, the signal is truncated at zero.

**-Synth** returns the negative difference between the current filtered signal and the current reference. if the signal rises above the reference level, the signal is truncated at zero. The value returned is the absolute value of the difference.

**|Synth|** returns the absolute value of the difference between the current filtered signal and the current reference.

**Reference** returns the current internal reference value. This may be of use as a form of ultra-slow filtered synthetic data.

**DI** returns the value of the Detection Integrator.

**Status** returns a status byte composed of bits with meanings as follows:

Bit 0...1 (lowest 2 bits) - Calibration error code:
- 00 = no error
- 01 = no detectable signal (may be a shorted electrode)
- 10 = saturated signal, cannot calibrate (too much Cx)
- 11 = unstable signal, cannot calibrate (Cx varying too much over time, or interference, or a circuit fault)

Bit 2 - lower detect threshold;
if 1, signal has dropped through the lower threshold

Bit 3 - upper detect threshold;
if 1, signal has risen above the upper threshold

Bit 4 - OUT status - if 1, the OUT pin is active (regardless of active high / low setup in [J] - if [J] is set to active low, Bit 4 will still go high when active)

Bit 5 - Calibration - if 1, unit is busy calibrating

Bit 6 - OBJ line has been asserted low;
not responsive to the UART commands 'o' or 'O'

Bit 7 - BG line has been asserted low;
not responsive to the UART command 's' or 'B'

# 9 - DRIFT COMPENSATION & DETECTION

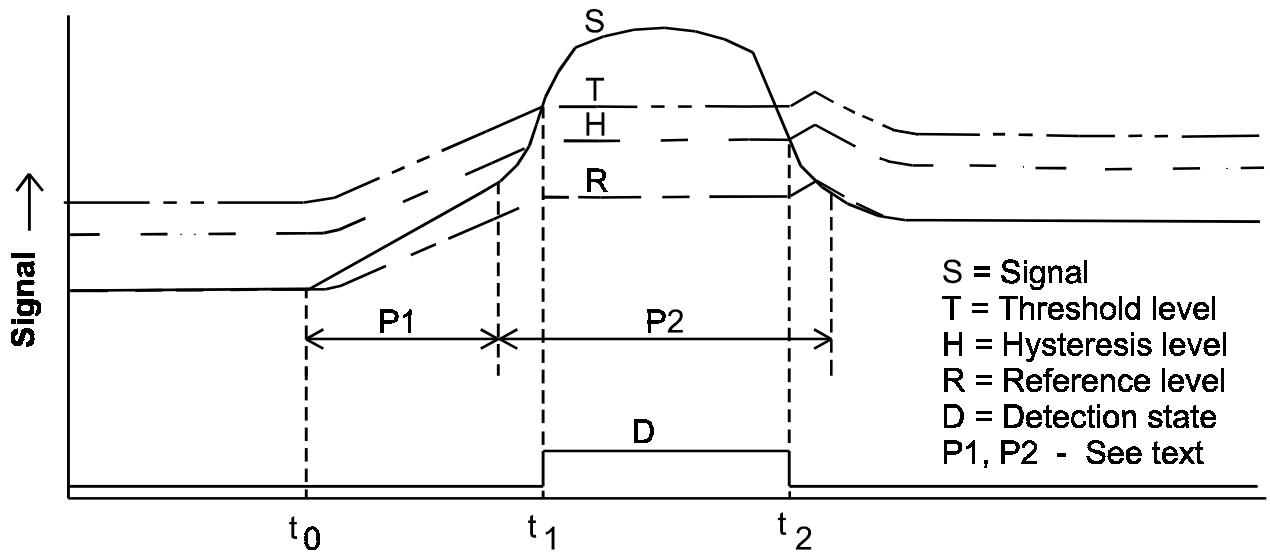
Figure 9-1 shows how the reference level, thresholds and hysteresis interact with the drift compensation mechanism. Prior to time $t_0$, the sensor is shown as being quiescent; Reference and Signal have the same value. During interval $P_1$ the signal begins to rise slowly, perhaps due to environmental factors or a slow moving inbound object; the reference level 'drift compensates' upwards at the selected rate limit to try and track the slow Signal changes. Because threshold 'T' is tied to 'R', no detection occurs yet since 'T' also rises. Then, during interval $P_2$ an object enters the field rapidly and causes the signal to rise much faster than can be compensated for by 'drift compensation'; at time $t_1$ a detection event 'D' occurs.

'S' falls as the object recedes, and the signal finally drops through the hysteresis level 'H' at time $t_2$, causing 'D' to cease. The reference level once again tries to keep up with changes in the signal, even spiking upwards briefly while the signal is still higher than the 'real' background level.

Negative signal swings and negative threshold work in exactly the same manner and are simply the mirror image of the diagram shown.

QTWinView software is an excellent tool for observing the interactions of these parameters with signals in real time.

**Figure 9-1 Drift Compensation and Threshold Detection**



# 10 - E97S BOARD

Figures 10-1 through 10-4 show the artwork and schematic diagram of the E97S eval board which incorporates the QT9701B2. This board is designed to permit all forms of output, including OUT, STAT, UART, SPI, and (with additional user-supplied parts) raw sampled analog, and is a convenient reference design that may be copied freely.

**FIGURE 10-1 E97S SILK LAYER**

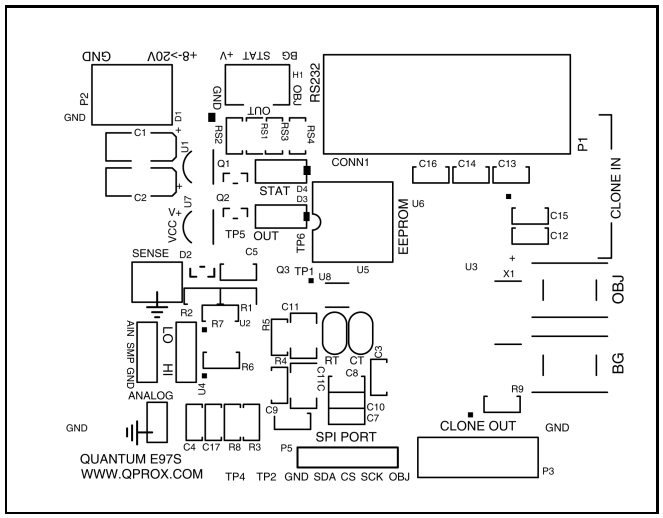
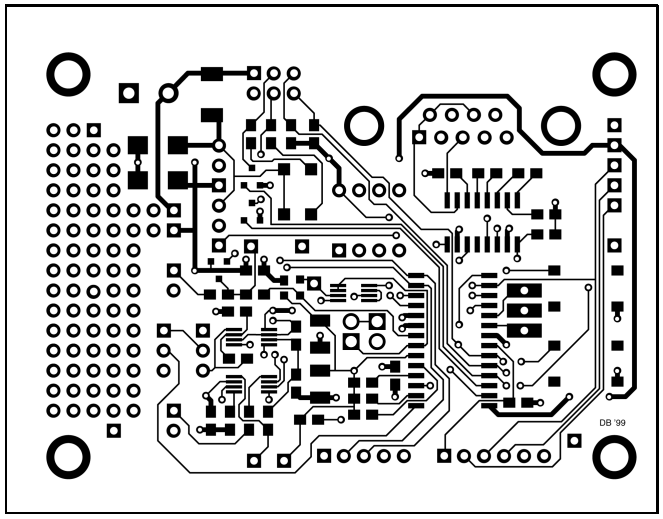


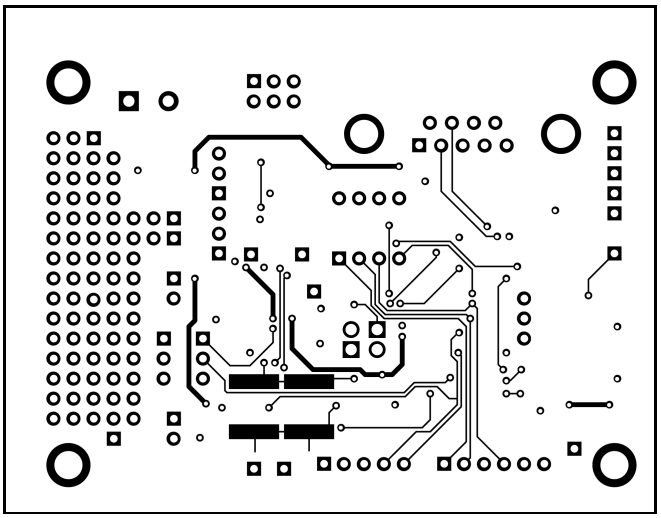

**FIGURE 10-2 E97S TOP LAYER**




The U8 circuit provides a simple means of creating transfer times of less than 200ns in hardware. Rt and Ct can be used to create narrow transfer switching gate pulses on Q3, provided that the Width setup is set to 400ns or less to allow enough time between pulses for the RC network to restabilize.

This circuit can be disabled if not wanted by simply jumpering CT to ground and removing RT; doing so will create a direct logical drive connection from XFR to the transfer switch. In an OEM product, if the circuit is not desired it should be eliminated and replaced with a direct connection from XFR to the gate of Q3, with

**FIGURE 10-3 E97S BOTTOM LAYER**



a 47pF NPO capacitor connected from this same line to ground.

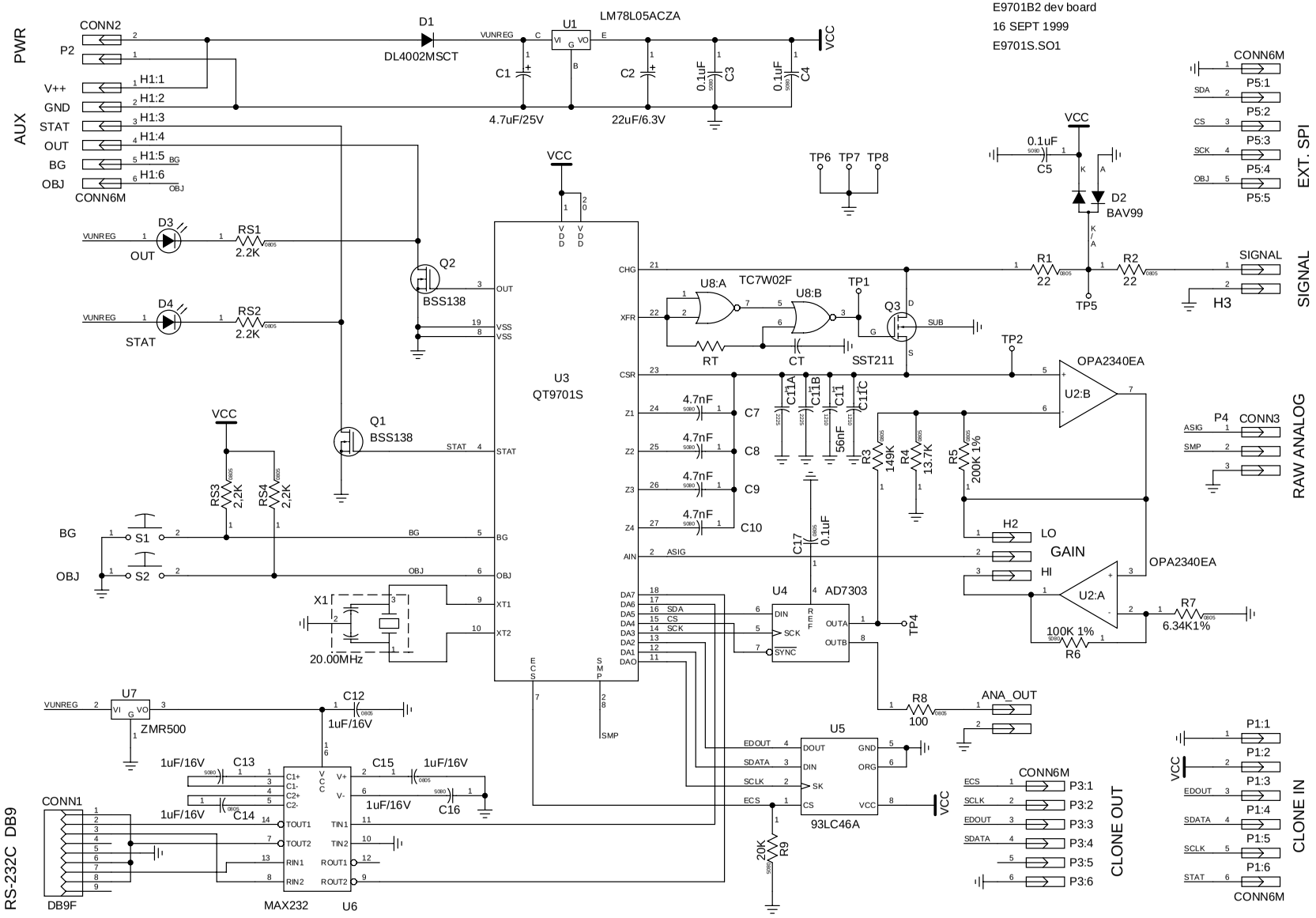
The multiple C11 capacitors are positions provided on the pcb, both top and rear, to accommodate numerous types and sizes of SMT capacitors. Capacitors C7 through C10 are ceramic NPO types.

Amp gain can be jumper-selected via H2, which provides a factor of 16 step change in gain.

Also provided are port connectors for cloning in (P1) and out (P3). Cloning is described in more detail in Section 3.4.

GWK format artwork for this board can be found on Quantum's web site at http://www.qprox.com and may be freely used to create customized artwork.

# FIGURE 10-4 E97S BOARD SCHEMATIC



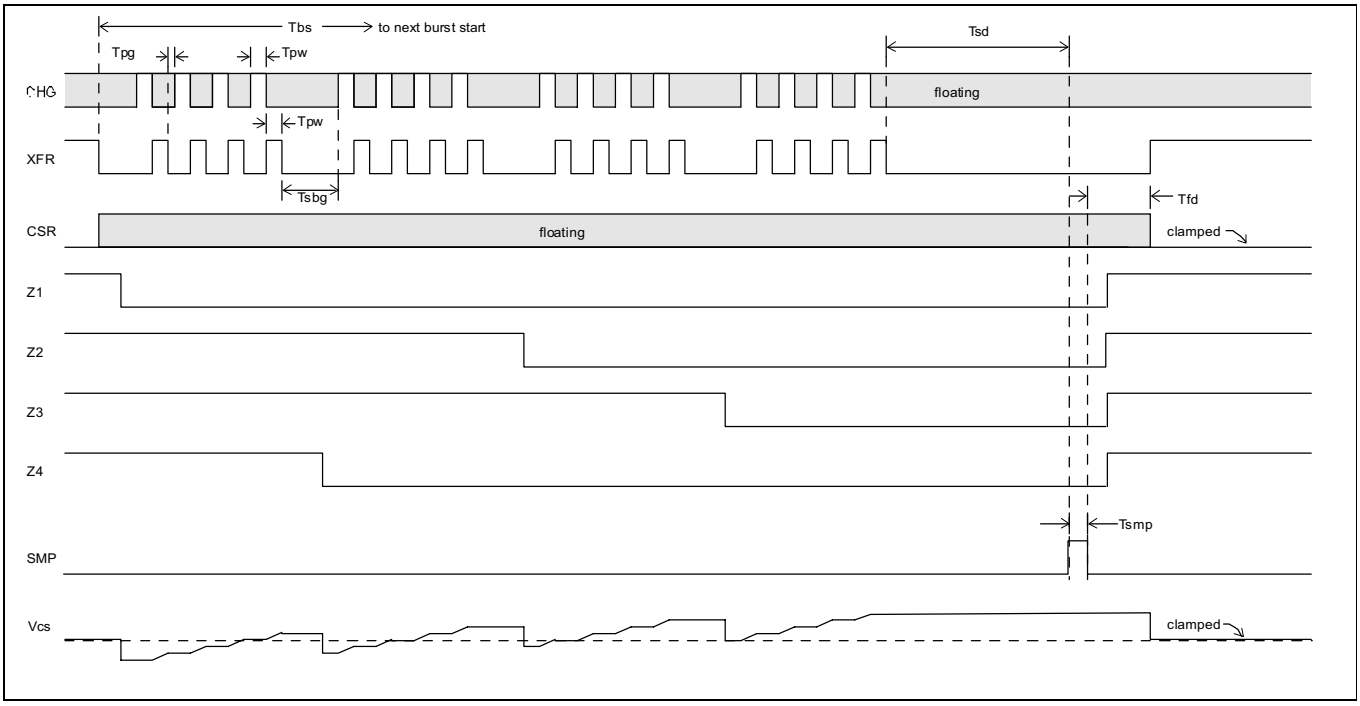
## 11.1 ABSOLUTE MAXIMUM SPECIFICATIONS

Operating temp ..... as designated by suffix
Storage temp ..... -55°C to +125°C
$V_{DD}$ ..... -0.5 to +6.5 V
Max continuous pin current, any control or drive pin ..... ±25mA
Short circuit duration to ground, CHG line ..... infinite
Short circuit duration to $V_{DD}$, CHG line ..... infinite
Short circuit duration to ground, any other pin ..... 5 secs
Voltage forced onto any control or drive pin ..... -0.3V to (Vdd + 0.3) Volts

## 11.2 RECOMMENDED OPERATING CONDITIONS

$V_{DD}$ ..... 5.0 ±0.2V
Supply ripple+noise ..... 5mV p-p
Load capacitance ..... 0 to 1,000pF
R2R dac value (Mode 1) ..... 100K ohms
Cz values ..... 7% of (Cs + Cz), max, each Cz, if used
Cs value ..... 1nF to 100nF

## FIGURE 11-1 TIMING DIAGRAM - MODE 2 **See note 2**



## TABLE 11-1 AC SPECIFICATIONS Mode 2, Fosc = 20MHz, Vdd = 5.0, Ta = recommended operating range

| Parameter | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| FOSC | Oscillator frequency | 0 | | 20 | MHz | Crystal, resonator, or external source |
| FDUTY | Oscillator duty cycle | 45 | | 55 | % | |
| TPW | Pulse width | 200 | | 1,400 | ns | Selectable; see Table 7-1 |
| TBS | Burst spacing interval | 0.2 | | 100 | ms | Selectable; see Table 7-1 |
| TPG | Pulse gap | 200 | | 1,600 | ns | TPW dependent; see Table 11-4 |
| TSBG | Sub-burst interpulse gap | 4.6 | | 6.6 | µs | TPW dependent; see Table 11-4 |
| TSD | Burst end to sample delay | 30 | | 30.6 | µs | |
| TSMP | Sample pulse width | | 4.2 | | µs | |
| TZH | Zx hold time | | 16.8 | | µs | |
| TFD | CSR/XFR float delay | | 16.8 | | µs | |
| BR | Burst randomization | | | ± 50 | % | % of TBS, burst spacing interval |
| TEMIN | BG/OBJ evoke duration | TBS | | 1.4 | s | Normal recalibration function only |
| TEFORCE | BG/OBJ mode change | 1.6 | | | s | Forced mode change |

**Note 1:** There are always 4 sub-bursts within a burst; as burst length increases, the number of QT cycles in all sub-bursts increases equally.

**Note 2:** Charge cancellation lines Z1..Z4 are sequenced as shown when all four are required. When only one is required, only Z1 transitions; when 2 are required, Z1 and Z2 transition; when 3 are required, Z1, Z2, and Z3 transition. Non-transitioning Zx lines always remain high. Points of transition for each Zx line are fixed as shown in Figure 11-1.

## TABLE 11-4 BURST TIMING VS. Tpw

| Parameter | TPW | | | | | | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | 200ns | 400ns | 600ns | 800ns | 1000ns | 1200ns | 1400ns | | |
| TPG | 1600 | 1000 | 800 | 200 | 200 | 200 | 200 | ns | |
| TSBG | 5.6 | 5.4 | 5.2 | 5.0 | 5.0 | 5.0 | 4.6 | µs | No Cz caps firing |
| TSBG | 6.6 | 6.4 | 6.2 | 6.0 | 6.0 | 6.0 | 5.6 | µs | Cz caps firing |

## TABLE 11-5 SIGNAL PROCESSING

| Description | Min | Max | Units | Notes |
|---|---|---|---|---|
| Threshold differential | 4 | 62 | counts | Note 1, 2 |
| Hysteresis | 0 | 50 | % | Note 1 |
| Median filter length | 5 | 9 | samples | Note 3; pipelined |
| Boxcar filter length | 2 | 64 | samples | Note 1, 3; pipelined |
| Burst randomization, % of burst spacing | ±12.5 | ±50 | % | Note 1, 3; See also Tables 7-2, 7-3, 7-4 |
| Drift compensation rate | 100 | 0.2 | secs/level | Note 1, 3 |
| Post-detection integrator length | 1 | 200 | counts | Note 1, 3 |
| Post-detection recalibration timer duration | 0.2 | 100 | secs | Note 1, 3 |
| Pulse stretch duration | 0.1 | 10 | secs | Note 1, 3 |
| Drift cal store to eeprom interval | 1 | 60 | mins | Note 1, 3 |

**Note 1:** For possible presets see Table 7-1
**Note 2:** Value can be made arbitrary in BG/OBJ or OBJ learn modes.
**Note 3:** This feature can be disabled.

# TABLE 11-6 DC SPECIFICATIONS

**20MHz, Vdd = 5V, Ta = recommended range, unless otherwise noted**

| Parameter | Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Vdd | Supply voltage | 4.5 | 5 | 5.5 | V | |
| Idd | Supply current | | 10 | 20 | mA | |
| Vdds | Supply turn-on slope | 70 | | | V/s | Required for proper startup |
| Vil | Low input logic level | | | 0.8 | V | BG, OBJ, XT1, DA0, DA1, DA2 |
| Vhl | High input logic level | 4 | | | V | BG, OBJ, XT1, DA0, DA1, DA2 |
| Vol | Low output voltage | | | 0.15 | V | OUT, STAT, ECS, DA0 - DA7 (Note 1) |
| Voh | High output voltage | Vdd-0.15 | | | V | OUT, STAT, ECS, DA0 - DA7 (Note 1) |
| Vain | AIN input range | 0 | | Vdd | V | |
| Iout | OUT, STAT pin current | | | 50 | µA | Recommended limit, source or sink |
| Idac | DAC pin currents | | | 100 | µA | Recommended limit, source or sink |
| Iil | Input leakage current | | | ±1 | µA | |
| Rchg | CHG source resistance | | 65 | | ohms | 0 [ Ichg [ 10mA |
| Rcs | CHG short resistance | 15 | 35 | | ohms | Note 2 |
| Ichg | CHG limiting current | | 36 | | mA | Vchg = 0 |
| Cx | Load capacitance range | 0 | | 1,000 | pF | |
| Ix | Load shunt conductance | 0 | | 250 | µA | Conductance across Cx |
| Czmax | Cz limit | | | 0.02 | µF | Per Cz |
| Csmax | Cs limit | | | 0.2 | µF | |
| Ar | Acquisition resolution | | | 8 | bits | |
| Al | Acquisition linearity | | | ±1 | lsb | |
| Av | Amp gain, recommended | | 284 | | V/V | Note 3 |
| S[1] | Sensitivity - digital path | | 16 | | fF/lsb | Note 3 |
| S[2] | Sensitivity - analog output | | 0.82 | | fF/mV | Note 3 |

**Note 1:** Sourcing or sinking 1mA current
**Note 2:** Resistance to ground on CHG that can be automatically detected as a short
**Note 3:** Using circuit of Figure 10-4

*All specifications subject to improvement.*

# TABLE 11.7 GAIN CHART

Gains computed at Vcc = 5.0, circuit of Figure 10-4 for both High Amp Gain and Low Amp Gain. An Excel spreadsheet program which allows easy recalculation of gains with component changes, Gaincalc.xls, can be found on the Quantum website.

**HIGH AMP GAIN**

| | In order of descending burst length | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 64 | 56 | 48 | 40 | 32 | 24 | 16 | 8 | 4 |
| pF / V | 0.823 | 0.941 | 1.097 | 1.317 | 1.65 | 2.19 | 3.29 | 6.58 | 13.17 |
| V / pF | 1.22 | 1.06 | 0.91 | 0.76 | 0.608 | 0.456 | 0.304 | 0.152 | 0.076 |
| fF / bit | 16.1 | 18.4 | 21.5 | 25.8 | 32.3 | 43.0 | 64.6 | 129.1 | 258.2 |
| % of Full Gain | 100.00% | 87.50% | 75.00% | 62.50% | 50.00% | 37.50% | 25.00% | 12.50% | 6.25% |

**LOW AMP GAIN**

| | In order of descending burst length | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 64 | 56 | 48 | 40 | 32 | 24 | 16 | 8 | 4 |
| pF / V | 13.80 | 15.78 | 18.41 | 22.09 | 27.61 | 36.81 | 55.22 | 110.44 | 220.9 |
| mV / pF | 72.4 | 63.4 | 54.3 | 45.3 | 36.2 | 27.2 | 18.1 | 9.1 | 4.5 |
| fF / bit | 271 | 309 | 361 | 433 | 541 | 722 | 1083 | 2165 | 4331 |
| % of Full Gain | 5.96% | 5.22% | 4.47% | 3.73% | 2.98% | 2.24% | 1.49% | 0.75% | 0.37% |

# 12 - 93LC46A SERIAL E$^2$PROM CONTENTS

Note that the Microchip 93LC46A uses byte-mode boundary addressing. Some prom programmers may not recognize this structure or may default to word (16 bit) mode. Consult your prom programmer manufacturer for details or upgrade requirements.

| Address | Select item | Parameter | Valid range (decimal) | Comments |
|---|---|---|---|---|
| 0 | 0 | sensitivity | 0..9 | |
| 1 | 1 | hysteresis | 0..3 | |
| 2 | 2 | reference offset | 0..9 | |
| 3 | 3 | unused | - | |
| 4 | 4 | pulse width | 0..8 | |
| 5 | 5 | burst length | 0..8 | |
| 6 | 6 | burst spacing | 0..8 | |
| 7 | 7 | randomization | 0..3 | |
| 8 | 8 | drift rate | 0..9 | |
| 9 | 9 | median filter | 0..1 | |
| 10 | A | boxcar averaging | 0..6 | |
| 11 | B | detect integrator | 0..8 | |
| 12 | C | max on-duration | 0..9 | |
| 13 | D | detection mode | 0..9 | |
| 14 | E | calibration control | 0..3 | |
| 15 | F | drift store / data locking | 0..9 | |
| 16 | G | serial modes / UART rate | 0..9 | |
| 17 | H | verbose data | 0..8 | |
| 18 | J | polarities | 0..3 | |
| 19 | L | output stretch | 0..9 | |
| 20 | N | unused | - | |
| 21 | P | SPI format | 0..1 | |
| 22 | U | mode / SPI data output | 0..8 | |
| 23 | - | Cz store | 0..4 | cal store for Cz charge cancellation capacitors |
| 24 | - | offset store | 0..255 | cal store for R2R DAC |
| 25 | - | reference store | 0..255 | cal store for reference, incl. periodic [F.a] store |
| 26 | - | threshold store | 0..255 | for (+) threshold only; (-) threshold is a lookup |
| 27 | - | unused | - | |
| 28 | - | mode flags | 0..255 | see chart below |
| 29 | - | check byte | 85..89 | must be 85 (0x55 - 0x59 hex) for e$^2$prom to be recognized |

## Mode Flag Bits

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Function | * | - | * | * | * | *bg | bgobj | obj |

- Unused
* Bits used for internal processing; the state of these are ignored, even though written

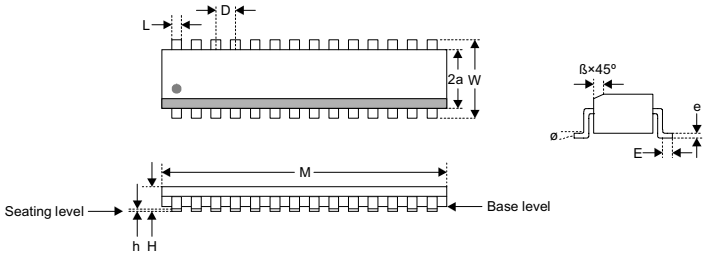
Note: All process flags are all ignored on powerup if 'data locking' [F.b] is off

Eeprom is read only once on power up;e$^2$prom will be reread and a recalibration induced if pin 1 is held low for 10us minimum.

Flag bits: obj 1 = unit in 'pure' obj mode
bgobj 1 = unit in 'bgobj' mode
bg 1 = unit in bg mode (stored to e$^2$prom but not read back)

Notes: If obj & bgobj are both 0, unit is presumed to be in pure 'bg' mode
If any e$^2$prom location between address 0 and 21 is out of a 0..9 bound, or if the check byte (address 28) is not 0x55, the e$^2$prom is ignored and default settings are used instead.

# 13 - PACKAGE OUTLINE - QT9701B2-S

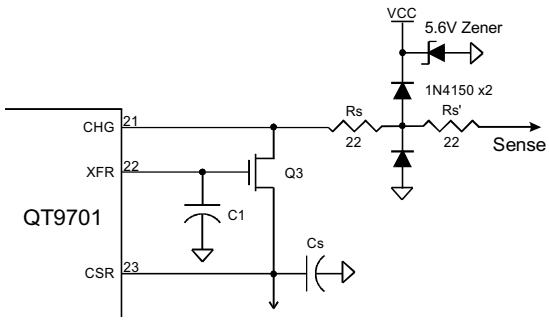



| Package type: 28-pin SOIC | | | | | | |
|---|---|---|---|---|---|---|
| SYMBOL | Millimeters | | | Inches | | |
| | Min | Max | Notes | Min | Max | Notes |
| | | | | | | |
| M | 17.703 | 18.085 | | 0.697 | 0.712 | |
| W | 10.007 | 10.643 | | 0.394 | 0.419 | |
| 2a | 7.416 | 7.595 | | 0.292 | 0.299 | |
| H | 2.362 | 2.642 | | 0.093 | 0.104 | |
| h | 0.101 | 0.3 | | 0.004 | 0.012 | |
| D | 1.270 | 1.27 | BSC | 0.050 | 0.050 | BSC |
| L | 0.355 | 0.483 | | 0.014 | 0.019 | |
| E | 0.406 | 1.143 | | 0.016 | 0.045 | |
| e | 0.241 | 0.318 | | 0.009 | 0.013 | |
| ß | 0.381 | 0.762 | | 0.015 | 0.030 | |
| Ø | 0º | 8º | | 0º | 8º | |

# 14 - ESD NETWORK

The network of Figure 14-1 is suggested to shunt ESD currents without significantly loading the sense lead with unwanted parasitic capacitance. Care should be taken that the sense lead does not overshoot or ring during QT pulses, causing conduction into one of the two clamp diodes; such conduction currents can lead to a marked drop in QT efficiency, and can also cause a strong thermal dependency due to the thermal coefficients of the diodes. These effects are most pronounced when the ringing occurs at the transfer edge, i.e. when Q3 turns on from the leading edge of XFR. Raising the two 22 ohm resistors will damp resonances while simultaneously increasing ESD protection. Resonances can also be reduced by making the sense wire short, running the sense wire through coaxial cable, or running the sense wire along a grounded metal plane such as a piece of sheet metal.

**FIGURE 14-1 Recommended ESD Network**




The presence of ringing can be tested for without an oscilloscope by slightly heating one of the clamp diodes and watching the analog signal level. If ringing-induced diode clamping is occurring, the signal will suffer substantial drift.

The two diodes and zener should be placed very close to the sense lead, and physically configured so that the diode clamping currents return to earth ground without traversing the remaining portion of the PCB. This calls for a robust, very direct chassis ground connection near the sense lead connection, and all other ground-referenced connections including power and control I/O lines coming from the same side of the PCB as the sense lead. Where this is not possible, the return ground path for ESD currents should be made very heavy and be routed away from the remaining sensor circuitry via an independent path back to the nearest chassis connection.

ESD can also be controlled by limiting access to the sense electrode, for example by covering the electrode with plastic or placing it behind a nonconductive surface. Note that the resistors in the ESD circuit can adversely affect the CHG short circuit detection feature by limiting current flow out of CHG.

**For SMT designs:** A BAV99 dual diode makes an acceptable diode clamp in one package.

**Transient voltage suppressors** (TVS) are basically 'dirty', heavy-duty zeners and should not be used directly on the CHG line. TVS diodes have extremely high levels of nonlinear junction capacitance and in most cases high leakage currents which can make the sensor drift prone and swamped with excess Cx.

**Ferrite beads:** Ferrite beads and similar lossy inductors can sometimes be used to slow the edges of the QT pulses while simultaneously slowing ESD transients. Great care should be taken to ensure that the resulting circuit is properly damped to eliminate ringing for the above mentioned reasons. Additional damping can be had by further increasing series resistance.

# 15 - CUSTOMIZATION

The QT9701B2 can be mask-customized for various applications to suit. For example, more specific timing and signal processing parameters may be incorporated, or the defaults can be altered so as to eliminate the need for an external $e^2$prom. If customized defaults are used, they can still be overridden by means of an external $e^2$prom in case requirements change.

It is also possible to incorporate entirely new features into the device for a specific application. Consult Quantum for further details on customization options.

**QUANTUM Research Group Ltd.**


651 Holiday Drive Bldg 5 / 300
Pittsburgh, PA 15220 USA
Tel: 412-391-7367 Fax: 412-291-1015
email: admin@qprox.com
**http://qprox.com**

***In the United Kingdom***
Enterprise House, Southampton, Hants SO14 3XB
Tel: +44 (0)23 8045 3934 Fax: +44 (0)23 8045 3939