HARRIS

HMM-11820

GaAs MMIC Amplifier 6–18 GHz

PRODUCT DATA

Features

- **Low DC Current Draw Provides High dB/mA Performance**
- **On-Chip Source Resistor Network for Easy Bias Point Selection**
- **Directly Cascadable Without Interstage Matching**
- **DC Blocking of Both RF Input and Output**
- **Ti/Pt/Au Metallization and Large Gate Cross Section for Enhanced Reliability**
- **Dielectric Scratch/Short Circuit Protection Improves Durability**
- **Individual Die Serialization Provides the *Ultimate* in Traceability**
- **Custom Wafer Qualification Available to Meet Source Control Drawings**

Description

The HMM-11820 is a cascadable, broadband gain block designed for applications where minimum DC power consumption is an important consideration. A completely integrated amplifier, the HMM-11820 includes DC blocking of the RF input and output and an on-chip source bias resistor network.

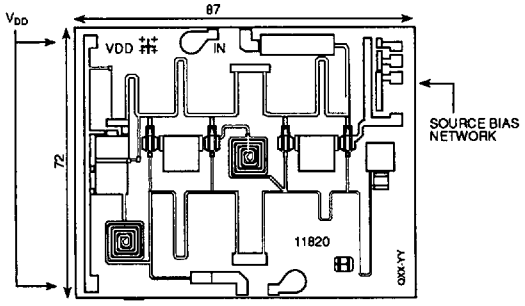
The distributed amplifier design (4x 200 µm FETs) offers ultra wide bandwidth performance, while special active layer implants and DC-series FET biasing give the HMM-11820 both high dB/mA and low noise figure.

Electrical performance competes directly with MIC hybrids, while its small size and ruggedness as a monolithic circuit, give the HMM-11820 an advantage for demanding military applications or wherever space is at a premium.

The HMM-11820 is based on the same process as Harris Microwave's HMF family of discrete 0.5 µm recessed gate FETs providing a broad manufacturing baseline.

Standard wafer qualification includes 100 percent on-wafer DC probe and visual inspection, as well as RF evaluation on a sample test basis. Special wafer qualification to customer electrical specifications and/or screening requirements is available.

Device Outline

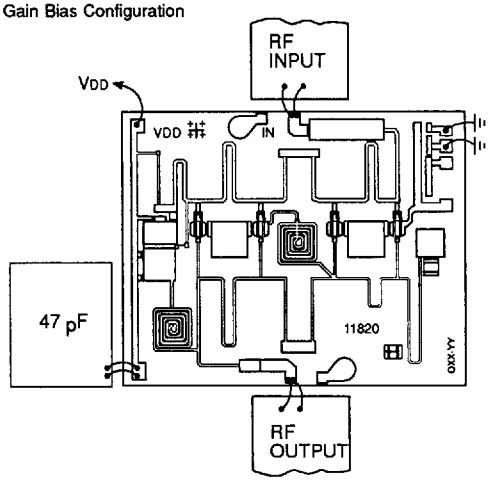


DIMENSIONS IN MILS

CHIP THICKNESS 5 MILS
Au BACKSIDE METALLIZATION

Bonding Diagram

Gain Bias Configuration



Electrical Specifications at T_A = 25°C

SYMBOL	PARAMETER	UNITS	MIN	TYP	MAX
Freq.	Operating Frequency Range	GHz	6		18
S_{21}	Small Signal Gain	dB	4.5	6.0	
ΔG	Gain Flatness	dB		±0.5	±0.8
P_{1dB}	Output Power at 1dB Gain Compression	dBm		12.0	
VSWR	Input/Output VSWR			1.5:1	2:1
NF	Noise Figure	dB		5.5	
Conditions for above : V_{DD} = +8.5 V, I_{DD} = 35 mA (typical), Gain Bias Configuration					
I_{DD}	Drain Current, V_{DD} = +8.0 V, R_S = 0 Ω	mA	25	50	80

NOTES: 1.Typical RF performance and minimum limits are based on testing of sample units from each wafer on 50 Ω test carriers and do not include correction for tuner/fixture losses. DC min/max limits are guaranteed by 100% on-wafer probe testing.
2. Max I_{DD} is the terminal current with R_S = 0 Ω. This is the saturated source drain current (I_{DSS}) for the series parallel combination of FETs in the circuit.

Product Ratings

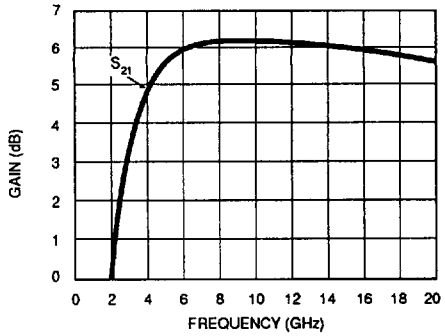
SYMBOL	PARAMETER	MAXIMUM OPERATING CONDITIONS	
		RECOMMENDED	ABSOLUTE
V_{DD}	Supply Voltage	+10.5 V	+12.5 V
T_{CH}	Channel Temperature, Operating	+180°C	+250°C
T_{STG}	Storage Temperature	–65°C to +180°C	–65°C to +250°C

NOTE: Permanent damage may result from operation at conditions beyond absolute maximum ratings.

Refer to Application Note 201 for die attachment and wire-bonding recommendations.

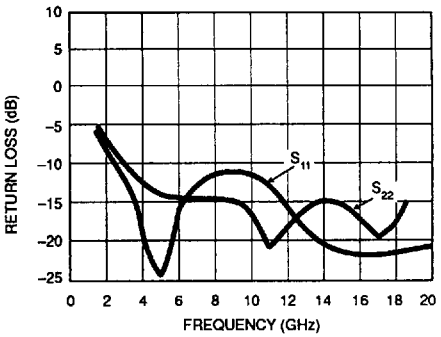
HMM-11820

Gain Performance



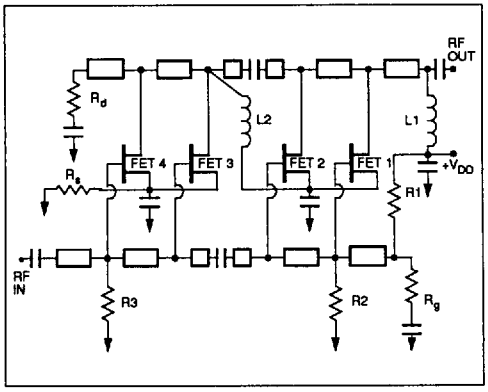
Gain (S_{21}) vs. Frequency. V_{DD} = 8.5 V, I_{DD} = 35 mA.

Return Loss

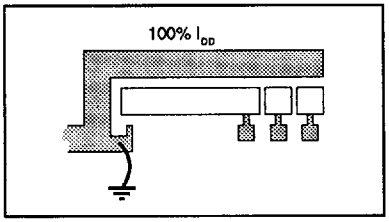


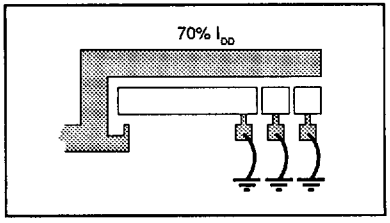
Input Return Loss (S_{11}) and Output Return Loss (S_{22}) vs. Frequency.

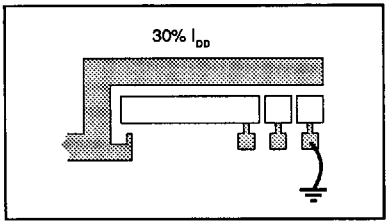
Device Schematic

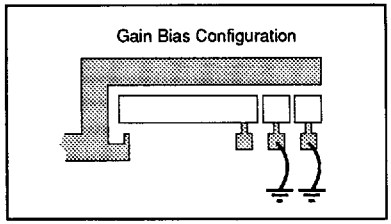


Source Resistor Bias Network, Nominal Values









Typical S-Parameters, V_{DD} = 8.5 V, I_{DD} = 35 mA (Gain Bias Configuration)

FREQ (GHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
2.0	.416	−152.4	1.042	−155.2	.010	70.6	.486	−158.4
3.0	.222	161.5	1.392	171.3	.018	61.2	.309	163.6
4.0	.058	96.8	1.735	135.6	.029	48.4	.217	144.0
5.0	.101	−59.9	1.930	102.7	.041	22.3	.198	130.9
6.0	.193	−98.6	2.002	70.5	.051	−4.0	.203	110.2
7.0	.243	−130.5	2.001	42.3	.060	−29.5	.206	87.8
8.0	.253	−157.4	1.998	14.9	.068	−55.6	.192	61.6
9.0	.235	174.3	2.026	−11.6	.078	−78.3	.153	30.3
10.0	.197	140.2	2.090	−39.3	.086	−102.3	.105	−11.2
11.0	.139	107.2	2.131	−68.1	.092	−122.6	.087	−82.0
12.0	.087	63.3	2.144	−98.2	.098	−145.3	.127	−132.7
13.0	.050	7.4	2.077	−127.4	.096	−170.7	.181	−159.7
14.0	.031	27.0	2.028	−157.9	.096	162.0	.222	178.8
15.0	.079	26.6	1.985	174.1	.096	133.7	.223	164.3
16.0	.124	7.3	2.010	144.5	.099	102.6	.192	156.2
17.0	.155	−23.5	2.000	109.6	.113	70.1	.155	177.1
18.0	.168	−37.3	1.924	75.2	.126	36.6	.158	−157.7

NOTE: S-Parameters include bond wire inductances and are measured in a 50 Ω microstrip fixture.