NEC

MOS INTEGRATED CIRCUIT

μPD16640C

300/309-OUTPUT TFT-LCD SOURCE DRIVER (64 GRAY SCALE)

DESCRIPTION

The μPD16640C is a source driver for TFT-LCD 64-gray scale displays. Its logic circuit operates at 3.3 V and the driver circuit operates at 3.3 or 5.0 V (selectable). The input data is digital data at 6 bits x 3 dots, and 260,000 colors can be displayed in 64-value outputs γ-corrected by the internal D/A converter and 11 external power supplies.

The clock frequency is 55 MHz MIN. By switching over the number of outputs between 300 and 309, the μPD16640C can be used in TFT-LCD panels conforming to the SVGA/XGA standards.

FEATURES

- CMOS level input
- Number of outputs selectable (O_{sel} = H : 300 outputs, O_{sel} = L : 309 outputs)
- 6 bits (gray scale data) x 3 dots input
- 64-value output by 11 external power supplies and internal D/A converter
- Output dynamic range : V_{SS2} + 0.1 V to V_{DD2} – 0.1 V
- High-speed data transfer: $f_{MAX.}$=55 MHz MIN.(internal data transfer speed when V_{DD1} = 3.0 V)
- Precharge-less output buffer
- Level of γ-corrected power supply can be inverted.
- Input data inversion function (INV)
- Logic power supply (V_{DD1}) : 3.3 V ± 0.3 V
- Driver power supply (V_{DD2}) : 3.3 V ± 0.3 V (V_{sel} = H)
  5.0 V ± 0.5 V (V_{sel} = L)

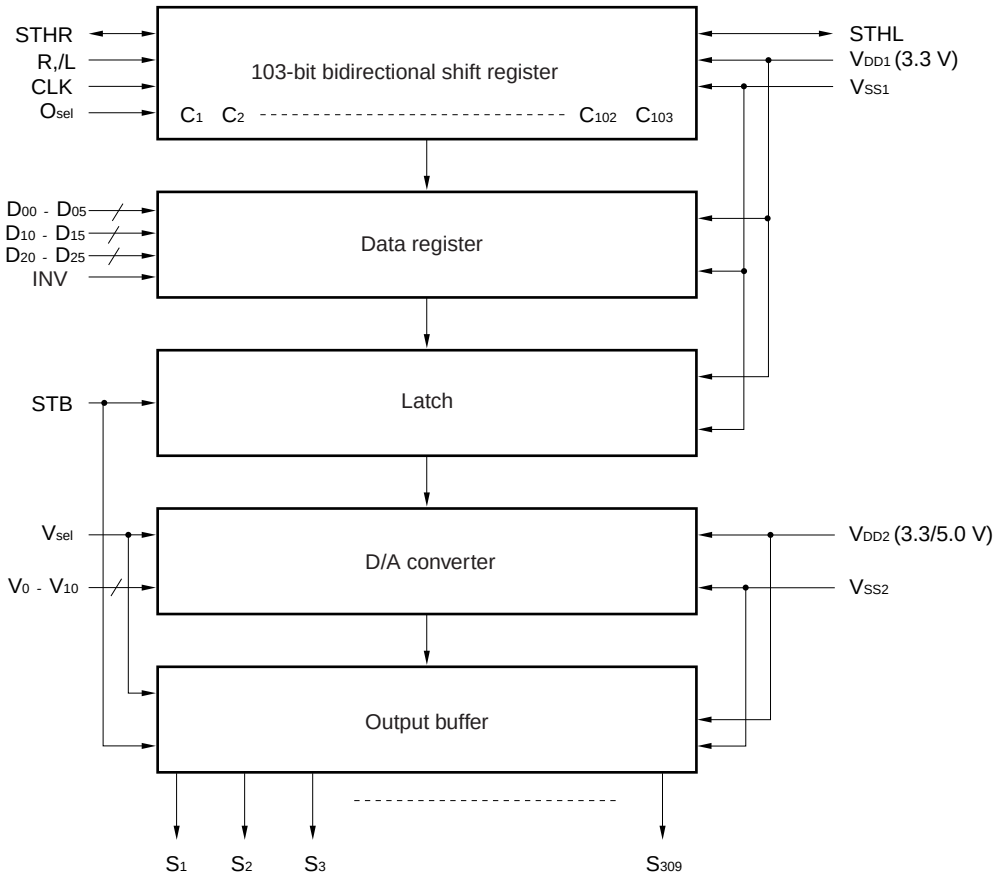
ORDERING INFORMATION

Part Number	Package
μPD16640CN-xxx	TCP (TAB package)

Remark The TCP's external shape is customized. To order your TCP's external shape, please contact a NEC salesperson.

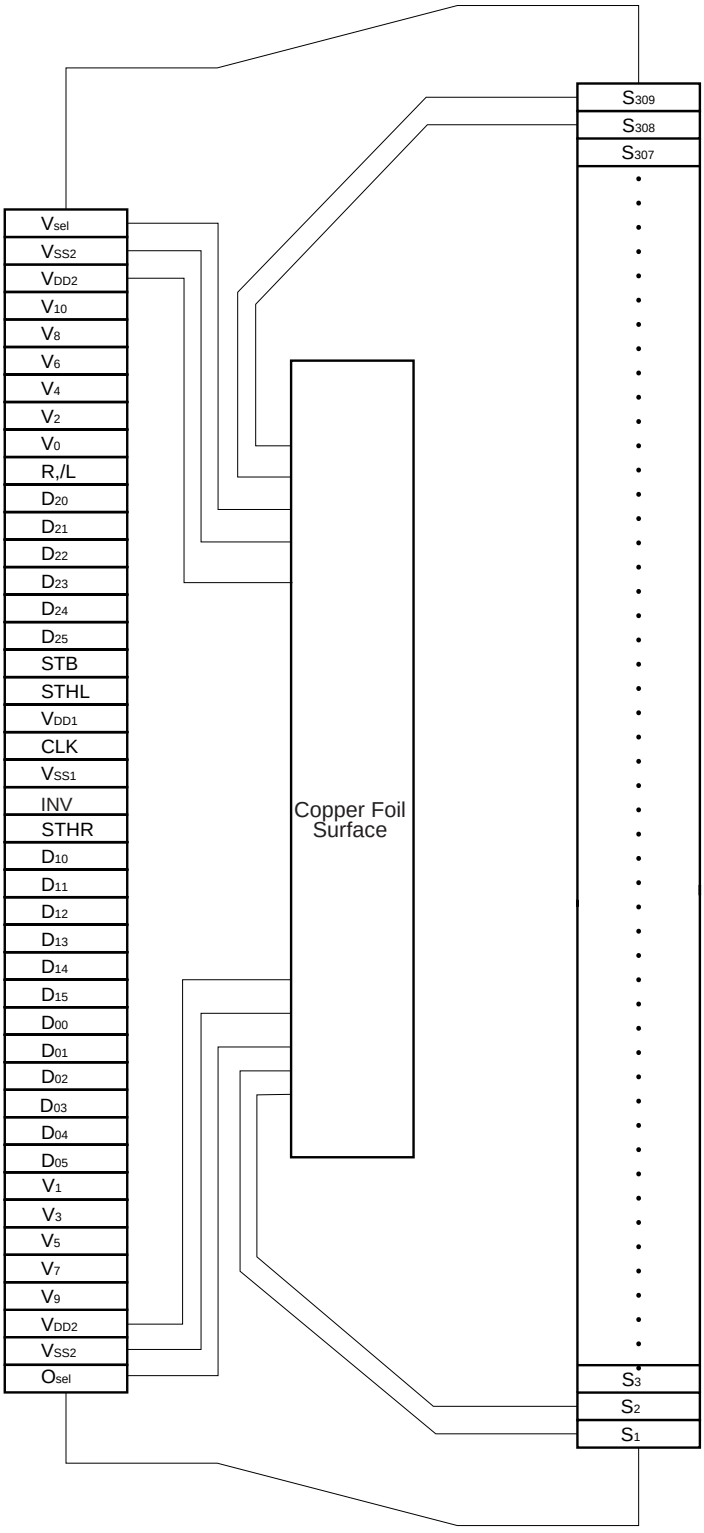
Document No. S11269EJ1V1DS00 (1st edition)
Date Published June 1999 NS CP (K)
Printed in Japan

1. BLOCK DIAGRAM



Remark /xxx indicates active low signal.

2. PIN CONFIGURATION (μPD16640CN-xxx)



Remark O_{sel} and V_{sel} pins are internally pulled up.

Therefore, the number of input pins can be reduced by opening or short-circuiting these pins to V_{SS2} by means of TCP writing.

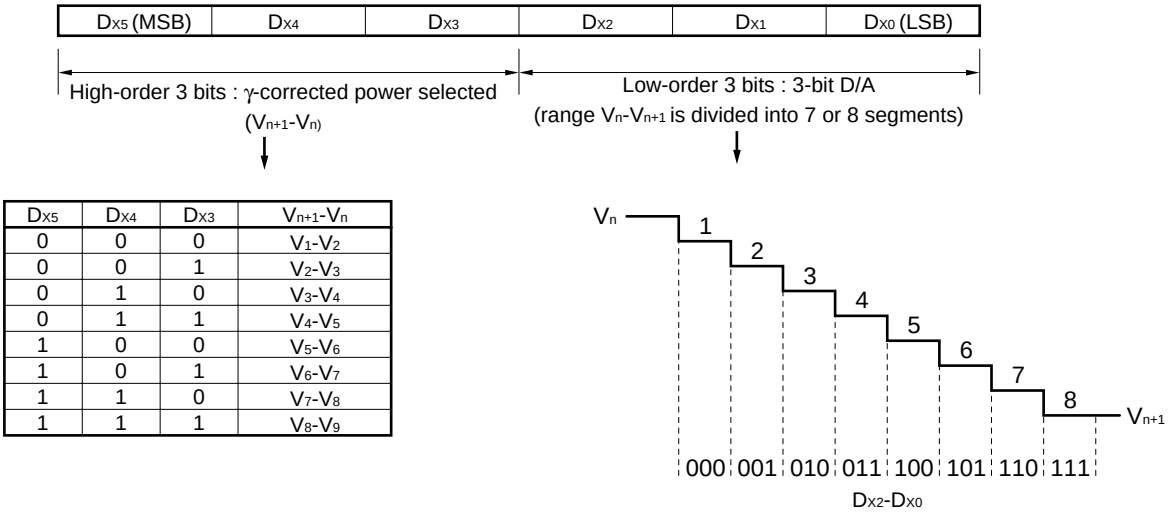
3. PIN FUNCTIONS

Pin Symbol	Pin Name	Description
S_1 to S_{309}	Driver output	Output 64 gray scale analog voltages converted from digital signals. O_{sel} = H : 300 outputs (S_1 - S_{150}, S_{160} - S_{309}) O_{sel} = L : 309 outputs (S_1 - S_{309}) Output pins S_{151} to S_{159} are invalid in 300-output mode.
D_{00} to D_{05} D_{10} to D_{15} D_{20} to D_{25}	Display data input	Inputs 18-bit-wide display gray scale data (6 bits) x 3 dots (RGB). D_{X0} : LSB, D_{X5} : MSB
R,/L	Shift direction select input	This pin inputs/outputs start pulses in cascade mode. Shift direction of shift register is as follows: R,/L = H : STHR input, $S_1 \rightarrow S_{309}$, STHL output R,/L = L : STHL input, $S_{309} \rightarrow S_1$, STHR output
STHR	Right shift start pulse I/O	R,/L = H : Inputs start pulse R,/L = L : Outputs start pulse
STHL	Left shift start pulse I/O	R,/L = H : Outputs start pulse R,/L = L : Inputs start pulse
O_{sel}	Number of output selection	Selects number of outputs. This pin is internally pulled up by V_{DD1} power supply. O_{sel} = H : 300 outputs O_{sel} = L : 309 outputs
V_{sel}	Driver voltage selection	Selects driver voltage. This pin is internally pulled up by V_{DD2} power supply. V_{sel} = H : 300 outputs V_{sel} = L : 309 outputs
CLK	Shift clock input	Inputs shift clock to shift register. Display data is loaded to data register at rising edge of this pin. When O_{sel} = H, start pulse output goes high at rising edge of 100th clock after start pulse has been input, and serves as start pulse to driver in next stage. When O_{sel} = L, start pulse output goes high at rising edge of 103rd clock after start pulse has been input, and serves as start pulse to driver in next stage. 103rd clock of driver in first stage serves as start pulse of driver in next stage.
STB	Latch input	Contents of data register are latched at rising edge, transferred to D/A converter, and output as analog voltage corresponding to display data. Contents of internal shift register are cleared after STB has been input. One pulse of this signal is input when μPD16640C is started, and then device operates normally. For STB input timing, refer to **8. SWITCHING CHARACTERISTIC WAVEFORM.**
V_0 to V_{10}	γ-corrected power supply	Inputs γ-corrected power from external source. V_{SS2}+0.1 V ≤ V_{10} ≤ V_9 ≤ V_8 ≤ V_7 ≤ V_6 ≤ V_5 ≤ V_4 ≤ V_3 ≤ V_2 ≤ V_1 ≤ V_0 ≤V_{DD2}–0.1 V or V_{SS2}+0.1 V ≤ V_0 ≤ V_1 ≤ V_2 ≤ V_3 ≤ V_4 ≤ V_5 ≤ V_6 ≤ V_7 ≤ V_8 ≤ V_9 ≤ V_{10} ≤V_{DD2}–0.1 V Maintain gray scale power supply during gray scale voltage output.
INV	Data inversion input	Input data can be inverted when display data is loaded. INV = H : Inverts and loads input data. INV = L : Does not invert input data.
V_{DD1}	Logic circuit power supply	3.3 V ± 0.3 V
V_{DD2}	Driver circuit power supply	V_{sel} = H : V_{DD2} = 3.3 V ± 0.3 V V_{sel} = L : V_{DD2} = 5.0 V ± 0.5 V
V_{SS1}	Logic ground	Ground
V_{SS2}	Driver ground	Ground

Caution Be sure to turn on power in the order V_{DD1}, logic input, V_{DD2}, and gray scale power (V_0 to V_{10}), and turn off power in the reverse order, to prevent the μPD16640C from being damaged by latchup. Be sure to observe this power sequence even during a transition period.

4. RELATION BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

The 11 major points on the γ-characteristic curve of the LCD panel are arbitrarily set by external power supplies V_0 through V_{10}. If the display data is 00H or 3FH, gray scale voltage V_0 or V_{10} is output. If the display data is in the range 01H to 3EH, the high-order 3 bits select an external powers pair V_{n+1}, V_n. The low-order 3 bits evenly divide the range of V_{n+1}, V_n into eight segments by means of D/A conversion (however, the ranges from V_9 to V_8 and from V_2 to V_1 are divided into seven segments) to output a 64-grayscale voltage.



D_{X5}	D_{X4}	D_{X3}	V_{n+1}-V_n
0	0	0	V_1-V_2
0	0	1	V_2-V_3
0	1	0	V_3-V_4
0	1	1	V_4-V_5
1	0	0	V_5-V_6
1	0	1	V_6-V_7
1	1	0	V_7-V_8
1	1	1	V_8-V_9

Figure 4-1. Relation between Input Data and γ-corrected Voltage

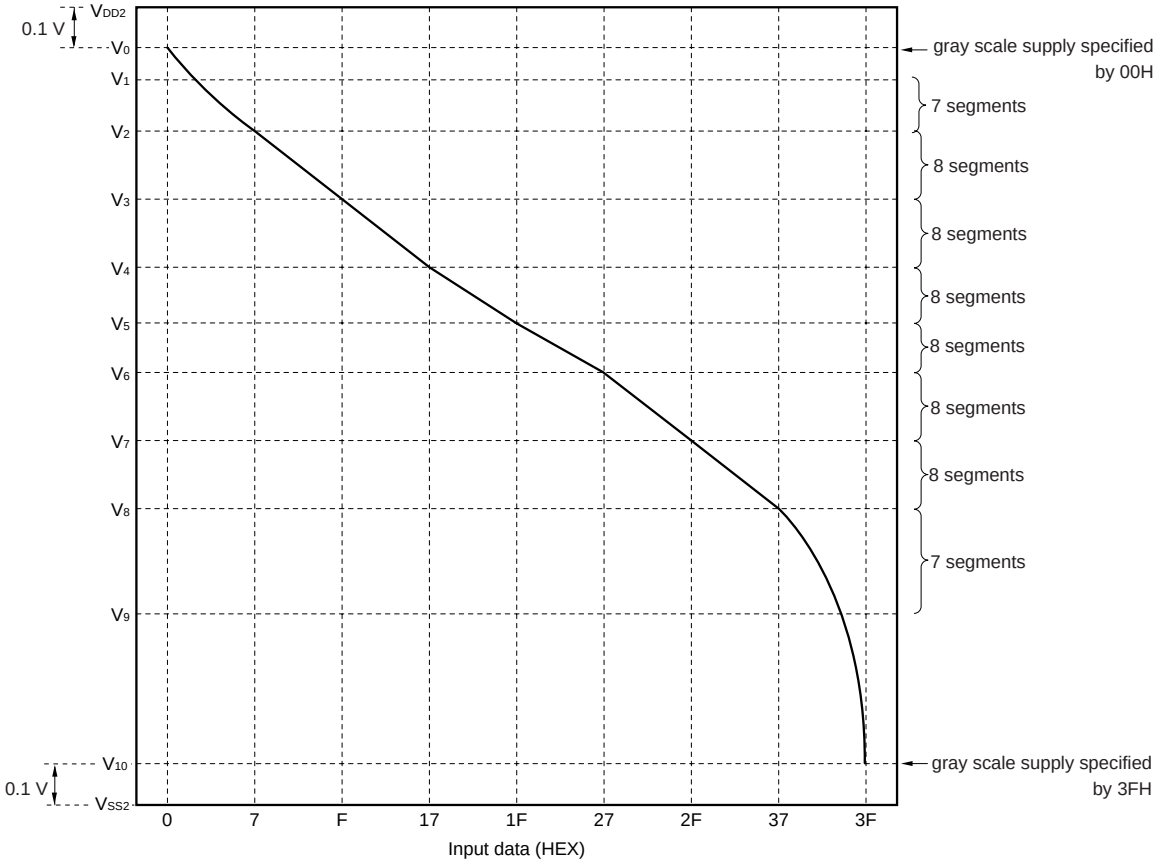


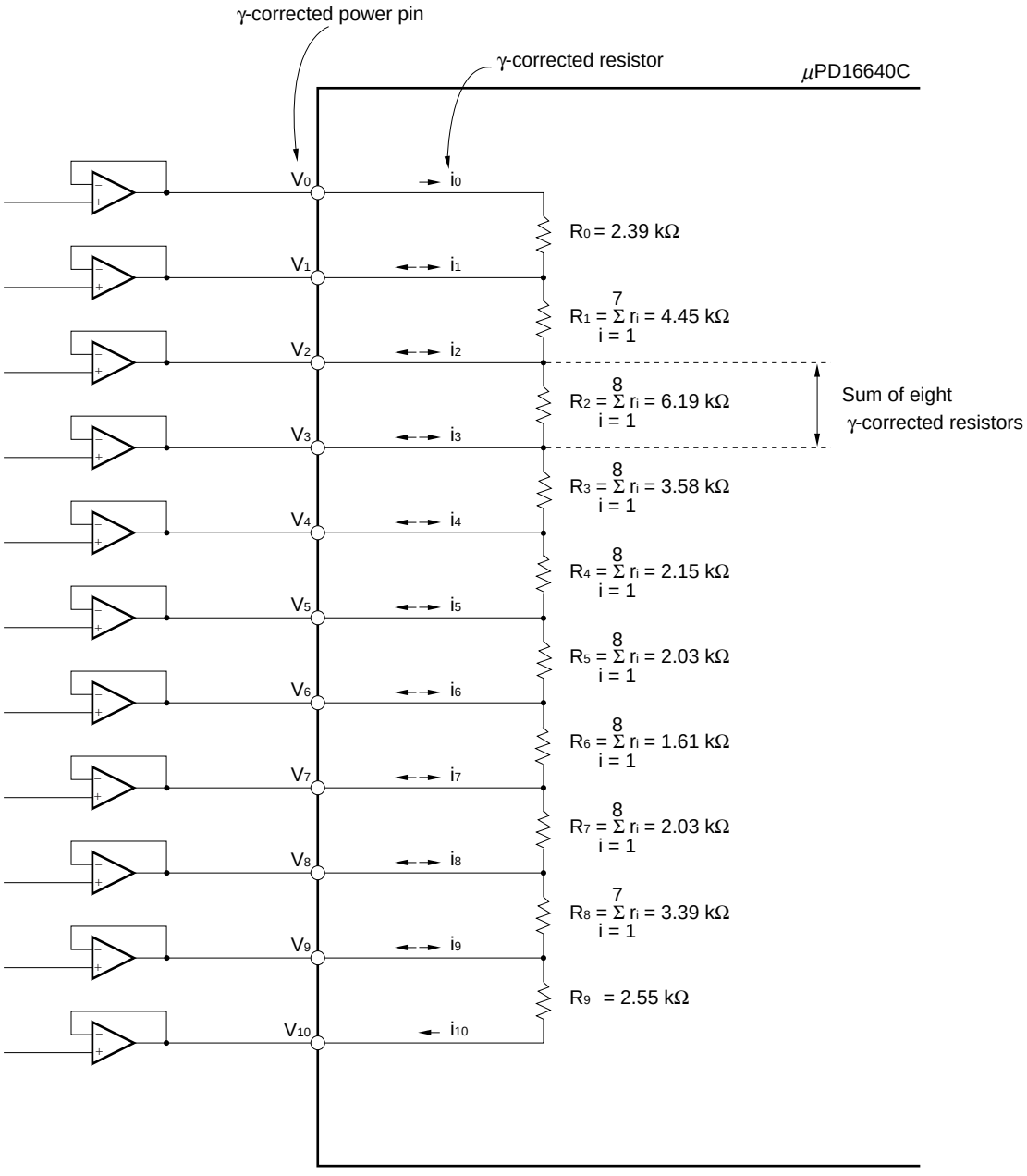
Table 4-1. Relation between Input Data and Output Voltage

Input Data	D_{X5}	D_{X4}	D_{X3}	D_{X2}	D_{X1}	D_{X0}	Output Voltage
00H	0	0	0	0	0	0	V_0
01H	0	0	0	0	0	1	$V_2 + (V_1 - V_2) \times 6/7$
02H	0	0	0	0	1	0	$V_2 + (V_1 - V_2) \times 5/7$
03H	0	0	0	0	1	1	$V_2 + (V_1 - V_2) \times 4/7$
04H	0	0	0	1	0	0	$V_2 + (V_1 - V_2) \times 3/7$
05H	0	0	0	1	0	1	$V_2 + (V_1 - V_2) \times 2/7$
06H	0	0	0	1	1	0	$V_2 + (V_1 - V_2) \times 1/7$
07H	0	0	0	1	1	1	V_2
08H	0	0	1	0	0	0	$V_3 + (V_2 - V_3) \times 7/8$
09H	0	0	1	0	0	1	$V_3 + (V_2 - V_3) \times 6/8$
0AH	0	0	1	0	1	0	$V_3 + (V_2 - V_3) \times 5/8$
0BH	0	0	1	0	1	1	$V_3 + (V_2 - V_3) \times 4/8$
0CH	0	0	1	1	0	0	$V_3 + (V_2 - V_3) \times 3/8$
0DH	0	0	1	1	0	1	$V_3 + (V_2 - V_3) \times 2/8$
0EH	0	0	1	1	1	0	$V_3 + (V_2 - V_3) \times 1/8$
0FH	0	0	1	1	1	1	V_3
10H	0	1	0	0	0	0	$V_4 + (V_3 - V_4) \times 7/8$
11H	0	1	0	0	0	1	$V_4 + (V_3 - V_4) \times 6/8$
12H	0	1	0	0	1	0	$V_4 + (V_3 - V_4) \times 5/8$
13H	0	1	0	0	1	1	$V_4 + (V_3 - V_4) \times 4/8$
14H	0	1	0	1	0	0	$V_4 + (V_3 - V_4) \times 3/8$
15H	0	1	0	1	0	1	$V_4 + (V_3 - V_4) \times 2/8$
16H	0	1	0	1	1	0	$V_4 + (V_3 - V_4) \times 1/8$
17H	0	1	0	1	1	1	V_4
18H	0	1	1	0	0	0	$V_5 + (V_4 - V_5) \times 7/8$
19H	0	1	1	0	0	1	$V_5 + (V_4 - V_5) \times 6/8$
1AH	0	1	1	0	1	0	$V_5 + (V_4 - V_5) \times 5/8$
1BH	0	1	1	0	1	1	$V_5 + (V_4 - V_5) \times 4/8$
1CH	0	1	1	1	0	0	$V_5 + (V_4 - V_5) \times 3/8$
1DH	0	1	1	1	0	1	$V_5 + (V_4 - V_5) \times 2/8$
1EH	0	1	1	1	1	0	$V_5 + (V_4 - V_5) \times 1/8$
1FH	0	1	1	1	1	1	V_5
20H	1	0	0	0	0	0	$V_6 + (V_5 - V_6) \times 7/8$
21H	1	0	0	0	0	1	$V_6 + (V_5 - V_6) \times 6/8$
22H	1	0	0	0	1	0	$V_6 + (V_5 - V_6) \times 5/8$
23H	1	0	0	0	1	1	$V_6 + (V_5 - V_6) \times 4/8$
24H	1	0	0	1	0	0	$V_6 + (V_5 - V_6) \times 3/8$
25H	1	0	0	1	0	1	$V_6 + (V_5 - V_6) \times 2/8$
26H	1	0	0	1	1	0	$V_6 + (V_5 - V_6) \times 1/8$
27H	1	0	0	1	1	1	V_6
28H	1	0	1	0	0	0	$V_7 + (V_6 - V_7) \times 7/8$
29H	1	0	1	0	0	1	$V_7 + (V_6 - V_7) \times 6/8$
2AH	1	0	1	0	1	0	$V_7 + (V_6 - V_7) \times 5/8$
2BH	1	0	1	0	1	1	$V_7 + (V_6 - V_7) \times 4/8$
2CH	1	0	1	1	0	0	$V_7 + (V_6 - V_7) \times 3/8$
2DH	1	0	1	1	0	1	$V_7 + (V_6 - V_7) \times 2/8$
2EH	1	0	1	1	1	0	$V_7 + (V_6 - V_7) \times 1/8$
2FH	1	0	1	1	1	1	V_7
30H	1	1	0	0	0	0	$V_8 + (V_7 - V_8) \times 7/8$
31H	1	1	0	0	0	1	$V_8 + (V_7 - V_8) \times 6/8$
32H	1	1	0	0	1	0	$V_8 + (V_7 - V_8) \times 5/8$
33H	1	1	0	0	1	1	$V_8 + (V_7 - V_8) \times 4/8$
34H	1	1	0	1	0	0	$V_8 + (V_7 - V_8) \times 3/8$
35H	1	1	0	1	0	1	$V_8 + (V_7 - V_8) \times 2/8$
36H	1	1	0	1	1	0	$V_8 + (V_7 - V_8) \times 1/8$
37H	1	1	0	1	1	1	V_8
38H	1	1	1	0	0	0	$V_9 + (V_8 - V_9) \times 6/7$
39H	1	1	1	0	0	1	$V_9 + (V_8 - V_9) \times 5/7$
3AH	1	1	1	0	1	0	$V_9 + (V_8 - V_9) \times 4/7$
3BH	1	1	1	0	1	1	$V_9 + (V_8 - V_9) \times 3/7$
3CH	1	1	1	1	0	0	$V_9 + (V_8 - V_9) \times 2/7$
3DH	1	1	1	1	0	1	$V_9 + (V_8 - V_9) \times 1/7$
3EH	1	1	1	1	1	0	V_9
3FH	1	1	1	1	1	1	V_{10}

4.1 γ-corrected Power Circuit

The reference power supply of the D/A converter consists of a ladder circuit with a total of 64 resistors, and resistance Σri between γ-corrected power pins differs depending on each pair of γ-corrected power pins. One pair of γ-corrected power pins consists of seven or eight series resistors, and resistance Σri in the figure below is indicated as the sum of the seven or eight resistors. The resistance ratio between the γ-corrected power pins (Σri ratio) is designed to be a value relatively close to the ratio of the γ-corrected voltages V_1 to V_9 (gray-scale voltages in 8 steps) used in an actual LCD panel. Under ideal conditions where there is no difference between the two, therefore, there is no voltage difference between the voltage of the γ-corrected power supplies and the gray-scale voltages in 8 steps of the resistor ladder circuits of the μPD16640C, and no current flows into the γ-corrected power pins V_1 to V_9. As a result, a voltage-follower circuit is not necessary.

Figure 4-2. γ-corrected Power Circuit



5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format : 6 bits x RGB(3 dots)
Input width : 18 bits

(1) R,/L = H (right shift)

Output	S_1	S_2	S_3	…	S_{308}	S_{309}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	…	D_{10} to D_{15}	D_{20} to D_{25}

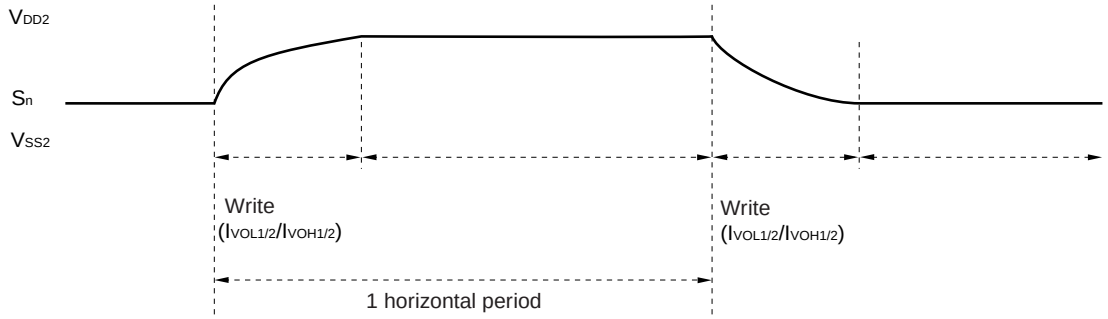
(2) R,/L = L (left shift)

Output	S_1	S_2	S_3	…	S_{299}	S_{300}
Data	D_{00} to D_{05}	D_{10} to D_{15}	D_{20} to D_{25}	…	D_{10} to D_{15}	D_{20} to D_{25}

6. OPERATION OF OUTPUT BUFFER

The output buffer consists of an operational amplifier circuit that does not perform precharge operation.
Therefore, driver output current $I_{VOH1/2}$ is the charging current to the LCD, and $I_{VOL1/2}$ is the discharging current.

Figure 6-1. LCD Panel Driving Waveform



7. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic power supply	V_{DD1}	–0.3 to +4.5	V
Driver power supply	V_{DD2}	–0.3 to +6.0	V
Input voltage	V_I	–0.3 to $V_{DD1,2}$ + 0.3	V
Output voltage	V_O	–0.3 to $V_{DD1,2}$ + 0.3	V
Operating ambient temperature	T_A	–10 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

Recommended Operating Range (T_A = –10 to +75 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Logic supply voltage	V_{DD1}		3.0	3.3	3.6	V
Driver supply voltage	V_{DD2}	V_{sel} = H	3.0	3.3	3.6	V
		V_{sel} = L	4.5	5.0	5.5	V
High-level input voltage	V_{IH}	R,/L, CLK, STB, O_{sel}, $V_{sel,}$	0.7V_{DD1}		V_{DD1}	V
Low-level input voltage	V_{IL}	STHR(STHL), D_{00}-D_{05},D_{10}-D_{15}, D_{20}-D_{25}	0		0.3V_{DD1}	V
γ-corrected supply voltage	V_0-V_{10}		V_{SS2}+0.1		V_{DD2}–0.1	V
Maximum clock frequency	$f_{MAX.}$		55			MHz

Electrical Characteristics (T_A = –10 to +75 °C, V_{DD1} = 3.3 V ± 0.3 V, V_{DD2} = 3.3 V ± 0.3 V or 5.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input leakage current	I_{IL}	D_{00}-D_{05}, D_{10}-D_{15}, D_{20}-D_{25}, R,/L, STB				±1.0	μA
Pull-up resistor	R_{PU}	V_{DD1} = 3.3 V, O_{sel}, V_{sel}		40	100	250	kΩ
High-level output voltage	V_{OH}	STHR(STHL),I_O=–1.0 mA		V_{DD1} – 0.5			V
Low-level output voltage	V_{OL}	STHR(STHL),I_O=+1.0 mA				0.5	V
Static current consumption of γ-corrected supply current (V_{DD2} = 3.3 V or 5.0 V)	I_{vn1}	V_{DD1}=3.3 V V_n–V_{n+1}=0.5 V	V_0-V_1	105	210	420	μA
			V_1-V_2	56	113	226	μA
			V_2-V_3	41	82	164	μA
			V_3-V_4	70	140	280	μA
			V_4-V_5	117	234	468	μA
			V_5-V_6	124	248	496	μA
			V_6-V_7	156	313	626	μA
			V_7-V_8	124	248	496	μA
			V_8-V_9	74	149	298	μA
			V_9-V_{10}	99	198	396	μA
Driver output current (V_{DD2} = 3.3 V)	I_{VOH1}	V_{OUT}=2.7 V, V_x=3.2 V[Note1] V_{DD1}=V_{DD2}=3.3 V			–0.16	–0.08	mA
	I_{VOL1}	V_{OUT}=0.6 V, V_x=0.1 V[Note1] V_{DD1}=V_{DD2}=3.3 V		0.07	0.14		mA
Driver output current (V_{DD2} = 5.0 V)	I_{VOH2}	V_{OUT}=4.4 V, V_x=4.9 V[Note1] V_{DD1}=3.3 V, V_{DD2}=5.0 V			–0.24	–0.12	mA
	I_{VOL2}	V_{OUT}=0.6 V, V_x=0.1 V[Note1] V_{DD1}=3.3 V, V_{DD2}=5.0 V		0.10	0.20		mA
Output voltage deviation	ΔV_O	V_{DD1}=3.3 V, V_{DD2}=3.3 V or 5.0 V, V_{OUT}= 0.5 V,1.5 V, 2.5 V[Note1]			±10	±20	mV
Output voltage deviation	ΔV_{P-P}	Input data			±5		mV
Output voltage range	V_O	Input data : 00H to 3FH		V_{SS2} + 0.1		V_{DD2} – 0.1	V
Dynamic logic current consumption	I_{DD1}	No load[Note2]			0.5	2.5	mA
Dynamic driver current consumption	I_{DD21}	No load, V_{DD2}=3.3 V[Note2]			3.0	10	mA
	I_{DD22}	No load, V_{DD2}=5.0 V[Note2]			3.0	10	mA

Notes 1. V_X is output voltage of analog output pins S_1 to S_{309}.
V_{OUT} is the voltage applied to analog output pins S_1 to S_{309}.

2. The STB cycle is specified at 31 μs and f_{CLK} = 16 MHz.

Switching Characteristics (T_A = –10 to +75 °C, V_{DD1} = 3.3 V ± 0.3 V, V_{DD2} = 3.3 V ± 0.3 V or 5.0 V ± 0.5 V, V_{SS1} = V_{SS2} = 0 V)

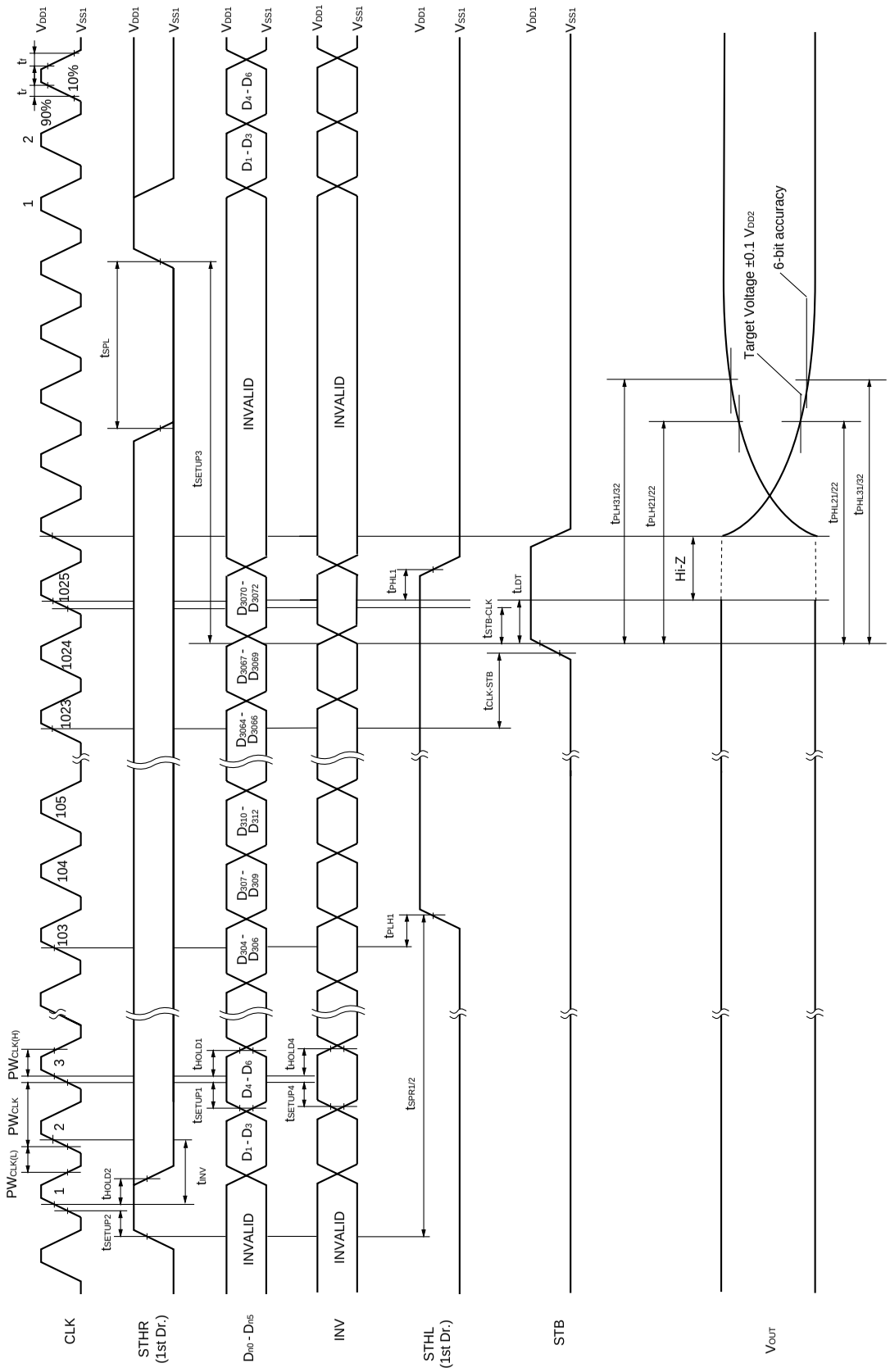
Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Start pulse delay time	t_{PLH1}	C_L = 15 pF			7	12	ns
	t_{PHL1}				7	12	ns
Driver output delay time	t_{PLH21}	V_{DD2}=3.3 V	V_O:0.1 V		2.6		μs
	t_{PLH31}	2 kΩ +75 pF x 2	→3.2 V		3.0	10	μs
	t_{PHL21}		V_O:3.2 V		2.4		μs
	t_{PHL31}		→0.1 V		3.2	10	μs
Driver output delay time	t_{PLH22}	V_{DD2}=5.0 V	V_O:0.1 V		2.2		μs
	t_{PLH32}	2 kΩ +75 pF x 2	→4.9 V		2.9	10	μs
	t_{PHL22}		V_O:4.9 V		2.6		μs
	t_{PHL32}		→0.1 V		3.6	10	μs
Input capacitance	C_{I1}	STHR(STHL), T_A=25 °C			10	20	pF
	C_{I2}	V_0-V_{10}, T_A = 25 °C			60	100	pF
	C_{I3}	STHR(STHL), other than V_0-V_{10}, T_A=25 °C			10	15	pF

Timing Requirements (T_A = –10 to +75 °C, V_{DD1} = 3.3 V ± 0.3 V, V_{SS1} = 0 V, t_r = t_f = 3.0 ns)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock pulse width	PW_{CLK}		18			ns
Clock pulse high period	$PW_{CLK (H)}$		4			ns
Clock pulse low period	$PW_{CLK (L)}$		4			ns
Data setup time	t_{SETUP1}		4			ns
Data hold time	t_{HOLD1}		0			ns
Start pulse setup time	t_{SETUP2}		4			ns
Start pulse hold time	t_{HOLD2}		0			ns
INV setup time	t_{SETUP4}		4			ns
INV hold time	t_{HOLD4}		0			ns
Start pulse low period	t_{SPL}		2			CLK
Start pulse rise time	t_{SPR1}	O_{sel}=H		100		CLK
	t_{SPR2}	O_{sel}=L		103		CLK
Final data timing	t_{SETUP3}		1			CLK
CLK-STB time	t_{INV}			1		CLK
STB-CLK time	t_{LDT}				1	CLK
Time between STB and start pulse	$t_{CLK-STB}$	CLK↑→STB↑	7			ns
STB-POL time	$t_{STB-CLK}$	STB↑ →CLK↑	7			ns

8. SWITCHING CHARACTERISTIC WAVEFORM(R,/L= H)

Unless otherwise specified, the input level is defined to V_{IH} = 0.7 V_{DD1}, V_{IL} = 0.3 V_{DD1}.



9. RECOMMENDED MOUNTING CONDITIONS

The following conditions must be met for mounting conditions of the μPD16640C.

For more details, refer to the **Semiconductor Device Mounting Technology Manual(C10535E).**

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD16640CN-xxx : TCP(TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350 °C, heating for 2 to 3 sec ; pressure 100g(per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100 °C ; pressure 3 to 8 kg/cm^2; time 3 to 5 sec. Real bonding 165 to 180 °C pressure 25 to 45 kg/cm^2 time 30 to 40secs(When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite,Ltd).

Caution To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Reference Documents

NEC Semiconductor Device Reliability/Quality Control System(C10983E)

Quality Grades to NEC's Semiconductor Devices(C11531E)

- **The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.**
- No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Corporation. NEC Corporation assumes no responsibility for any errors which may appear in this document.
- NEC Corporation does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from use of a device described herein or any other liability arising from use of such device. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Corporation or others.
- Descriptions of circuits, software, and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software, and information in the design of the customer's equipment shall be done under the full responsibility of the customer. NEC Corporation assumes no responsibility for any losses incurred by the customer or third parties arising from the use of these circuits, software, and information.
- While NEC Corporation has been making continuous effort to enhance the reliability of its semiconductor devices, the possibility of defects cannot be eliminated entirely. To minimize risks of damage or injury to persons or property arising from a defect in an NEC semiconductor device, customers must incorporate sufficient safety measures in its design, such as redundancy, fire-containment, and anti-failure features.
- NEC devices are classified into the following three quality grades:
  "Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.
  - Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots
  - Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)
  - Specific: Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

  The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

M7 98.8