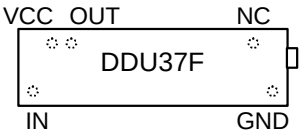
MECHANICALLY VARIABLE TTL DELAY LINE (SERIES DDU37F)

FEATURES

- Ideal for "Set and Forget" applications
- Multi-turn adjustment screw (approx. 40 turns)
- Input & output fully TTL interfaced & buffered (10 T^2L fan-out capability)
- **Resolution:** As low as 0.12ns
- **Minimum delay (T_{D0}):** 6ns typical
- **Output rise time:** 2ns typical
- **Min. input pulse width:** 20% of maximum delay
- **Power dissipation:** 230mW maximum
- **Operating temperature:** 0° to 70°C (Commercial)
  -55° to 125°C (Military)
- **Temperature coefficient:** 100 PPM/°C

PACKAGES



DDU37F-xx (Commercial)
DDU37F-xxM (Military)
xx = Dash number

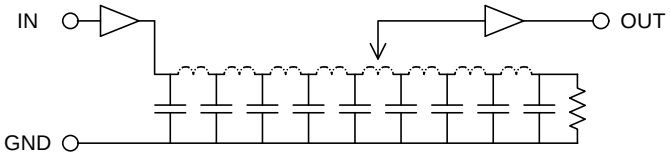
FUNCTIONAL DESCRIPTION

The DDU37F-series device is a mechanically variable, FAST-TTL interfaced delay line. The signal input (IN) is reproduced at the tap output (OUT), shifted by an amount which can be adjusted between T_{D0} and T_{D0}+ T_{DVAR}, where T_{DVAR} is given by the device dash number (See Table). The device operates from a single 5V supply and is TTL interfaced, capable of driving up to 10 TTL loads.

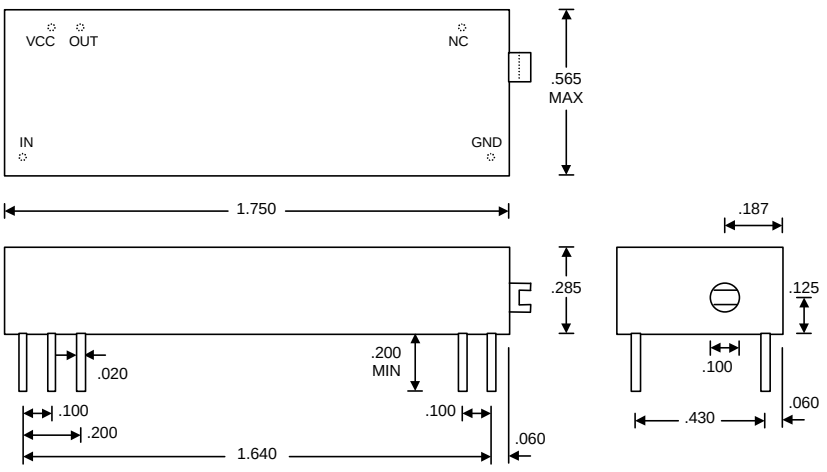
PIN DESCRIPTIONS

IN	Signal Input
OUT	Fixed Output
VCC	+5V
GND	Ground
NC	No connection

SERIES SPECIFICATIONS



Functional Diagram



Package Dimensions

DASH NUMBER SPECIFICATIONS

Part Number	T_{DVAR} (ns)
DDU37F-25	15
DDU37F-30	20
DDU37F-40	30
DDU37F-50	40
DDU37F-60	50
DDU37F-70	60
DDU37F-80	70
DDU37F-100	90
DDU37F-120	100
DDU37F-150	130
DDU37F-200	180

Note: Other delay times available on request

APPLICATION NOTES

HIGH FREQUENCY RESPONSE

The DDU37F tolerances are guaranteed for input pulse widths and periods greater than those specified in the test conditions. Although the device will function properly for pulse widths as small as 20% of the total delay and periods as small as 40% of the total delay (for a symmetric input), the delays may deviate from their values at low frequency. However, for a given input condition, the deviation will be repeatable from pulse to pulse. Contact technical support at Data Delay Devices if your application requires device testing at a specific input condition.

POWER SUPPLY BYPASSING

The DDU37F relies on a stable power supply to produce repeatable delays within the stated tolerances. A 0.1uf capacitor from VCC to GND, located as close as possible to the VCC pin, is recommended. A wide VCC trace and a clean ground plane should be used.

DEVICE SPECIFICATIONS

TABLE 1: ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{CC}	-0.3	7.0	V	
Input Pin Voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Storage Temperature	T_{STRG}	-55	150	C	
Lead Temperature	T_{LEAD}		300	C	10 sec

TABLE 2: DC ELECTRICAL CHARACTERISTICS

(0C to 70C, 4.75V to 5.25V)

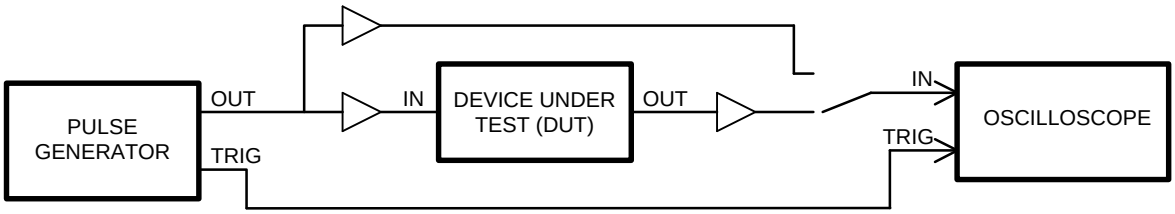
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
High Level Output Voltage	V_{OH}	2.5	3.4		V	V_{CC} = MIN, I_{OH} = MAX V_{IH} = MIN, V_{IL} = MAX
Low Level Output Voltage	V_{OL}		0.35	0.5	V	V_{CC} = MIN, I_{OL} = MAX V_{IH} = MIN, V_{IL} = MAX
High Level Output Current	I_{OH}			-1.0	mA	
Low Level Output Current	I_{OL}			20.0	mA	
High Level Input Voltage	V_{IH}	2.0			V	
Low Level Input Voltage	V_{IL}			0.8	V	
Input Clamp Voltage	V_{IK}			-1.2	V	V_{CC} = MIN, I_I = I_{IK}
Input Current at Maximum Input Voltage	I_{IHH}			0.1	mA	V_{CC} = MAX, V_I = 7.0V
High Level Input Current	I_{IH}			20	µA	V_{CC} = MAX, V_I = 2.7V
Low Level Input Current	I_{IL}			-0.6	mA	V_{CC} = MAX, V_I = 0.5V
Short-circuit Output Current	I_{OS}	-60		-150	mA	V_{CC} = MAX
Output High Fan-out				25	Unit	
Output Low Fan-out				12.5	Load	

DELAY LINE AUTOMATED TESTING

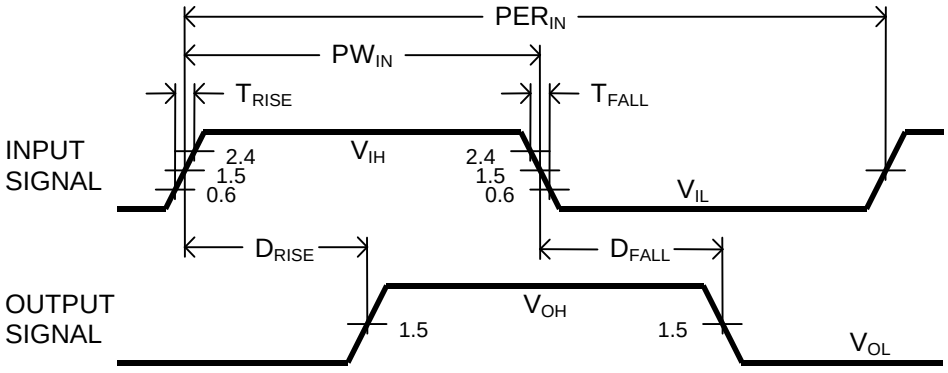
TEST CONDITIONS

INPUT:		**OUTPUT:**	
Ambient Temperature:	25°C ± 3°C	**Load:**	1 FAST-TTL Gate
Supply Voltage (Vcc):	5.0V ± 0.1V	**C_{load}:**	5pf ± 10%
Input Pulse:	High = 3.0V ± 0.1V Low = 0.0V ± 0.1V	**Threshold:**	1.5V (Rising & Falling)
Source Impedance:	50Ω Max.		
Rise/Fall Time:	3.0 ns Max. (measured between 0.6V and 2.4V)		
Pulse Width:	PW_{IN} = 1.5 x Total Delay		
Period:	PER_{IN} = 10 x Total Delay		

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.



Test Setup



Timing Diagram For Testing