RL78/G1A

RENESAS MCU

R01DS0151EJ0001
Rev.0.01
2011.12.26

Combines Multi-channel 12-Bit A/D Converter, True Low Power Platform (as low as 66 μA/MHz, and 0.57 μA for RTC + LVD), 1.6 V to 3.6 V operation, 16 to 64 Kbyte Flash, 41 DMIPS at 32 MHz

1. OUTLINE

1.1 Features

Ultra-Low Power Technology
- 1.6 V to 3.6 V operation from a single supply
- Stop (RAM retained): 0.23 μA, (LVD enabled): 0.31 μA
- Halt (RTC + LVD): 0.57 μA
- Snooze: T.B.D.
- Operating: 66 μA/MHz

16-bit RL78 CPU Core
- Delivers 41 DMIPS at maximum operating frequency of 32 MHz
- Instruction Execution: 86% of instructions can be executed in 1 to 2 clock cycles
- CISC Architecture (Harvard) with 3-stage pipeline
- Multiply Signed & Unsigned: 16 x 16 to 32-bit result in 1 clock cycle
- MAC: 16 x 16 to 32-bit result in 2 clock cycles
- 16-bit barrel shifter for shift & rotate in 1 clock cycle
- 1-wire on-chip debug function

Code Flash Memory
- Density: 16 KB to 64 KB
- Block size: 1 KB
- On-chip single voltage flash memory with protection from block erase/writing
- Self-programming with secure boot swap function and flash shield window function

Data Flash Memory
- Data Flash with background operation
- Data flash size: 4 KB
- Erase Cycles: 1 Million (typ.)
- Erase/programming voltage: 1.8 V to 3.6 V

RAM
- 2 KB to 4 KB size options
- Supports operands or instructions
- Back-up retention in all modes

High-speed On-chip Oscillator
- 32 MHz with +/– 1% accuracy over voltage (1.8 V to 3.6 V) and temperature (–20 °C to +85 °C)
- Pre-configured settings: 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 4 MHz & 1 MHz

Reset and Supply Management
- Power-on reset (POR) monitor/generator
- Low voltage detection (LVD) with 12 setting options (Interrupt and/or reset function)

Data Memory Access (DMA) Controller
- Up to 2 fully programmable channels
- Transfer unit: 8- or 16-bit

Multiple Communication Interfaces
- Up to 6 x I^2C master
- Up to 1 x I^2C multi-master
- Up to 6 x CSI/SPI (7-, 8-bit)
- Up to 3 x UART (7-, 8-, 9-bit)
- Up to 1 x LIN

Extended-Function Timers
- Multi-function 16-bit timers: Up to 8 channels
- Real-time clock (RTC): 1 channel (full calendar and alarm function with watch correction function)
- Interval Timer: 12-bit, 1 channel
- 15 kHz watchdog timer: 1 channel (window function)

Rich Analog
- ADC: Up to 28 channels, 12-bit resolution, 3.375 μs conversion time
- Supports 1.6 V
- Internal voltage reference (1.45 V)
- On-chip temperature sensor

Safety Features (IEC or UL 60730 compliance)
- Flash memory CRC calculation
- RAM parity error check
- RAM write protection
- SFR write protection
- Illegal memory access detection
- Clock stop/ frequency detection
- ADC self-test

General Purpose I/O
- 3.6 V tolerant, high-current (up to 20 mA per pin)
- Open-Drain, Internal Pull-up support

Operating Ambient Temperature
- Standard: –40 °C to +85 °C

Package Type and Pin Count
From 3 mm x 3 mm to 10 mm x 10 mm
QFP: 48, 64
QFN: 32, 48
LGA: 25
BGA: 64

○ ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/G1A			
			25 pins	32 pins	48 pins	64 pins
64 KB	4 KB	4 KB Note	R5F10E8E	R5F10EBE	R5F10EGE	R5F10ELE
48 KB	4 KB	3 KB	R5F10E8D	R5F10EBD	R5F10EGD	R5F10ELD
32 KB	4 KB	2 KB	R5F10E8C	R5F10EBC	R5F10EGC	R5F10ELC
16 KB	4 KB	2 KB	R5F10E8A	R5F10EBA	R5F10EGA	–

Note This is about 3 KB when the self-programming function and data flash function are used.

1.2 Ordering Information

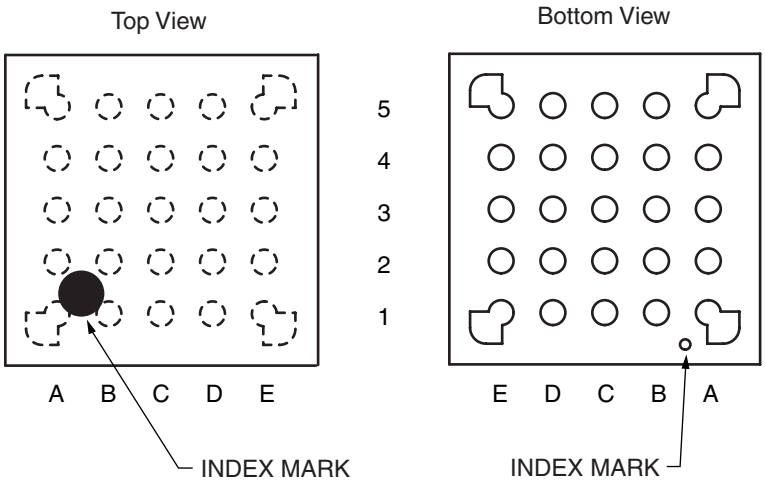
- **Flash memory version (lead-free product)**

Pin count	Package	Data flash	Part Number
25 pins	25-pin plastic FLGA (3 × 3)	Mounted	R5F10E8AALA, R5F10E8CALA, R5F10E8DALA, R5F10E8EALA
32 pins	32-pin plastic WQFN (fine pitch) (5 × 5)	Mounted	R5F10EBAANA, R5F10EBCANA, R5F10EBDANA, R5F10EBEANA
48 pins	48-pin plastic LQFP (fine pitch) (7 × 7)	Mounted	R5F10EGAAFB, R5F10EGCAFB, R5F10EGDAFB, R5F10EGEAFB
	48-pin plastic WQFN (7 × 7)	Mounted	R5F10EGAANA, R5F10EGCANA, R5F10EGDANA, R5F10EGEANA
64 pins	64-pin plastic LQFP (fine pitch) (10 × 10)	Mounted	R5F10ELCAFB, R5F10ELDAFB, R5F10ELEAFB
	64-pin plastic FBGA (4 × 4)	Mounted	R5F10ELCABG, R5F10ELDABG, R5F10ELEABG

1.3 Pin Configuration (Top View)

1.3.1 25-pin products

- 25-pin plastic FLGA (3 × 3)



	A	B	C	D	E	
5	P40/TOOL0	$\overline{\text{RESET}}$	P03/ANI16/ RxD1/TO00/ (KR1)	P23/ANI3/ (KR3)	AV_{SS}	5
4	P122/X2/ EXCLK	P137/INTP0	P02/ANI17/ TxD1/TI00/ (KR0)	P22/ANI2/ (KR2)	AV_{DD}	4
3	P121/X1	V_{DD}	P21/ANI1/ AV_{REFM}	P11/ANI20/ SI00/SDA00/ RxD0/ TOOLRxD	P10/ANI18/ $\overline{\text{SCK00}}$/SCL00	3
2	REGC	V_{SS}	P30/ANI27/ SCK11/SCL11/ INTP3	P51/ANI25/ SO11/INTP2	P50/ANI26/ SI11/SDA11 INTP1	2
1	P60/SCLA0	P61/SDAA0	P31/ANI29/TI03/ TO03/PCLBUZ0 /INTP4	P12/ANI21/ SO00/TxD0/ TOOLTxD	P20/ANI0/ AV_{REFP}	1
	A	B	C	D	E	

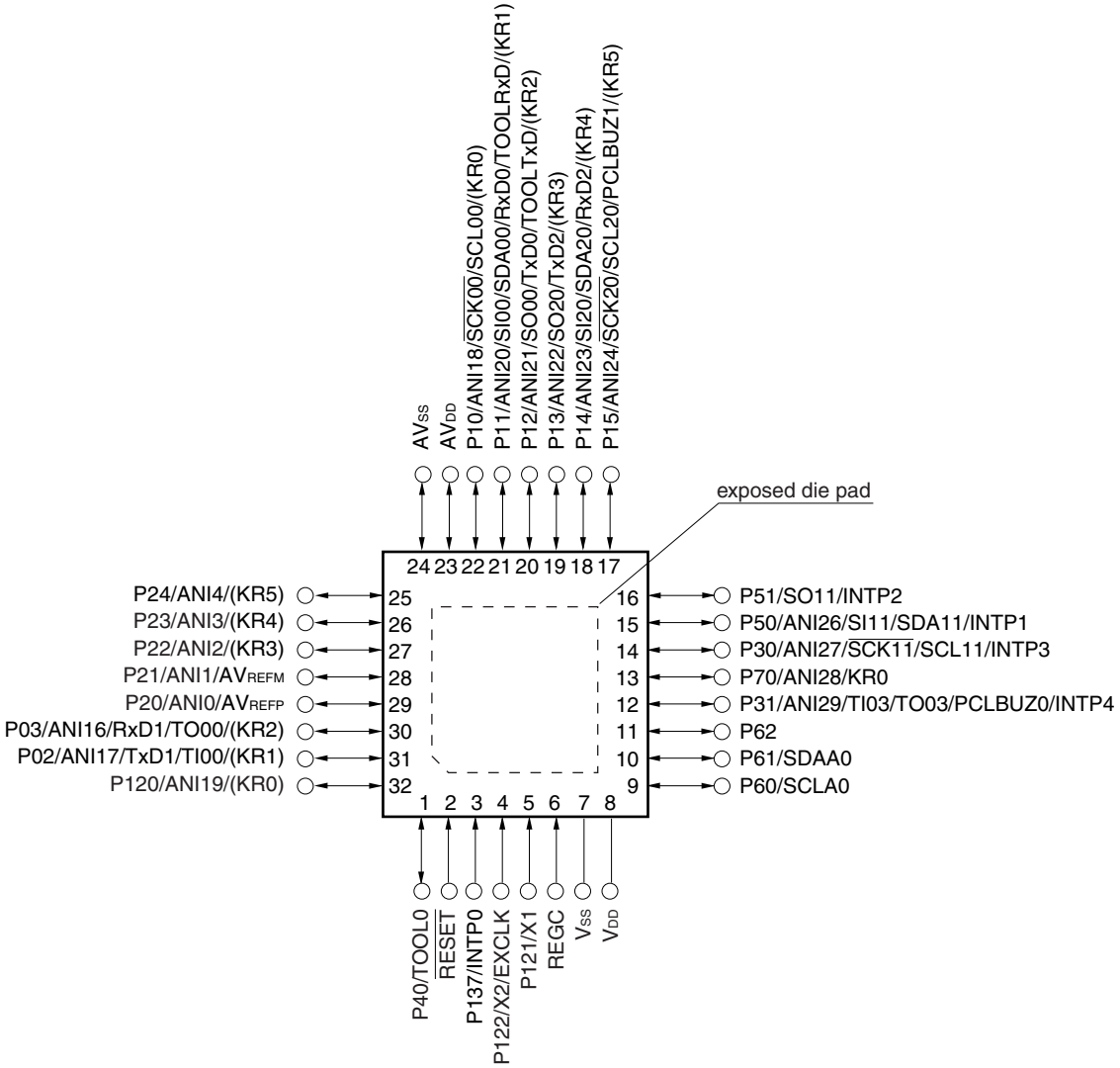
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.2 32-pin products

- 32-pin plastic WQFN (fine pitch) (5 × 5)



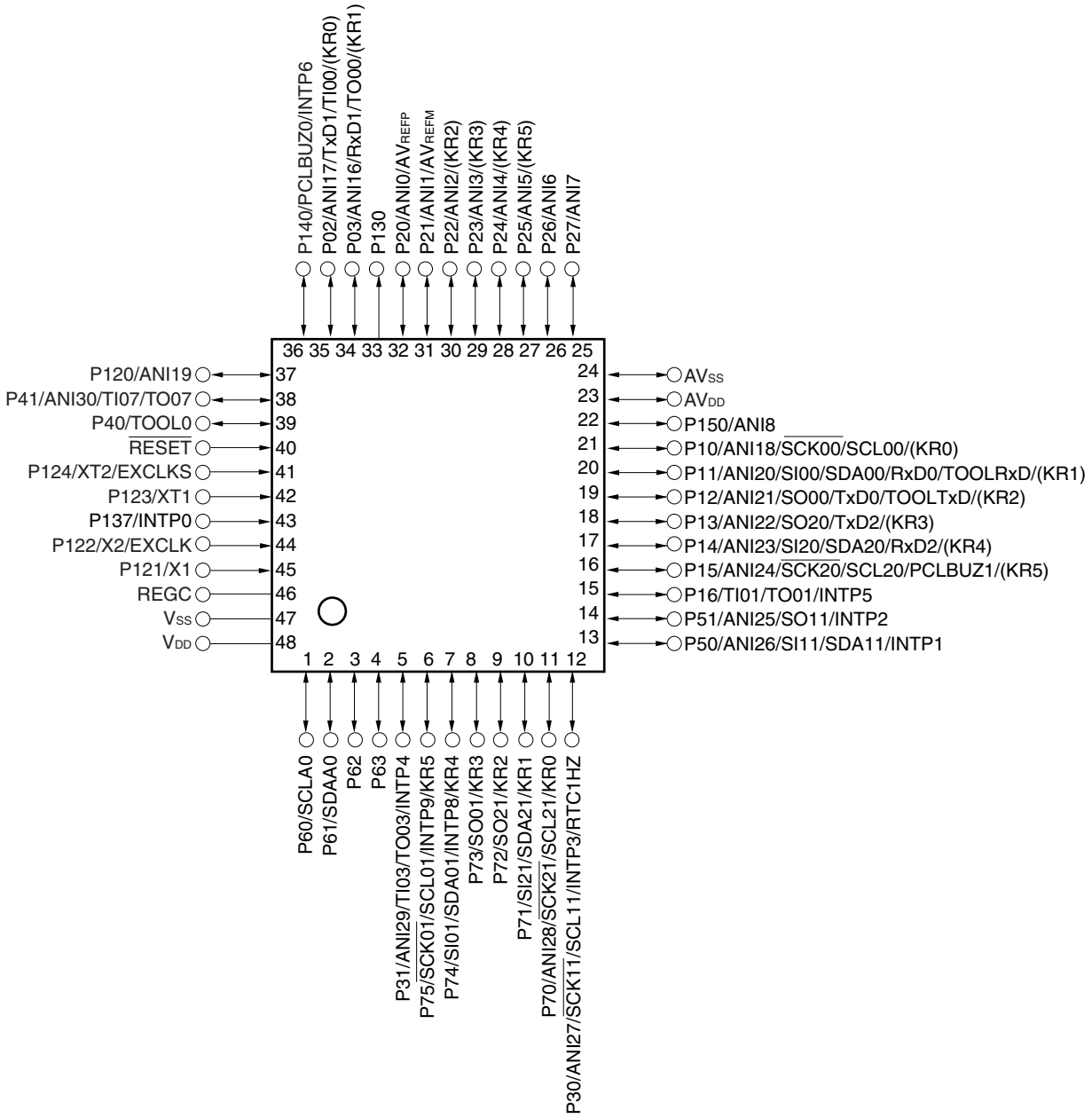
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.3 48-pin products

- 48-pin plastic LQFP (fine pitch) (7 × 7)

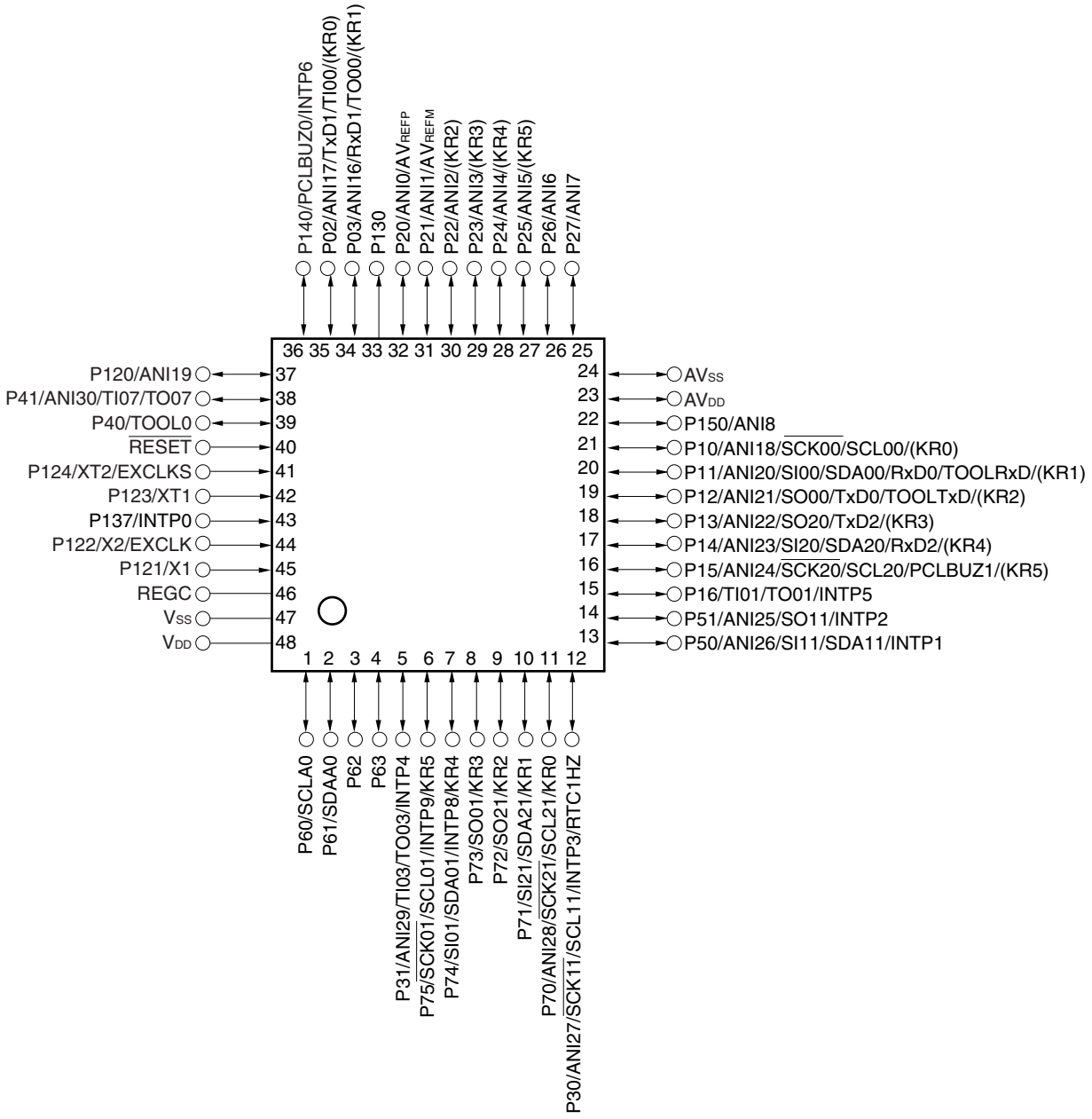


Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

- 48-pin plastic WQFN (7 × 7)



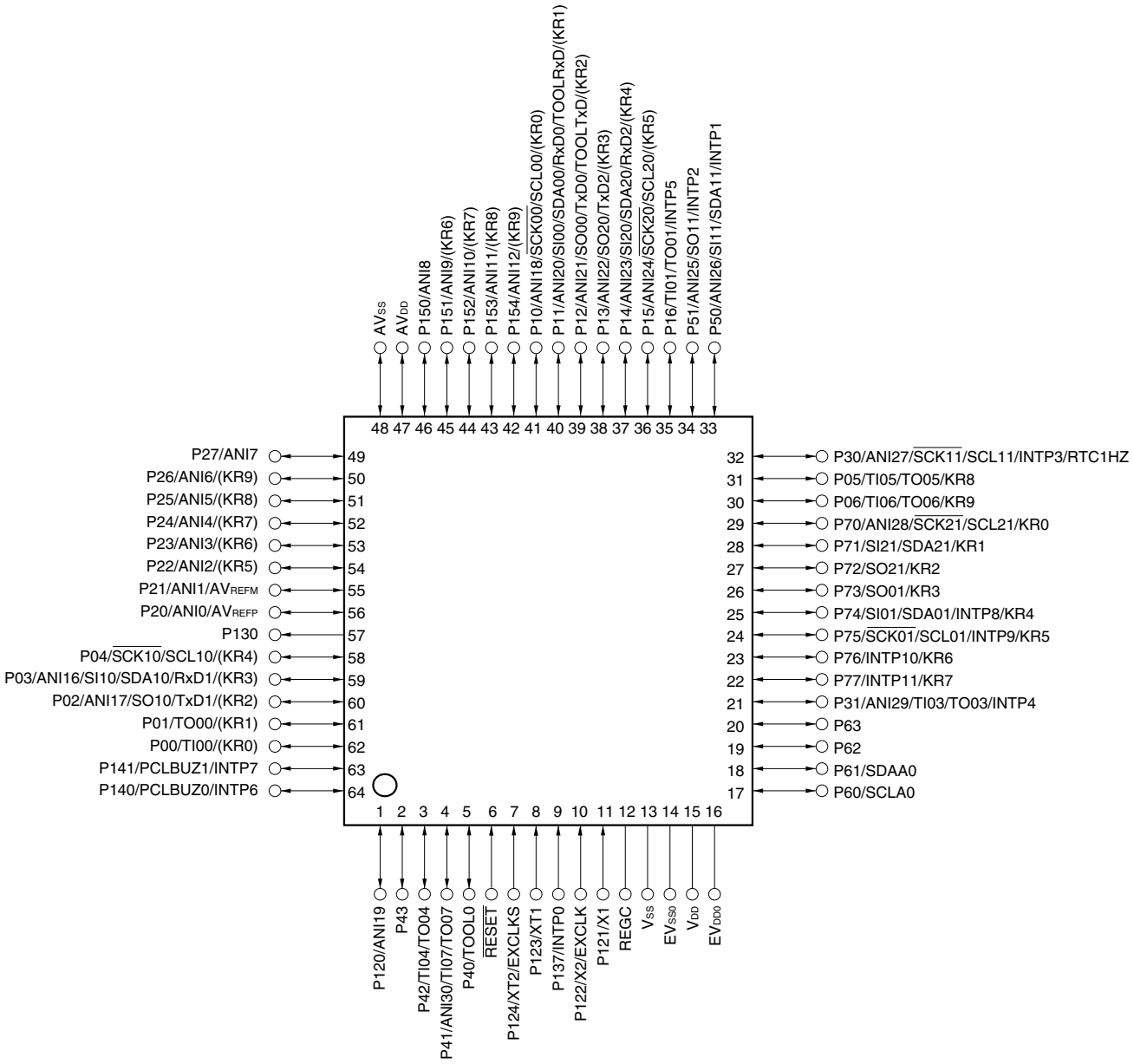
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.4 64-pin products

- 64-pin plastic LQFP (fine pitch) (10 × 10)



Cautions 1. Make EV_{SS0} pin the same potential as V_{SS} pin.

2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.

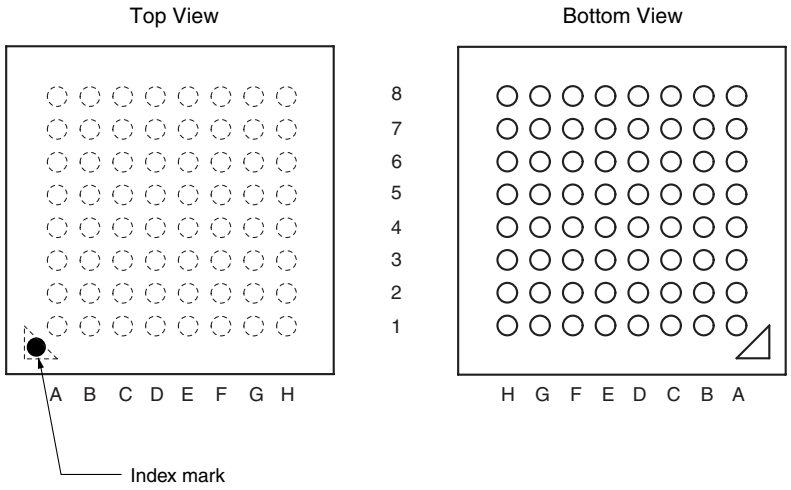
3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification.**

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS}0pins to separate ground lines.

3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

- 64-pin plastic FBGA (4 × 4)



Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
A1	P05/TI05/TO05/KR8	C1	P51/ANI25/SO11 /INTP2	E1	P153/ANI11/(KR8)	G1	AV_{DD}
A2	P30/ANI27/$\overline{SCK11}$ /SCL11/INTP3 /RTC1HZ	C2	P71/SI21/SDA21/KR1	E2	P154/ANI12/(KR9)	G2	P25/ANI5/(KR8)
A3	P70/ANI28/$\overline{SCK21}$ /SCL21/KR0	C3	P74/SI01/SDA01 /INTP8/KR4	E3	P10/ANI18/$\overline{SCK00}$ /SCL00/(KR0)	G3	P24/ANI4/(KR7)
A4	P75/$\overline{SCK01}$/SCL01 /INTP9/KR5	C4	P16/TI01/TO01/INTP5	E4	P11/ANI20/SI00 /SDA00/RxD0 /TOOLRxD/(KR1)	G4	P22/ANI2/(KR5)
A5	P77/INTP11/KR7	C5	P15/ANI24/$\overline{SCK20}$ /SCL20/(KR5)	E5	P03/ANI16/SI10 /SDA10/RxD1/(KR3)	G5	P130
A6	P61/SDAA0	C6	P63	E6	P41/ANI30/TI07/TO07	G6	P02/ANI17/SO10/TxD1 /(KR2)
A7	P60/SCLA0	C7	V_{SS}	E7	$\overline{RESET}$	G7	P00/TI00/(KR0)
A8	EV_{DD0}	C8	P121/X1	E8	P137/INTP0	G8	P124/XT2/EXCLKS
B1	P50/ANI26 /SI11 /SDA11/INTP1	D1	P13/ANI22/SO20 /TxD2/(KR3)	F1	P150/ANI8	H1	AV_{SS}
B2	P72/SO21/KR2	D2	P06/TI06/TO06/KR9	F2	P151/ANI9/(KR6)	H2	P27/ANI7
B3	P73/SO01/KR3	D3	P12/ANI21/SO00 /TxD0/TOOLTxD/(KR2)	F3	P152/ANI10/(KR7)	H3	P26/ANI6/(KR9)
B4	P76/INTP10/KR6	D4	P14/ANI23/SI20/ SDA20/RxD2/(KR4)	F4	P21/ANI1/AV_{REFM}	H4	P23/ANI3/(KR6)
B5	P31/ANI29/TI03/TO03 /INTP4	D5	P42/TI04/TO04	F5	P04/$\overline{SCK10}$/SCL10 /(KR4)	H5	P20/ANI0/AV_{REFP}
B6	P62	D6	P40/TOOL0	F6	P43	H6	P141/PCLBUZ1/INTP7
B7	V_{DD}	D7	REGC	F7	P01/TO00/(KR1)	H7	P140/PCLBUZ0/INTP6
B8	EV_{SS0}	D8	P122/X2/EXCLK	F8	P123/XT1	H8	P120/ANI19

Cautions 1. Make EV_{SS0} pin the same potential as V_{SS} pin.

2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.

3. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification.**

2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.

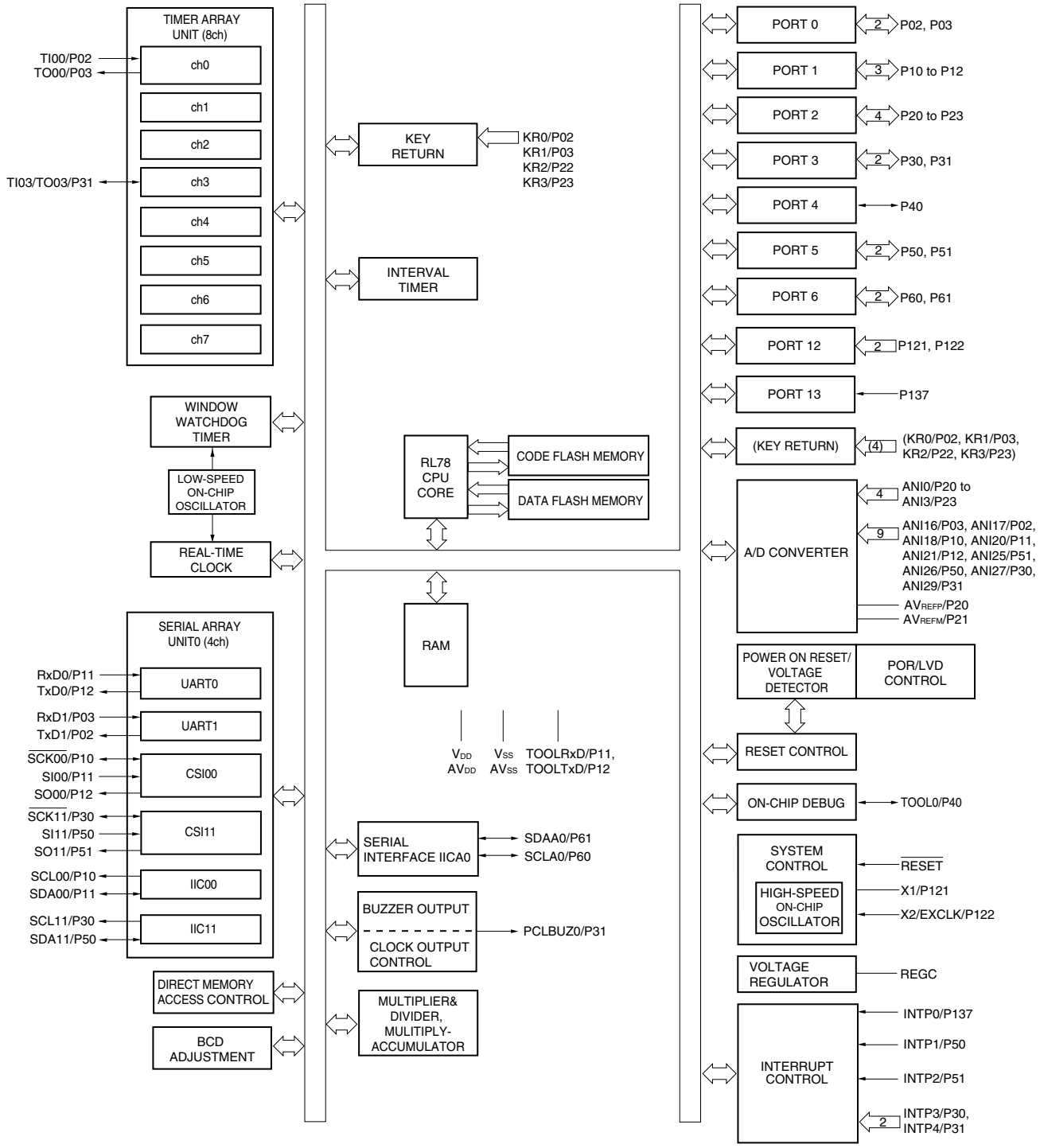
3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.4 Pin Identification

ANI0 to ANI12, ANI16 to ANI30:	Analog input
AV_{DD}:	Analog power supply
AV_{SS}:	Analog ground
AV_{REFM}:	A/D converter reference potential (− side) input
AV_{REFP}:	A/D converter reference potential (+ side) input
EV_{DD0}:	Power supply for port
EV_{SS0}:	Ground for port
EXCLK:	External clock input (main system clock)
EXCLKS:	External clock input (sub system clock)
INTP0 to INTP11:	External interrupt input
KR0 to KR9:	Key return
P00 to P06:	Port 0
P10 to P16:	Port 1
P20 to P27:	Port 2
P30, P31:	Port 3
P40 to P43:	Port 4
P50, P51:	Port 5
P60 to P63:	Port 6
P70 to P77:	Port 7
P120 to P124:	Port 12
P130, P137:	Port 13
P140, P141:	Port 14
P150 to P154:	Port 15
PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output
REGC:	Regulator capacitance
RESET:	Reset
RTC1HZ:	Real-time clock correction clock (1 Hz) output
RxD0 to RxD2:	Receive data
SCK00, SCK01, SCK10, SCK11, SCK20, SCK21:	Serial clock input/output
SCLA0, SCL00, SCL01, SCL10, SCL11, SCL20, SCL21:	Serial clock input/output
SDAA0, SDA00, SDA01, SDA10, SDA11, SDA20, SDA21:	Serial data input/output
SI00, SI01, SI10, SI11, SI20, SI21:	Serial data input
SO00, SO01, SO10, SO11, SO20, SO21:	Serial data output
TI00, TI01, TI03 to TI07:	Timer input
TO00, TO01, TO03 to TO07:	Timer output
TOOL0:	Data input/output for tool
TOOLRxD, TOOLTxD:	Data input/output for external device
TxD0 to TxD2:	Transmit data
V_{DD}:	Power supply
V_{SS}:	Ground
X1, X2:	Crystal oscillator (main system clock)
XT1, XT2:	Crystal oscillator (subsystem clock)

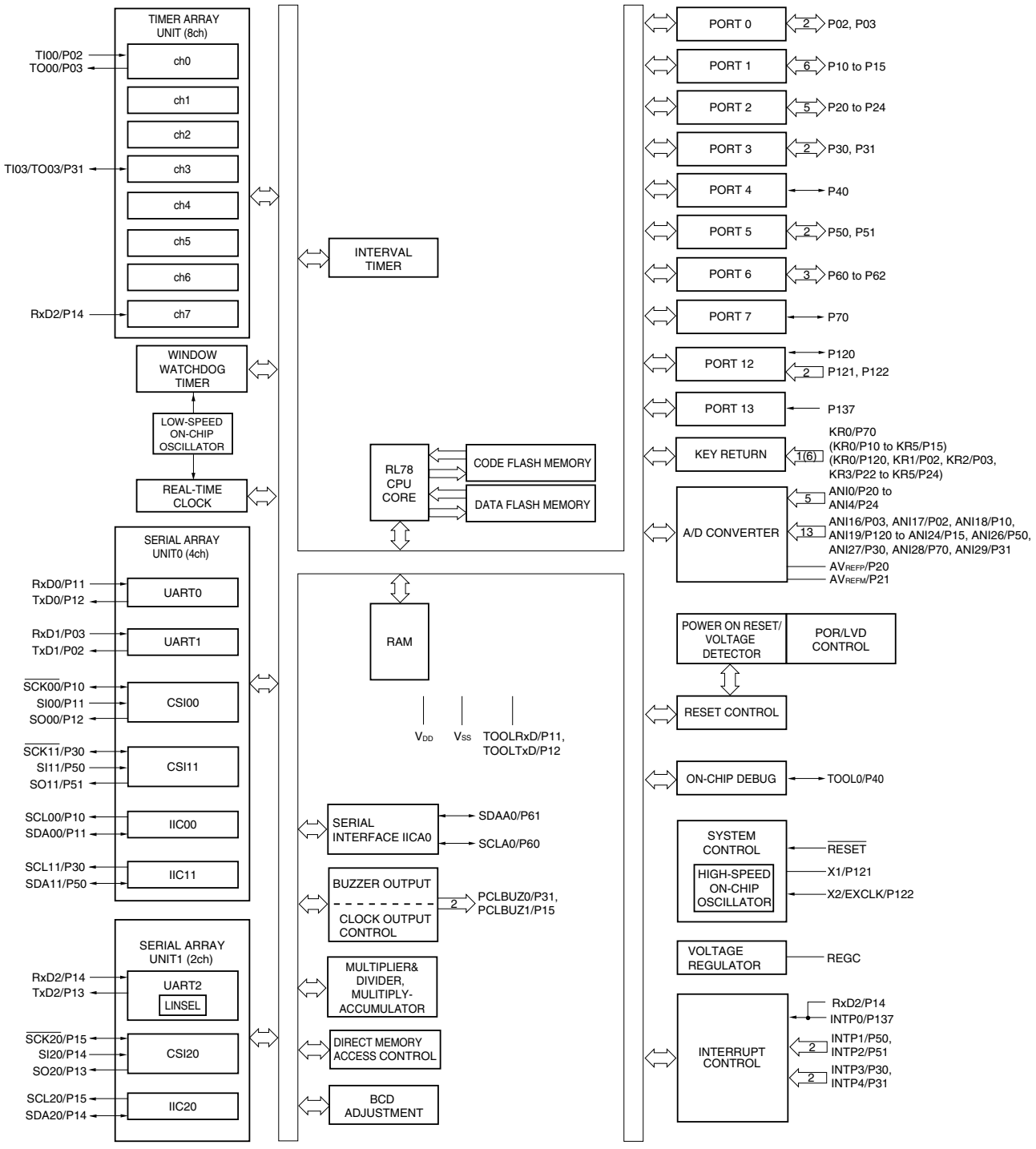
1.5 Block Diagram

1.5.1 25-pin products



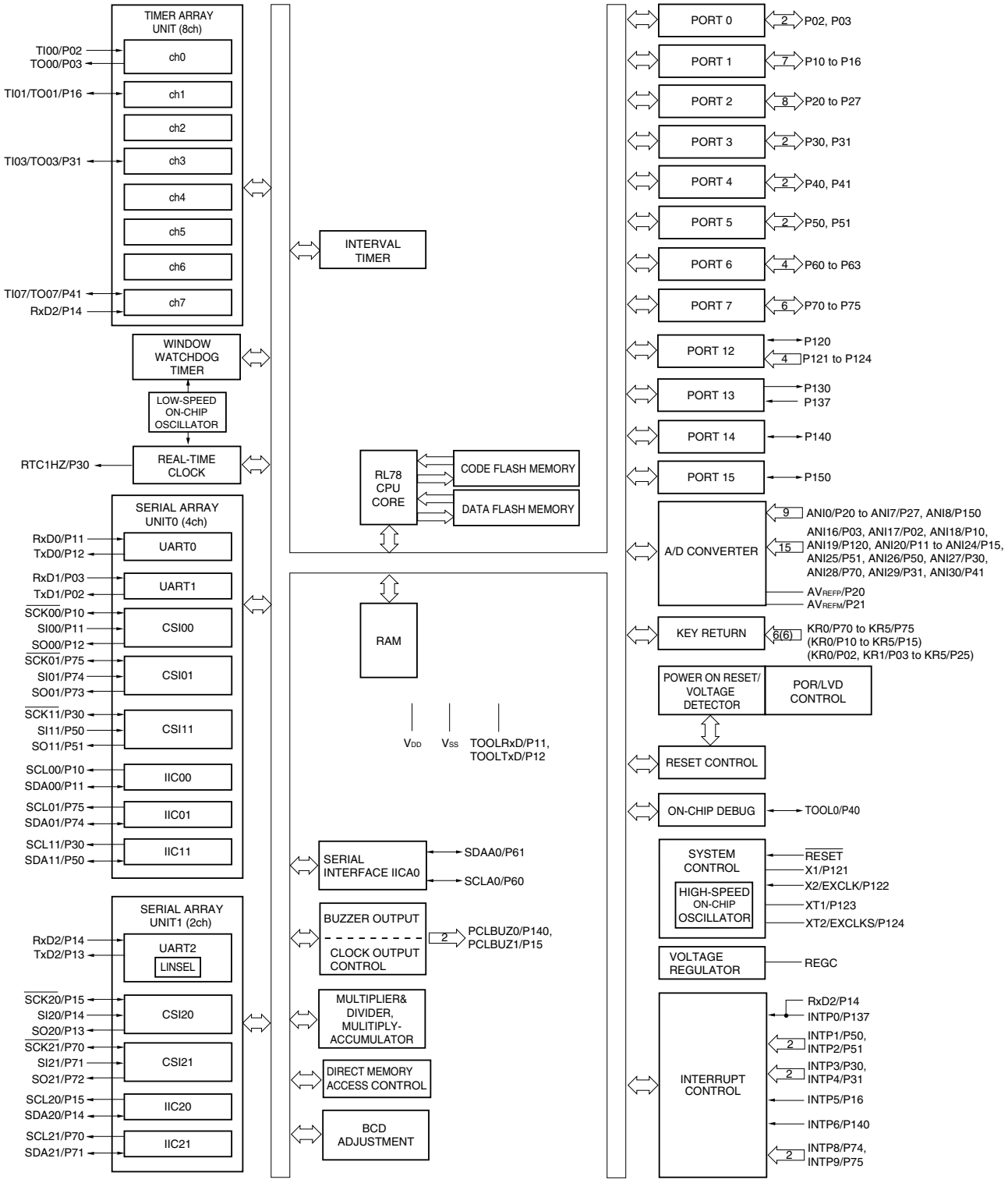
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.2 32-pin products



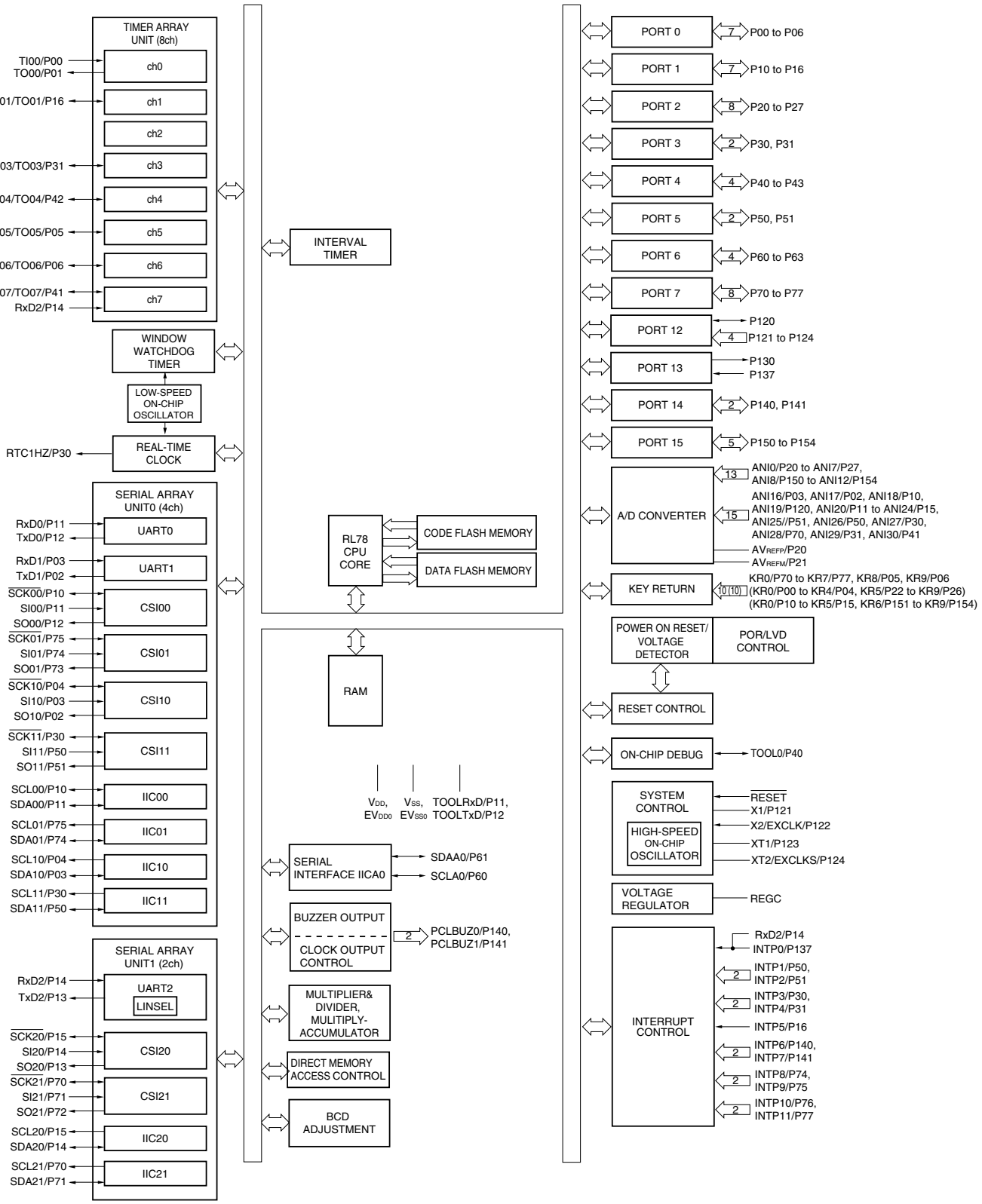
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.3 48-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.4 64-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.6 Outline of Functions

(1/2)

Item		25-pin	32-pin	48-pin	64-pin
		R5F10E8x	R5F10EBx	R5F10EGx	R5F10ELx
Code flash memory (KB)		16 to 64	16 to 64	16 to 64	32 to 64
Data flash memory (KB)		4	4	4	4
RAM (KB)		2 to 4Note1	2 to 4Note1	2 to 4Note1	2 to 4Note1
Memory space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: V_{DD} = 2.7 to 3.6 V, 1 to 8 MHz: V_{DD} = 1.8 to 2.7 V, 1 to 4 MHz: V_{DD} = 1.6 to 1.8 V			
	High-speed on-chip oscillator	High-speed operation: 1 to 32 MHz (V_{DD} = 2.7 to 3.6 V), High-speed operation: 1 to 16 MHz (V_{DD} = 2.4 to 3.6 V), Low-speed operation: 1 to 8 MHz (V_{DD} = 1.8 to 3.6 V), Low-voltage operation: 1 to 4 MHz (V_{DD} = 1.6 to 3.6 V)			
Subsystem clock		–		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz (TYP.): V_{DD} = 1.6 to 3.6 V	
Low-speed on-chip oscillator		15 kHz (TYP.): V_{DD} = 1.6 to 3.6 V			
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f_{IH} = 32 MHz operation)			
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)			
		–		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.			
I/O port	Total	19	26	42	56
	CMOS I/O	14	20	32	46
	CMOS input	3	3	5	5
	CMOS output	–	–	1	1
	N-ch open-drain I/O (6 V tolerance)	2	3	4	4
Timer	16-bit timer	8 channels			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	–		1 channel	
	Interval timer (IT)	1 channel			
	Timer output	2 channels (PWM outputs: 1 Note 2)		4 channels (PWM outputs: 3 Note 2)	7 channels (PWM outputs: 6 Note 2)
	RTC output	–		1 • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz or)	

Notes 1. In the case of the 4 KB, this is about 3 KB when the self-programming function and data flash function are used.

2. The number of outputs varies, depending on the setting.

(2/2)

Item		25-pin	32-pin	48-pin	64-pin
		R5F10E8x	R5F10EBx	R5F10EGx	R5F10ELx
Clock output/buzzer output		1	2	2	2
		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation)		• 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
8/12-bit resolution A/D converter		13 channels	18 channels	24 channels	28 channels
Serial interface		[25-pin products] • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel [32-pin products] • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 1 channel [48-pin products] • CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels • CSI: 1 channel/UART: 1 channel/simplified I^2C: 1 channel • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 2 channels [64-pin products] • CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I^2C: 2 channels			
	I^2C bus	1 channel	1 channel	1 channel	1 channel
Multiplier and divider/multiply-accumulator		• 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)			
DMA controller		2 channels			
Vectored interrupt sources	Internal	24	27	27	27
	External	6	6	10	13
Key interrupt		0 ch (4 ch) Note 1	1 ch (6 ch) Note 1	6 ch	10 ch
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note 2 • Internal reset by RAM parity error • Internal reset by illegal-memory access			
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.03 V • Power-down-reset: 1.50 ±0.03 V			
Voltage detector		1.63 V to 3.06 V (12 stages)			
On-chip debug function		Provided			
Power supply voltage		V_{DD} = 1.6 to 3.6 V			
Operating ambient temperature		T_A = −40 to +85 °C			

Notes 1. Can be used by the Peripheral I/O redirection register (PIOR).

2. The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS

Cautions 1. These specifications show target values, which may change after device evaluation.

2. The RL78/G1A has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

3. The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V_{DD}		−0.5 to +6.5	V
	EV_{DD0}	$EV_{DD0} \leq V_{DD}$	−0.5 to +6.5	V
	AV_{DD}	$AV_{DD0} \leq V_{DD}$	−0.5 to +4.6	V
	V_{SS}		−0.5 to +0.3	V
	EV_{SS0}		−0.5 to +0.3	V
	AV_{SS}		−0.5 to +0.3	V
REGC pin input voltage	V_{IREGC}	REGC	−0.3 to +2.8 and −0.3 to V_{DD} +0.3 Note 1	V
Input voltage	V_{I1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	−0.3 to EV_{DD0} +0.3 and −0.3 to V_{DD} +0.3 Note 2	V
	V_{I2}	P60 to P63 (N-ch open-drain)	−0.3 to +6.5	V
	V_{I3}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$	−0.3 to V_{DD} +0.3 Note 2	V
	V_{I4}	P20 to P27, P150 to P154	−0.3 to AV_{DD} +0.3 Note 3	V
Output voltage	V_{O1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P130, P140, P141	−0.3 to EV_{DD0} +0.3 Note 2	V
	V_{O2}	P20 to P27, P150 to P154	−0.3 to V_{DD} +0.3 Note 2	V
Analog input voltage	V_{AI1}	ANI16 to ANI30	−0.3 to EV_{DD0} +0.3 Note 2	V
	V_{AI2}	ANI0 to ANI12	−0.3 to AV_{DD} +0.3 Note 2	V

Notes 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum ratinwg of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Must be 4.6 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	I_{OH1}	Per pin	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	−40	mA
		Total of all pins −170 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	−70	mA
			P05, P06, P10 to P16, P30, P31, P50, P51, P70 to P77,	−100	mA
	I_{OH2}	Per pin	P20 to P27, P150 to P154	−0.1	mA
		Total of all pins		−1.3	mA
Output current, low	I_{OL1}	Per pin	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P130, P140, P141	40	mA
		Total of all pins 170 mA	P00 to P04, P40 to P43, P120, P130, P140, P141	70	mA
			P05, P06, P10 to P16, P30, P31, P50, P51, P60 to P63, P70 to P77	100	mA
	I_{OL2}	Per pin	P20 to P27, P150 to P154	0.4	mA
		Total of all pins		6.4	mA
Operating ambient temperature	T_A	In normal operation mode		−40 to +85	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

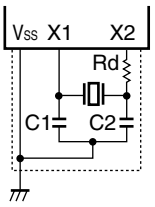
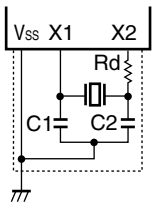
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

2.2 Oscillator Characteristics

2.2.1 Main system clock oscillator characteristics

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		X1 clock oscillation frequency (fx)Note	2.7 V ≤ V_{DD} ≤ 3.6 V	1.0		20.0	MHz
			1.8 V ≤ V_{DD} < 2.7 V	1.0		8.0	MHz
			1.6 V ≤ V_{DD} < 1.8 V	1.0		4.0	MHz
Crystal resonator		X1 clock oscillation frequency (fx)Note	2.7 V ≤ V_{DD} ≤ 3.6 V	1.0		20.0	MHz
			1.8 V ≤ V_{DD} < 2.7 V	1.0		8.0	MHz
			1.6 V ≤ V_{DD} < 1.8 V	1.0		4.0	MHz

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions 1. When using the X1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

2.2.2 On-chip oscillator characteristics

(T_A = –20 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Note	f_{IH}	1.8 V ≤ V_{DD} ≤ 3.6 V	32 MHz selected	31.68	32.00	32.32	MHz
			24 MHz selected	23.76	24.00	24.24	MHz
			16 MHz selected	15.84	16.00	16.16	MHz
			12 MHz selected	11.88	12.00	12.12	MHz
			8 MHz selected	7.92	8.00	8.08	MHz
			4 MHz selected	3.96	4.00	4.04	MHz
			1 MHz selected	0.99	1.00	1.01	MHz
		1.6 V ≤ V_{DD} < 1.8 V	32 MHz selected	30.40	32.00	33.60	MHz
			24 MHz selected	22.80	24.00	25.20	MHz
			16 MHz selected	15.20	16.00	16.80	MHz
			12 MHz selected	11.40	12.00	12.60	MHz
			8 MHz selected	7.60	8.00	8.40	MHz
			4 MHz selected	3.80	4.00	4.20	MHz
			1 MHz selected	0.95	1.00	1.05	MHz
Low-speed on-chip oscillator clock frequency	f_{IL}			12.75	15	17.25	kHz

(T_A = –40 to –20°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

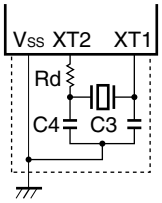
Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Note	f_{IH}	1.8 V ≤ V_{DD} ≤ 3.6 V	32 MHz selected	31.52	32.00	32.48	MHz
			24 MHz selected	23.64	24.00	24.36	MHz
			16 MHz selected	15.76	16.00	16.24	MHz
			12 MHz selected	11.82	12.00	12.18	MHz
			8 MHz selected	7.88	8.00	8.12	MHz
			4 MHz selected	3.94	4.00	4.06	MHz
			1 MHz selected	0.985	1.00	1.015	MHz
		1.6 V ≤ V_{DD} < 1.8 V	32 MHz selected	30.24	32.00	33.76	MHz
			24 MHz selected	22.68	24.00	25.32	MHz
			16 MHz selected	15.12	16.00	16.88	MHz
			12 MHz selected	11.34	12.00	12.66	MHz
			8 MHz selected	7.56	8.00	8.44	MHz
			4 MHz selected	3.78	4.00	4.22	MHz
			1 MHz selected	0.945	1.00	1.055	MHz
Low-speed on-chip oscillator clock frequency	f_{IL}			12.75	15	17.25	kHz

Note This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

2.2.3 Subsystem clock oscillator characteristics

(T_A = −40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Resonator	Recommended Circuit	Items	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		XT1 clock oscillation frequency (f_{XT})Note		32	32.768	35	kHz

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions 1. When using the XT1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the X1 oscillator. Particular care is therefore required with the wiring method when the XT1 clock is used.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = −40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	Per pin for P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	1.6 V ≤ EV_{DD0} ≤ 3.6 V			−10.0 [Note 2]	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty = 70%[Note 3])	2.7 V ≤ EV_{DD0} ≤ 3.6 V			−10.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			−5.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			−2.5	mA
		Total of P05, P06, P10 to P16, P30, P31, P50, P51, P70 to P77, (When duty = 70%[Note 3])	2.7 V ≤ EV_{DD0} ≤ 3.6 V			−19.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			−10.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			−5.0	mA
		Total of all pins (When duty = 70%[Note 3])	1.6 V ≤ EV_{DD0} ≤ 3.6 V			−29.0	mA
	I_{OH2}	Per pin for P20 to P27, P150 to P154	1.6 V ≤ AV_{DD} ≤ 3.6 V			−0.1[Note 2]	mA
		Total of all pins (When duty = 70%[Note 3])	1.6 V ≤ AV_{DD} ≤ 3.6 V			−1.3	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the EV_{DD0}, V_{DD} pins to an output pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor is 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 50% and I_{OH} = −10.0 mA

Total output current of pins = (−10.0 × 0.7)/(50 × 0.01) = −14.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Cautions 1. P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 do not output high level in N-ch open-drain mode.

2. Always use AV_{DD} pin with the same potential as the V_{DD} pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(T_A = −40 to +85°C, 1.6 V ≤ AV_{DD} ≤ 3.6 V, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low[Note 1]	I_{OL1}	Per pin for P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141				20.0[Note 2]	mA
		Per pin for P60 to P63				15.0[Note 2]	mA
		Total of P00 to P04, P40 to P43, P120, P130, P140, P141 (When duty = 70%[Note 3])	2.7 V ≤ EV_{DD0} ≤ 3.6 V			15.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			9.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			4.5	mA
		Total of P05, P06, P10 to P16, P30, P31, P50, P51, P60 to P63, P70 to P77 (When duty = 70%[Note 3])	2.7 V ≤ EV_{DD0} ≤ 3.6 V			35.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			20.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			10.0	mA
		Total of all pins (When duty = 70%[Note 3])				50.0	mA
	I_{OL2}	Per pin for P20 to P27, P150 to P154				0.4[Note 2]	mA
		Total of all pins (When duty = 70%[Note 3])	1.6 V ≤ AV_{DD} ≤ 3.6 V			5.2	mA

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS0} and V_{SS} pin.

2. However, do not exceed the total current value.

3. Specification under conditions where the duty factor is 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)

<Example> Where n = 50% and I_{OL} = 10.0 mA
Total output current of pins = (10.0 × 0.7)/(50 × 0.01) = 14.0 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Caution Always use AV_{DD} pin with the same potential as the V_{DD} pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(T_A = –40 to +85°C, 1.6 V ≤ AV_{DD} ≤ 3.6 V, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	Normal input buffer	0.8EV_{DD0}		EV_{DD0}	V
	V_{IH2}	P01, P03, P04, P10, P11, P13 to P16, P43	TTL input buffer 3.3 V ≤ EV_{DD0} < 3.6 V	2.0		EV_{DD0}	V
			TTL input buffer 1.6 V ≤ EV_{DD0} < 3.3 V	1.5		EV_{DD0}	V
	V_{IH3}	P20 to P27, P150 to P154		0.7AV_{DD}		AV_{DD}	V
	V_{IH4}	P60 to P63		0.7EV_{DD0}		6.0	V
	V_{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	Normal input buffer	0		0.2EV_{DD0}	V
	V_{IL2}	P01, P03, P04, P10, P11, P13 to P16, P43	TTL input buffer 3.3 V ≤ EV_{DD0} < 3.6 V	0		0.5	V
			TTL input buffer 1.6 V ≤ EV_{DD0} < 3.3 V	0		0.32	V
	V_{IL3}	P20 to P27, P150 to P154		0		0.3AV_{DD}	V
	V_{IL4}	P60 to P63		0		0.3EV_{DD0}	V
	V_{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2V_{DD}	V

Cautions 1. The maximum value of V_{IH} of pins P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 is EV_{DD0}, even in the N-ch open-drain mode.

2. Always use AV_{DD} pin with the same potential as the V_{DD} pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(T_A = −40 to +85°C, 1.6 V ≤ AV_{DD} ≤ 3.6 V, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	2.7 V ≤ EV_{DD0} ≤ 3.6 V, I_{OH1} = −2.0 mA	EV_{DD0} − 0.6			V
			1.8 V ≤ EV_{DD0} ≤ 3.6 V, I_{OH1} = −1.5 mA	EV_{DD0} − 0.5			V
			1.6 V ≤ EV_{DD0} < 3.6 V, I_{OH1} = −1.0 mA	EV_{DD0} − 0.5			V
	V_{OH2}	P20 to P27, P150 to P154	1.6 V ≤ AV_{DD} ≤ 3.6 V, I_{OH2} = −100 μA	AV_{DD} − 0.5			V
Output voltage, low	V_{OL1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P130, P140, P141	2.7 V ≤ EV_{DD0} ≤ 3.6 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V ≤ EV_{DD0} ≤ 3.6 V, I_{OL1} = 1.5 mA			0.4	V
			1.8 V ≤ EV_{DD0} ≤ 3.6 V, I_{OL1} = 0.6 mA			0.4	V
			1.6 V ≤ EV_{DD0} < 1.8 V, I_{OL1} = 0.3 mA			0.4	V
	V_{OL2}	P20 to P27, P150 to P154	1.6 V ≤ AV_{DD} ≤ 3.6 V, I_{OL2} = 400 μA			0.4	V
	V_{OL3}	P60 to P63	2.7 V ≤ EV_{DD0} ≤ 3.6 V, I_{OL3} = 3.0 mA			0.4	V
			1.8 V ≤ EV_{DD0} ≤ 3.6 V, I_{OL3} = 2.0 mA			0.4	V
			1.6 V ≤ EV_{DD0} < 1.8 V, I_{OL3} = 1.0 mA			0.4	V

Caution 1. P00, P02 to P04, P10 to P15, P43, P50, P71, and P74 do not output high level in N-ch open-drain mode.

2. Always use AV_{DD} pin with the same potential as the V_{DD} pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(T_A = −40 to +85°C, 1.6 V ≤ AV_{DD} ≤ 3.6 V, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P63, P70 to P77, P120, P140, P141	V_I = EV_{DD0}				1	μA
	I_{LIH2}	P20 to P27, P137, P150 to P154, $\overline{RESET}$	V_I = V_{DD}				1	μA
	I_{LIH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{DD}	In input port or external clock input			1	μA
				In resonator connection			10	μA
	I_{LIH4}	P20 to P27, P150 to P154	V_I = AV_{DD}				1	μA
Input leakage current, low	I_{LIL1}	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P60 to P67, P70 to P77, P120, P140, P141	V_I = EV_{SS0}				−1	μA
	I_{LIL2}	P20 to P27, P137, P150 to P154, $\overline{RESET}$	V_I = V_{SS}				−1	μA
	I_{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V_I = V_{SS}	In input port or external clock input			−1	μA
				In resonator connection			−10	μA
	I_{LIL4}	P20 to P27, P150 to P154	V_I = AV_{SS}				−1	μA
On-chip pull-up resistance	R_U	P00 to P06, P10 to P16, P30, P31, P40 to P43, P50, P51, P70 to P77, P120, P140, P141	V_I = EV_{SS0}, In input port		10	20	100	kΩ

Caution Always use AV_{DD} pin with the same potential as the V_{DD} pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

2.3.2 Supply current characteristics

(T_A = −40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) (1/2)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current	I_{DD1} Note 1	Operating mode	High-speed operation Note 5	f_{IH} = 32 MHz Note 3	Basic operation	V_{DD} = 3.0 V		2.1		mA
					Normal operation	V_{DD} = 3.0 V		4.6	7.0	mA
				f_{IH} = 24 MHz Note 3	Normal operation	V_{DD} = 3.0 V		3.7	5.5	mA
				f_{IH} = 16 MHz Note 3	Normal operation	V_{DD} = 3.0 V		2.7	4.0	mA
			Low-speed operation Note 5	f_{IH} = 8 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.2	1.8	mA
						V_{DD} = 2.0 V		1.2	1.8	mA
			Low-voltage operation Note 5	f_{IH} = 4 MHz Note 3	Normal operation	V_{DD} = 3.0 V		1.2	1.7	mA
						V_{DD} = 2.0 V		1.2	1.7	mA
			High-speed operation Note 5	f_{MX} = 20 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		3.0	4.6	mA
						Resonator connection		3.2	4.8	mA
				f_{MX} = 10 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.9	2.7	mA
						Resonator connection		1.9	2.7	mA
			Low-speed operation Note 5	f_{MX} = 8 MHz Note 2, V_{DD} = 3.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	mA
				f_{MX} = 8 MHz Note 2, V_{DD} = 2.0 V	Normal operation	Square wave input		1.1	1.7	mA
						Resonator connection		1.1	1.7	mA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 4 T_A = −40°C	Normal operation	Square wave input		4.1		μA
						Resonator connection		4.2		μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +25°C	Normal operation	Square wave input		4.1	4.9	μA
						Resonator connection		4.2	5.0	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +50°C	Normal operation	Square wave input		4.2	5.5	μA
						Resonator connection		4.3	5.6	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +70°C	Normal operation	Square wave input		4.2	6.3	μA
						Resonator connection		4.3	6.4	μA
				f_{SUB} = 32.768 kHz Note 4 T_A = +85°C	Normal operation	Square wave input		4.8	7.7	μA
						Resonator connection		4.9	7.8	μA

(**Notes** and **Remarks** are listed on the next page.)

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.

2. When high-speed on-chip oscillator and subsystem clock are stopped.

3. When high-speed system clock and subsystem clock are stopped.

4. When high-speed on-chip oscillator and high-speed system clock are stopped. When real-time counter and watchdog timer is stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

High speed operation: V_{DD} = 2.7 V to 3.6 V@1 MHz to 32 MHz, V_{DD} = 2.4 V to 3.6 V@1 MHz to 16 MHz
Low speed operation: V_{DD} = 1.8 V to 3.6 V@1 MHz to 8 MHz
Low voltage operation: V_{DD} = 1.6 V to 3.6 V@1 MHz to 4 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V) (2/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	High-speed operation Note 7	f_{IH} = 32 MHz Note 4	V_{DD} = 3.0 V		0.54	1.63	mA
				f_{IH} = 24 MHz Note 4	V_{DD} = 3.0 V		0.44	1.28	mA
				f_{IH} = 16 MHz Note 4	V_{DD} = 3.0 V		0.40	1.00	mA
			Low-speed operation Note 7	f_{IH} = 8 MHz Note 4	V_{DD} = 3.0 V		260	530	μA
					V_{DD} = 2.0 V		260	530	μA
			Low-voltage operation Note 7	f_{IH} = 4 MHz Note 4	V_{DD} = 3.0 V		420	640	μA
					V_{DD} = 2.0 V		420	640	μA
			High-speed operation Note 7	f_{MX} = 20 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.28	1.00	mA
					Resonator connection		0.45	1.17	mA
				f_{MX} = 10 MHz Note 3, V_{DD} = 3.0 V	Square wave input		0.19	0.60	mA
					Resonator connection		0.26	0.67	mA
			Low-speed operation Note 7	f_{MX} = 8 MHz Note 3, V_{DD} = 3.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	μA
				f_{MX} = 8 MHz Note 3, V_{DD} = 2.0 V	Square wave input		95	330	μA
					Resonator connection		145	380	μA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5 T_A = –40°C	Square wave input		0.25		μA
					Resonator connection		0.44		μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +25°C	Square wave input		0.30	0.57	μA
					Resonator connection		0.49	0.76	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +50°C	Square wave input		0.33	1.17	μA
					Resonator connection		0.52	1.36	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +70°C	Square wave input		0.36	1.97	μA
					Resonator connection		0.55	2.16	μA
				f_{SUB} = 32.768 kHz Note 5 T_A = +85°C	Square wave input		0.97	3.37	μA
					Resonator connection		1.16	3.56	μA
	I_{DD3} Note 6	STOP mode	T_A = –40°C				0.18		μA
			T_A = +25°C				0.23	0.50	μA
			T_A = +50°C				0.26	1.10	μA
			T_A = +70°C				0.29	1.90	μA
			T_A = +85°C				0.90	3.30	μA

(**Notes** and **Remarks** are listed on the next page.)

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

Notes 1. Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator and subsystem clock are stopped.

4. When high-speed system clock and subsystem clock are stopped.

5. When operating real-time clock (RTC) and setting ultra-low current consumption (AMPHS1 = 1). When high-speed on-chip oscillator and high-speed system clock are stopped. When watchdog timer is stopped. The values below the MAX. column include the leakage current.

6. When high-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. When watchdog timer is stopped. The values below the MAX. column include the leakage current.

7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

High speed operation: V_{DD} = 2.7 V to 3.6 V@1 MHz to 32 MHz, V_{DD} = 2.4 V to 3.6 V@1 MHz to 16 MHz
Low speed operation: V_{DD} = 1.8 V to 3.6 V@1 MHz to 8 MHz
Low voltage operation: V_{DD} = 1.6 V to 3.6 V@1 MHz to 4 MHz

Remarks 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

2. fIH: High-speed on-chip oscillator clock frequency

3. fSUB: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is T_A = 25°C

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
RTC operating current	I_{RTC} Notes 1, 2	f_{SUB} = 32.768 kHz	Real-time clock operation		0.02		μA
			Interval timer operation		0.02		
Watchdog timer operating current	I_{WDT} Notes 2, 3	f_{IL} = 15 kHz			0.22		μA
A/D converter operating current	I_{ADC} Note 4	Reference power supply is other than the internal reference voltage, AV_{DD} = 3.6 V	ANI0 to ANI12		460	1090	μA
			ANI16 to ANI30		400	950	μA
		Reference power supply is the internal reference voltage, AV_{DD} = 3.6 V	ANI0 to ANI12, ANI16 to ANI30		400	950	μA
Temperature sensor operating current	I_{TMPS}				75		μA
LVD operating current	I_{LVI} Note 5				0.08		μA
BGO operating current	I_{BGO} Note 6				2.50	12.20	mA

Notes 1. Current flowing only to the real-time clock (excluding the operating current of the XT1 oscillator). The TYP. value of the current value of the RL78/G1A is the sum of the TYP. values of either I_{DD1} or I_{DD2}, and I_{RTC}, when the real-time clock operates in operation mode or HALT mode. The I_{DD1} and I_{DD2} MAX. values also include the real-time clock operating current. However, I_{DD2} subsystem clock operation includes the operational current of the real-time clock.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

3. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78/G1A is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when f_{CLK} = f_{SUB} when the watchdog timer operates in STOP mode.

4. Current flowing only to the A/D converter. The current value of the RL78/G1A is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

5. Current flowing only to the LVD circuit. The current value of the RL78/G1A is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVD circuit operates in the Operating, HALT or STOP mode.

6. Current flowing only to the BGO. The current value of the RL78/G1A is the sum of I_{DD1} or I_{DD2} and I_{BGO} when the BGO operates in an operation mode.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. f_{CLK}: CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is T_A = 25°C

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

2.4 AC Characteristics

2.4.1 Basic operation

(T_A = –40 to +85°C, 1.6 V ≤ AV_{DD} ≤ 3.6 V, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	High-speed main mode	2.7 V ≤ V_{DD} ≤ 3.6 V	0.03125		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			Low voltage main mode	1.6 V ≤ V_{DD} ≤ 3.6 V	0.25		1	μs
			Low-speed main mode	1.8 V ≤ V_{DD} ≤ 3.6 V	0.125		1	μs
		Subsystem clock (f_{SUB}) operation		1.8 V ≤ V_{DD} ≤ 3.6 V	28.5	30.5	31.3	μs
		In the self programming mode	High-speed main mode	2.7 V ≤ V_{DD} ≤ 3.6 V	0.03125		1	μs
				2.4 V ≤ V_{DD} < 2.7 V	0.0625		1	μs
			Low voltage main mode	1.8 V ≤ V_{DD} ≤ 3.6 V	0.25		1	μs
			Low-speed main mode	1.8 V ≤ V_{DD} ≤ 3.6 V	0.125		1	μs
External main system clock frequency	f_{EX}	2.7 V ≤ V_{DD} ≤ 3.6 V			1.0		20.0	MHz
		1.8 V ≤ V_{DD} < 2.7 V			1.0		8.0	MHz
		1.6 V ≤ V_{DD} < 1.8 V			1.0		4.0	MHz
	f_{EXS}				32		35	kHz
External main system clock input high-level width, low-level width	t_{EXH}, t_{EXL}	2.7 V ≤ V_{DD} ≤ 3.6 V			24			ns
		1.8 V ≤ V_{DD} < 2.7 V			60			ns
		1.6 V ≤ V_{DD} < 1.8 V			120			ns
	t_{EXHS}, t_{EXLS}				13.7			μs
TI00, TI01, TI03 to TI07 input high-level width, low-level width	t_{TIH}, t_{TIL}				1/f_{MCK}+10			ns[Note]
TO00, TO01, TO03 to TO07 output frequency	f_{TO}	High-speed main mode		2.7 V ≤ EV_{DD0} ≤ 3.6 V			8	MHz
				1.8 V ≤ EV_{DD0} < 2.7 V			4	MHz
				1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
		Low voltage main mode		1.6 V ≤ EV_{DD0} ≤ 3.6 V			2	MHz
		Low-speed main mode		1.8 V ≤ EV_{DD0} ≤ 3.6 V			4	MHz
				1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
PCLBUZ0, PCLBUZ1 output frequency	f_{PCL}	High-speed main mode		2.7 V ≤ EV_{DD0} ≤ 3.6 V			8	MHz
				1.8 V ≤ EV_{DD0} < 2.7 V			4	MHz
				1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
		Low voltage main mode		1.8 V ≤ EV_{DD0} ≤ 3.6 V			4	MHz
				1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
		Low-speed main mode		1.8 V ≤ EV_{DD0} ≤ 3.6 V			4	MHz
				1.6 V ≤ EV_{DD0} < 1.8 V			2	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0		1.6 V ≤ V_{DD} ≤ 3.6 V	1			μs
		INTP1 to INTP11		1.6 V ≤ EV_{DD0} ≤ 3.6 V	1			μs
Key interrupt input low-level width	t_{KR}	KR0 to KR9		1.8 V ≤ EV_{DD0} ≤ 3.6 V, 1.8 V ≤ AV_{DD} ≤ 3.6 V	250			ns
				1.6 V ≤ EV_{DD0} < 1.8 V, 1.6 V ≤ AV_{DD} < 1.8 V	1			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}				10			μs

(**Note, Caution** and **Remark** are listed on the next page.)

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

Note The following conditions are required for low voltage interface when $EV_{DD0} < V_{DD}$
$1.8\ V \leq EV_{DD0} < 2.7\ V$: MIN. 125 ns
$1.6\ V \leq EV_{DD0} < 1.8\ V$: MIN. 250 ns

Caution Always use AV_{DD} pin with the same potential as the V_{DD} pin.

Remark f_{MCK}: Timer array unit operation clock frequency
(Operation clock to be set by the CKS0n bit of timer mode register 0n (TMR0n). n: Channel number (n = 0 to 7))

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

2.5 Peripheral Functions Characteristics

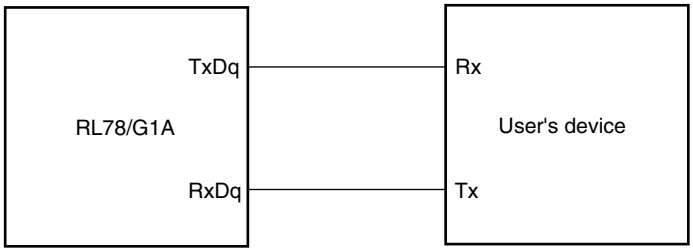
2.5.1 Serial array unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)

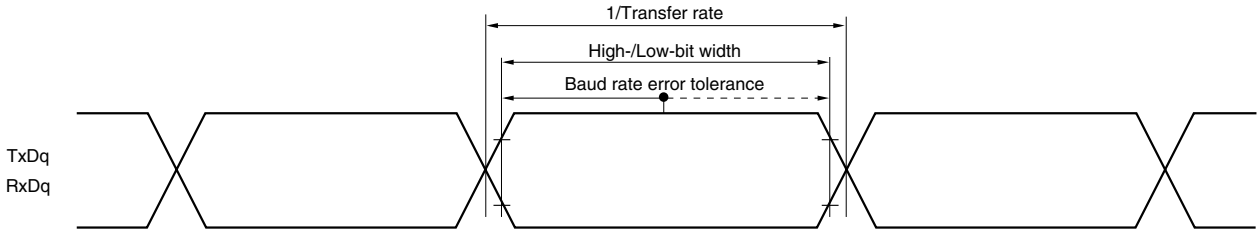
(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate Note 1					f_{MCK}/6 Note 2	bps
		Theoretical value of the maximum transfer rate f_{CLK} = 32 MHz, f_{MCK} = f_{CLK}			5.3	Mbps

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Notes 1. Transfer rate in the SNOOZE mode is max. 9600 bps, min. 4800 bps.

2. The following conditions are required for low voltage interface when EV_{DD0} < V_{DD}.

2.4 V ≤ EV_{DD0} < 2.7 V : MAX. 2.6 Mbps

1.8 V ≤ EV_{DD0} < 2.4 V : MAX. 1.3 Mbps

1.6 V ≤ EV_{DD0} < 1.8 V : MAX. 0.6 Mbps

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

2. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(2) During communication at same potential (CSI mode) (master mode (f_{MCK}/2), $\overline{SCKp}$... internal clock output)

(T_A = –40 to +85°C, 2.7 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	83.3 Note 1			ns
$\overline{SCKp}$ high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	t_{KCY1}/2 – 10			ns
SIp setup time (to $\overline{SCKp}$↑) Note 2	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	33 Note 5			ns
SIp hold time (from $\overline{SCKp}$↑) Note 3	t_{KSI1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	10			ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 4	t_{KSO1}	C = 20 pF Note 6			10	ns

Notes 1. The value must also be 2/f_{CLK} or more.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. Using the f_{MCK} within 24 MHz.

6. C is the load capacitance of the $\overline{SCKp}$ and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. This specification is valid only when CSI00's peripheral I/O redirect function is not used.

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM numbers (g = 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(3) During communication at same potential (CSI mode) (master mode (f_{MCK}/4), $\overline{SCKp}$... internal clock output)

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	125 Note 1			ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V	250 Note 1			ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	500 Note 1			ns
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	1000 Note 1			ns
$\overline{SCKp}$ high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	t_{KCY1}/2 – 18			ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V	t_{KCY1}/2 – 38			ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	t_{KCY1}/2 – 50			ns
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	t_{KCY1}/2 – 100			ns
SIp setup time (to $\overline{SCKp}$↑) Note 2	t_{SIK1}	2.7 V ≤ EV_{DD0} ≤ 3.6 V	38			ns
		2.4 V ≤ EV_{DD0} ≤ 3.6 V	75			ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V	150			ns
		1.6 V ≤ EV_{DD0} ≤ 3.6 V	300			ns
SIp hold time (from $\overline{SCKp}$↑) Note 3	t_{KSI1}		19			ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 4	t_{KSO1}	C = 30 pF Note 5			25	ns

Notes 1. The value must also be 4/f_{CLK} or more.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. C is the load capacitance of the $\overline{SCKp}$ and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. This specification is valid only when CSI00's peripheral I/O redirect function is not used.

2. p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2), g: PIM and POM numbers (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(4) During communication at same potential (CSI mode) (slave mode, $\overline{SCKp}$... external clock input)
(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time Note 5	t_{KCY2}	2.7 V ≤ EV_{DD0} < 3.6 V	16 MHz < f_{MCK}	8/f_{MCK}			ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}			ns
		1.8 V ≤ EV_{DD0} < 2.7 V	16 MHz < f_{MCK}	8/f_{MCK}			ns
			f_{MCK} ≤ 16 MHz	6/f_{MCK}			ns
		1.6 V ≤ EV_{DD0} < 1.8 V		6/f_{MCK}			ns
$\overline{SCKp}$ high-/low-level width	t_{KH2}, t_{KL2}	1.6 V ≤ EV_{DD0}≤ 3.6 V		t_{KCY2}/2			ns
SIp setup time (to $\overline{SCKp}$↑) Note 1	t_{SIK2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V		50			ns
		1.8 V ≤ EV_{DD0} < 2.7 V		80			ns
		1.6 V ≤ EV_{DD0} < 1.8 V		160			ns
SIp hold time (from $\overline{SCKp}$↑) Note 2	t_{KSI2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V		1/f_{MCK}+31			ns
		1.8 V ≤ EV_{DD0} < 2.7 V		1/f_{MCK}+31			ns
		1.6 V ≤ EV_{DD0} < 1.8 V		1/f_{MCK}+ 250			ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 3	t_{KSO2}	C = 30 pF Note 4	2.7 V ≤ EV_{DD0} < 3.6 V			2/f_{MCK}+44	ns
			2.4 V ≤ EV_{DD0} < 2.7 V			2/f_{MCK}+75	ns
			1.8 V ≤ EV_{DD0} < 2.4 V			2/f_{MCK}+110	ns
			1.6 V ≤ EV_{DD0} < 1.8 V			2/f_{MCK}+220	ns

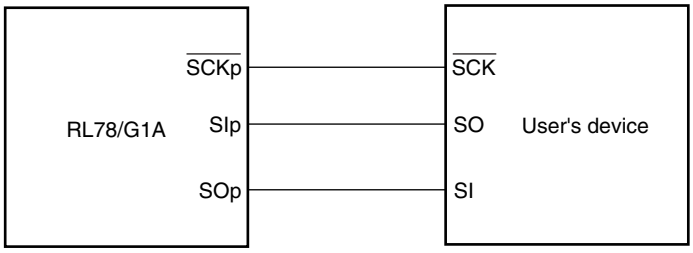
Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
4. C is the load capacitance of the SOp output lines.
5. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

Caution Select the TTL input buffer for the SIp pin and $\overline{SCKp}$ pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

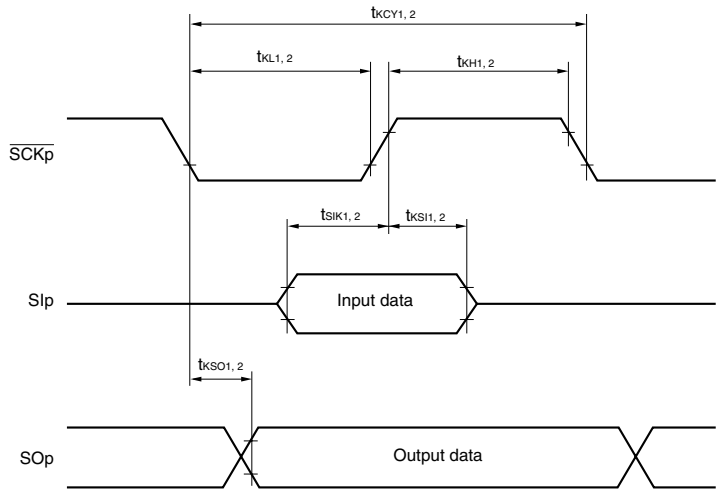
Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 2),
g: PIM number (g = 0, 1)
2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

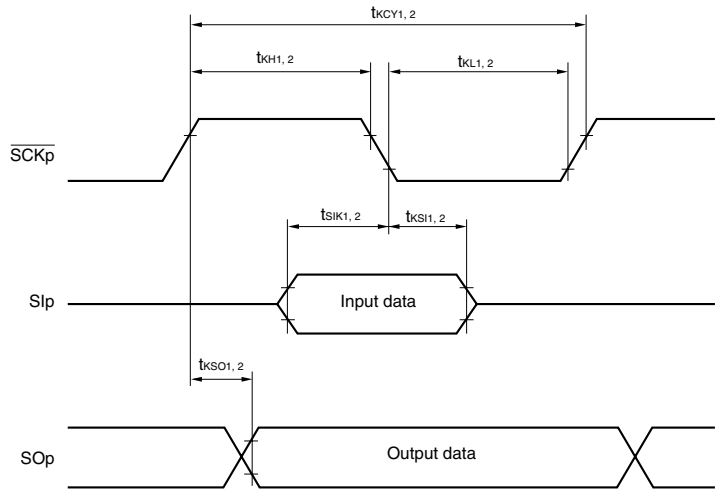
CSI mode connection diagram (during communication at same potential)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remarks 1. p: CSI number (p = 00, 01, 10, 11, 20, 21)

2. m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(5) During communication at same potential (simplified I^2C mode)

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

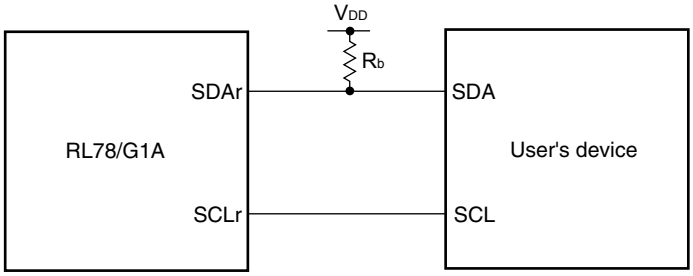
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ		1000	kHz
		1.8 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ		400	kHz
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ		300	kHz
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ		250	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	475		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	1150		ns
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		ns
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	475		ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	1150		ns
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1550		ns
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1850		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 85 Note		ns
		1.8 V ≤ EV_{DD} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 145 Note		ns
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK} + 230 Note		ns
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	1/f_{MCK} + 290 Note		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	ns
		1.8 V ≤ EV_{DD0} ≤ 3.6 V, C_b = 100 pF, R_b = 3 kΩ	0	355	ns
		1.8 V ≤ EV_{DD0} < 2.7 V, C_b = 100 pF, R_b = 5 kΩ	0	405	ns
		1.6 V ≤ EV_{DD0} < 1.8 V, C_b = 100 pF, R_b = 5 kΩ	0	405	ns

Note Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

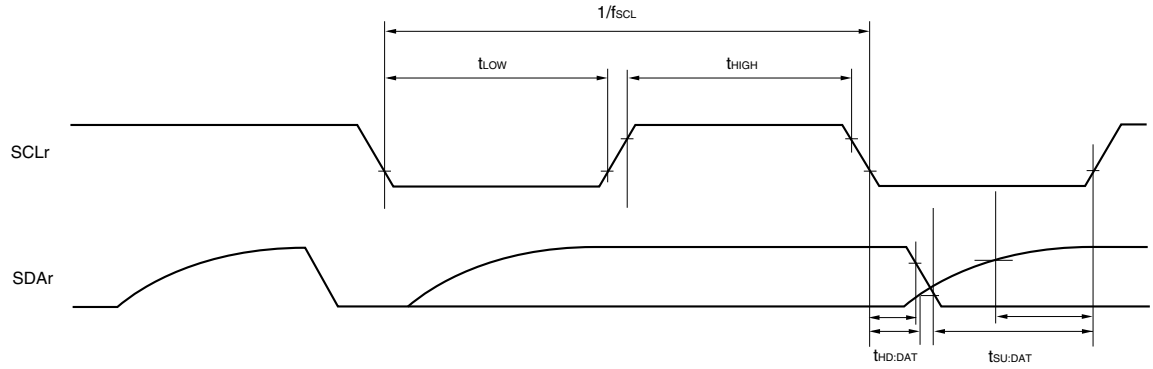
(**Caution** and **Remarks** are listed on the next page.)

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

Simplified I²C mode mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

Remarks 1. R_b[Ω]:Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

2. r: IIC number (r = 00, 01, 10, 11, 20, 21), g: PIM number (g = 0, 1), h: POM number (h = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10, 11)

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(6) Communication at different potential (2.5 V) (UART mode) (dedicated baud rate generator output) (1/2)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate		reception	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V				$f_{MCK}/6$ Note 1	bps
				Theoretical value of the maximum transfer rate f_{CLK} = 32 MHz, f_{MCK} = f_{CLK}			5.3	Mbps
			1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V				$f_{MCK}/6$ Notes 1 to 3	bps
				Theoretical value of the maximum transfer rate f_{CLK} = 8 MHz, f_{MCK} = f_{CLK}			1.3	Mbps

Notes 1. Transfer rate in the SNOOZE mode : MAX. 9600 bps, MIN. 4800 bps

2. Use it with $EV_{DD0} \geq V_b$.

3. The following conditions are required for low voltage interface when $EV_{DD0} < V_{DD}$.

2.4 V ≤ EV_{DD0} < 2.7 V : MAX. 2.6 Mbps

1.8 V ≤ EV_{DD0} < 2.4 V : MAX. 1.3 Mbps

1.6 V ≤ EV_{DD0} < 1.8 V : MAX. 0.6 Mbps

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. V_b[V]: Communication line voltage

2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10, 11)

4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in UART mode.

2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V: V_{IH} = 1.5 V, V_{IL} = 0.32 V

5. UART2 cannnot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(6) Communication at different potential (2.5 V) (UART mode) (dedicated baud rate generator output) (2/2)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Transfer rate		transmission	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V				**Notes 1, 2**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 2.7 kΩ, V_b = 2.3 V			1.2 Note 5	Mbps
			1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V				**Notes 1, 4, 5**	bps
				Theoretical value of the maximum transfer rate C_b = 50 pF, R_b = 5.5 kΩ, V_b = 1.6 V			0.43 Note 6	Mbps

Notes 1. Transfer rate in the SNOOZE mode : MAX. 9600 bps, MIN. 4800 bps

2. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD0} < 3.6 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

3. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 2 above to calculate the maximum transfer rate under conditions of the customer.

4. Use it with $EV_{DD0} \geq V_b$.

5. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 1.8 V ≤ EV_{DD0} < 3.3 V and 1.6 V ≤ V_b ≤ 2.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [\%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

6. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 7 above to calculate the maximum transfer rate under conditions of the customer.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. R_b[Ω]:Communication line (TxDq) pull-up resistance,
C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage

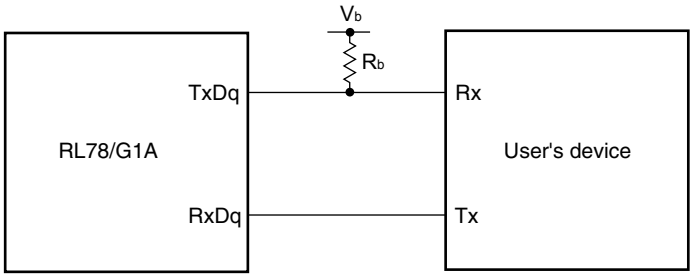
2. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10, 11))

4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in UART mode.
$2.7\ V \leq EV_{DD0} < 3.6\ V$, $2.3\ V \leq V_b \leq 2.7\ V$: $V_{IH} = 2.0\ V$, $V_{IL} = 0.5\ V$
$1.8\ V \leq EV_{DD0} < 3.3\ V$, $1.6\ V \leq V_b \leq 2.0\ V$: $V_{IH} = 1.5\ V$, $V_{IL} = 0.32\ V$

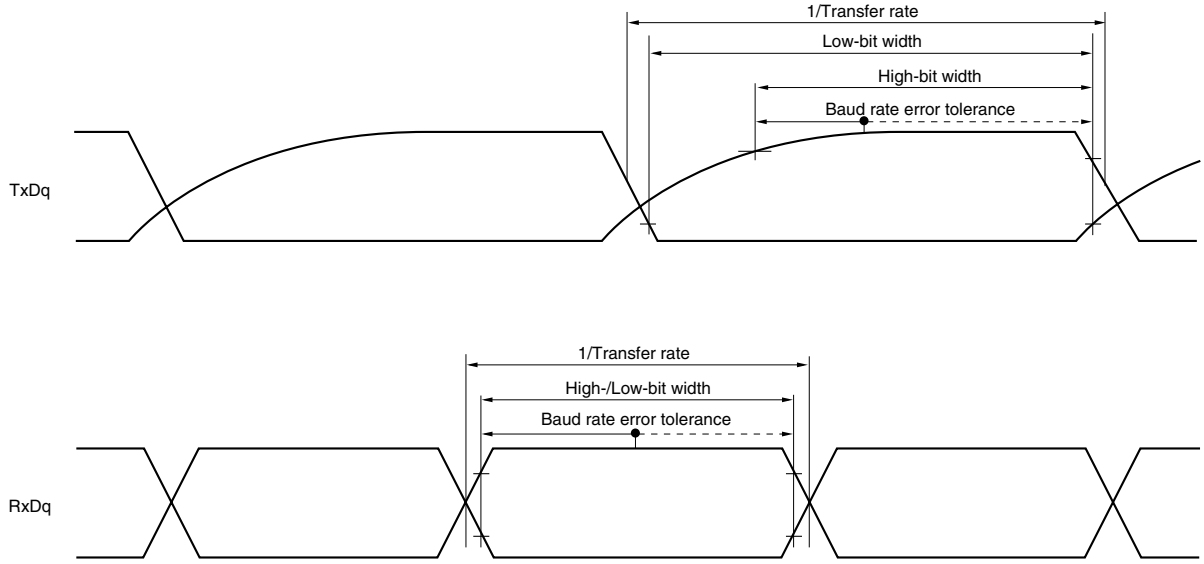
5. UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

UART mode connection diagram (during communication at different potential)



Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

UART mode bit width (during communication at different potential) (reference)



Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. UART2 cannot communicate at different potentia when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

2. $R_b[\Omega]$:Communication line (TxDq) pull-up resistance, $V_b[V]$: Communication line voltage

3. q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(7) Communication at different potential (2.5 V) (f_{MCK}/2) (CSI mode) (master mode, $\overline{SCKp}$... internal clock output)

(T_A = –40 to +85°C, 2.7 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY1}	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	300 Note 1			ns
$\overline{SCKp}$ high-level width	t_{KH1}	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 120			ns
$\overline{SCKp}$ low-level width	t_{KL1}	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 10			ns
SIp setup time (to $\overline{SCKp}$↑) Note 2	t_{SIK1}	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	121			ns
SIp hold time (from $\overline{SCKp}$↑) Note 2	t_{KSI1}	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	10			ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 2	t_{KSO1}	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			130	ns
SIp setup time (to $\overline{SCKp}$↓) Note 3	t_{SIK1}	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	33			ns
SIp hold time (from $\overline{SCKp}$↓) Note 3	t_{KSI1}	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	10			ns
Delay time from $\overline{SCKp}$↑ to SOp output Note 3	t_{KSO1}	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			10	ns

Notes 1. The value must also be 2/f_{CLK} or more.

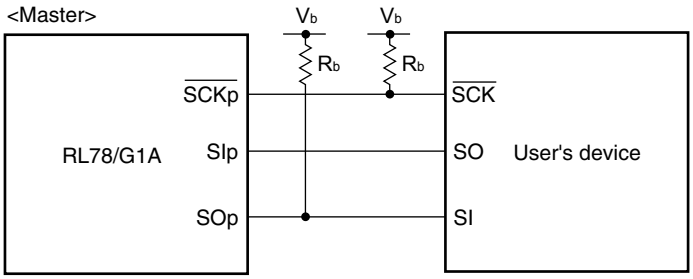
2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

3. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

(**Caution** and **Remark** are listed on the next page.)

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

CSI mode connection diagram (during communication at different potential)



Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. R_b[Ω]:Communication line ($\overline{SCKp}$, SOp) pull-up resistance, C_b[F]: Communication line ($\overline{SCKp}$, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 1)

3. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.

$2.7\ V \leq EV_{DD0} < 3.6\ V$, $2.3\ V \leq V_b \leq 2.7\ V$: $V_{IH} = 2.0\ V$, $V_{IL} = 0.5\ V$

4. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00)

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(8) Communication at different potential (2.5 V) (f_{MCK}/4) (CSI mode) (master mode, $\overline{SCKp}$... internal clock output) (1/2)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time	t_{KCY1}	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	500 Note			ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	1150 Note			ns
$\overline{SCKp}$ high-level width	t_{KH1}	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 170			ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	t_{KCY1}/2 – 458			ns
$\overline{SCKp}$ low-level width	t_{KL1}	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	t_{KCY1}/2 – 18			ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	t_{KCY1}/2 – 50			ns

Note The value must also be 4/f_{CLK} or more.

Cautions 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

2. Use it with EV_{DD0} ≥ V_b.

Remarks 1. R_b[Ω]:Communication line ($\overline{SCKp}$, SOp) pull-up resistance, C_b[F]: Communication line ($\overline{SCKp}$, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00, 01, 10, 20), m: Unit number , n: Channel number (mn = 00, 01, 02, 10), g: PIM and POM number (g = 0, 1)

3. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.

2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V: V_{IH} = 1.5 V, V_{IL} = 0.32 V

4. CSI01, CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(8) Communication at different potential (2.5 V) (f_{MCK}/4) (CSI mode) (master mode, $\overline{SCKp}$... internal clock output) (2/2)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SIp setup time (to $\overline{SCKp}$↑) Note 1	t_{SIK1}	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	177			ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	479			ns
SIp hold time (from $\overline{SCKp}$↑) Note 1	t_{KSI1}	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19			ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	19			ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 1	t_{KSO1}	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			195	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ			483	ns
SIp setup time (to $\overline{SCKp}$↓) Note 2	t_{SIK1}	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	44			ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	110			ns
SIp hold time (from $\overline{SCKp}$↓) Note 2	t_{KSI1}	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ	19			ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ	19			ns
Delay time from $\overline{SCKp}$↑ to SOp output Note 2	t_{KSO1}	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ			25	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V, C_b = 30 pF, R_b = 5.5 kΩ			25	ns

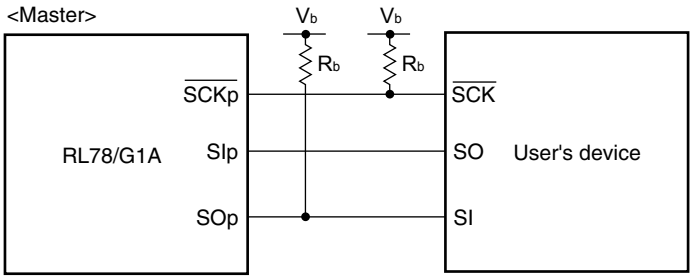
Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

(**Cautions** and **Remarks** are listed on the next page.)

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

CSI mode connection diagram (during communication at different potential)



Cautions 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and $\overline{SCKp}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

2. Use it with $EV_{DD0} \geq V_b$.

Remarks 1. R_b[Ω]:Communication line ($\overline{SCKp}$, SOp) pull-up resistance, C_b[F]: Communication line ($\overline{SCKp}$, SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00, 01, 10, 20), m: Unit number , n: Channel number (mn = 00, 01, 02, 10), g: PIM and POM number (g = 0, 1)

3. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.

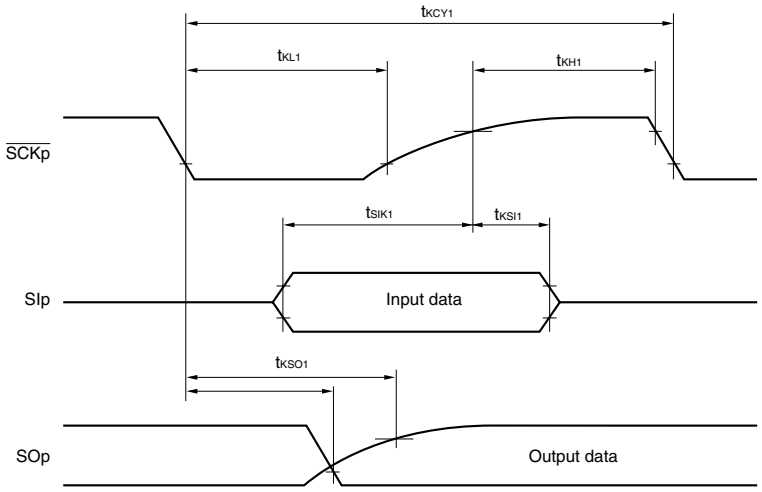
$2.7\ V \leq EV_{DD0} < 3.6\ V$, $2.3\ V \leq V_b \leq 2.7\ V$: $V_{IH} = 2.0\ V$, $V_{IL} = 0.5\ V$

$1.8\ V \leq EV_{DD0} < 3.3\ V$, $1.6\ V \leq V_b \leq 2.0\ V$: $V_{IH} = 1.5\ V$, $V_{IL} = 0.32\ V$

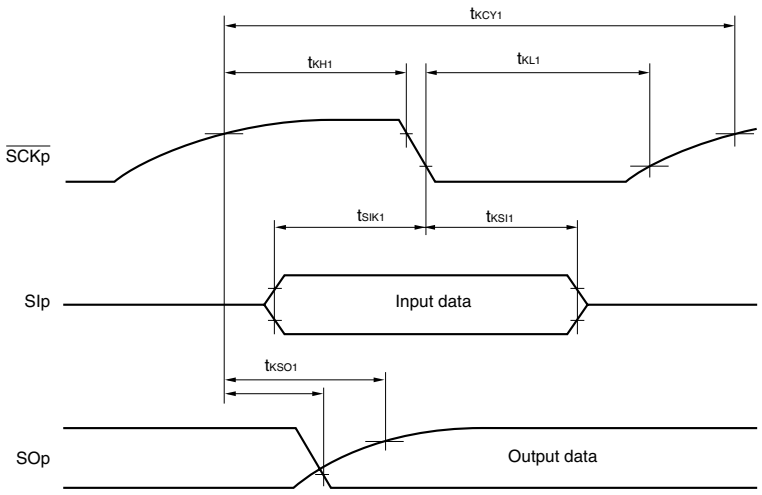
4. CSI01, CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin and $\overline{\text{SCKp}}$ pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01, 10, 20), m: Unit number, n: Channel number (m = 00, 01, 02, 10), g: PIM and POM number (g = 0, 1)

2. CSI01, CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(9) Communication at different potential (2.5 V) (CSI mode) (slave mode, $\overline{SCKp}$... external clock input)
(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
$\overline{SCKp}$ cycle time Note 1	t_{KCY2}	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V	24 MHz < f_{MCK}	20/f_{MCK}			ns
			20 MHz < f_{MCK} ≤ 24 MHz	16/f_{MCK}			ns
			16 MHz < f_{MCK} ≤ 20 MHz	14/f_{MCK}			ns
			8 MHz < f_{MCK} ≤ 16 MHz	12/f_{MCK}			ns
			4 MHz < f_{MCK} ≤ 8 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 4 MHz	6/f_{MCK}			ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2	24 MHz < f_{MCK}	48/f_{MCK}			ns
			20 MHz < f_{MCK} ≤ 24 MHz	36/f_{MCK}			ns
			16 MHz < f_{MCK} ≤ 20 MHz	32/f_{MCK}			ns
			8 MHz < f_{MCK} ≤ 16 MHz	26/f_{MCK}			ns
			4 MHz < f_{MCK} ≤ 8 MHz	16/f_{MCK}			ns
			f_{MCK} ≤ 4 MHz	10/f_{MCK}			ns
$\overline{SCKp}$ high-/low-level width	t_{KH2}, t_{KL2}	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V		t_{KCY2}/2 – 18			ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2		t_{KCY2}/2 – 50			ns
SIp setup time (to $\overline{SCKp}$↑) Note 3	t_{SIK2}	2.7 V ≤ EV_{DD0} ≤ 3.6 V		60			ns
		1.8 V ≤ EV_{DD0} < 3.3 V		97			ns
SIp hold time (from $\overline{SCKp}$↑) Note 4	t_{KSI2}			1/f_{MCK} + 31			ns
Delay time from $\overline{SCKp}$↓ to SOp output Note 5	t_{KSO2}	2.7 V ≤ EV_{DD0} < 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 30 pF, R_b = 2.7 kΩ				2/f_{MCK} + 214	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 2, C_b = 30 pF, R_b = 5.5 kΩ				2/f_{MCK} + 573	ns

Notes 1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps

2. Use it with EV_{DD0} ≥ V_b.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

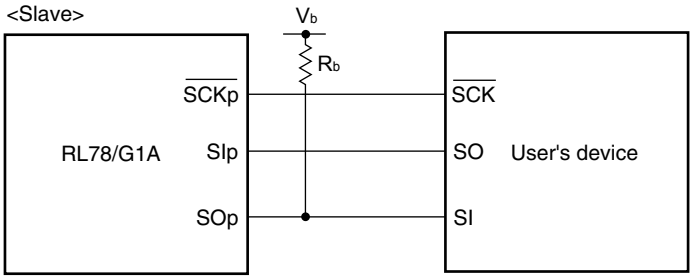
4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from $\overline{SCKp}$↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

5. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from $\overline{SCKp}$↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

(**Caution** and **Remarks** are listed on the next page.)

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

CSI mode connection diagram (during communication at different potential)



Caution Select the TTL input buffer for the SIp pin and $\overline{\text{SCKp}}$ pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. R_b[Ω]:Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

2. p: CSI number (p = 00, 01, 10, 20), m: Unit number (m = 0, 1), n: Channel number (n = 00, 01, 02, 10), g: PIM and POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00, 01, 02, 10))

4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.

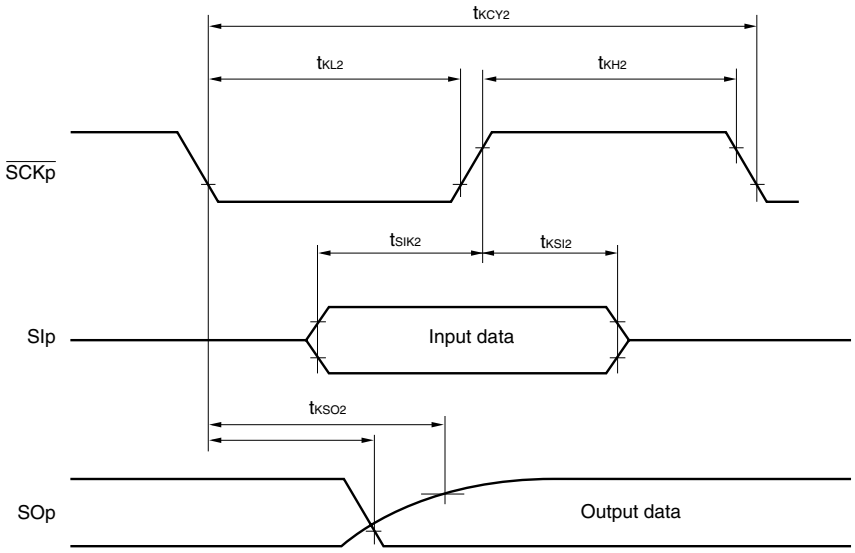
$2.7\ V \le EV_{DD0} < 3.6\ V$, $2.3\ V \le V_b \le 2.7\ V$: $V_{IH} = 2.0\ V$, $V_{IL} = 0.5\ V$

$1.8\ V \le EV_{DD0} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$: $V_{IH} = 1.5\ V$, $V_{IL} = 0.32\ V$

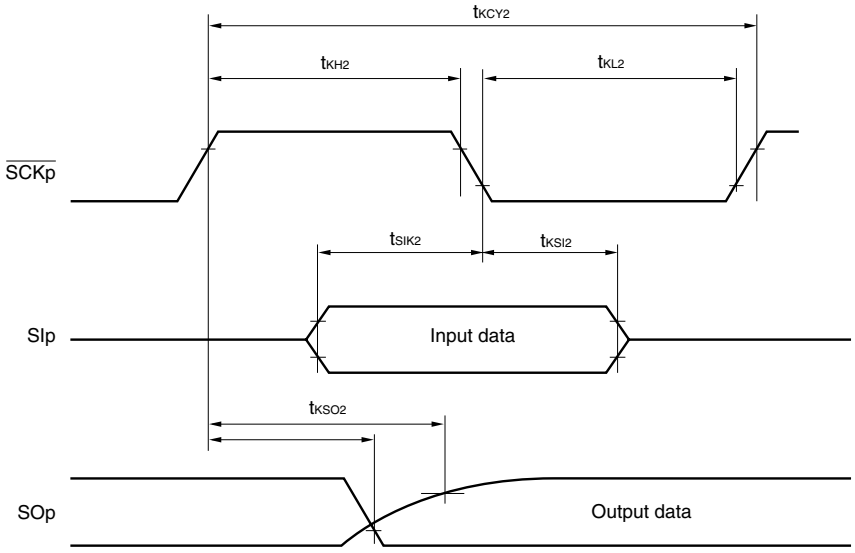
5. CSI01, CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Caution Select the TTL input buffer for the SIp pin and $\overline{\text{SCKp}}$ pin and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. p: CSI number (p = 00, 01, 10, 20), m: Unit number, n: Channel number (mn = 00, 01, 02, 10), g: PIM and POM number (g = 0, 1)

2. CSI01, CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(10) Communication at different potential (2.5 V) (simplified I^2C mode) (1/2)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ		1000	kHz
		2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ		400	kHz
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 1, C_b = 100 pF, R_b = 5.5 kΩ		300	kHz
Hold time when SCLr = “L”	t_{LOW}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	475		ns
		2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1150		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 1, C_b = 100 pF, R_b = 5.5 kΩ	1550		ns
Hold time when SCLr = “H”	t_{HIGH}	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	200		ns
		2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	600		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 1, C_b = 100 pF, R_b = 5.5 kΩ	610		ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(10) Communication at different potential (2.5 V) (simplified I^2C mode) (2/2)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 135 Note 2		ns
		2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	$1/f_{MCK}$ + 190 Note 2		ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Notes 1, C_b = 100 pF, R_b = 5.5 kΩ	$1/f_{MCK}$ + 190 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	ns
		2.7 V ≤ EV_{DD0} ≤ 3.6 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	355	ns
		1.8 V ≤ EV_{DD0} < 3.3 V, 1.6 V ≤ V_b ≤ 2.0 V Note 1, C_b = 100 pF, R_b = 5.5 kΩ	0	405	ns

Notes 1. Use it with $EV_{DD0} \geq V_b$.

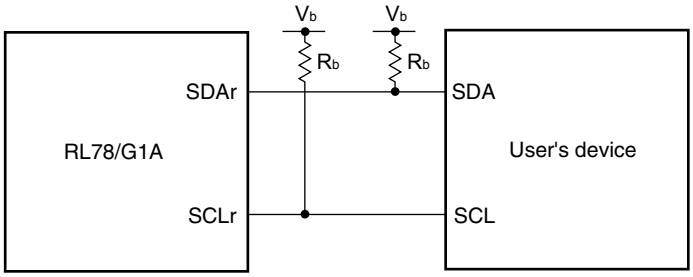
2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg).

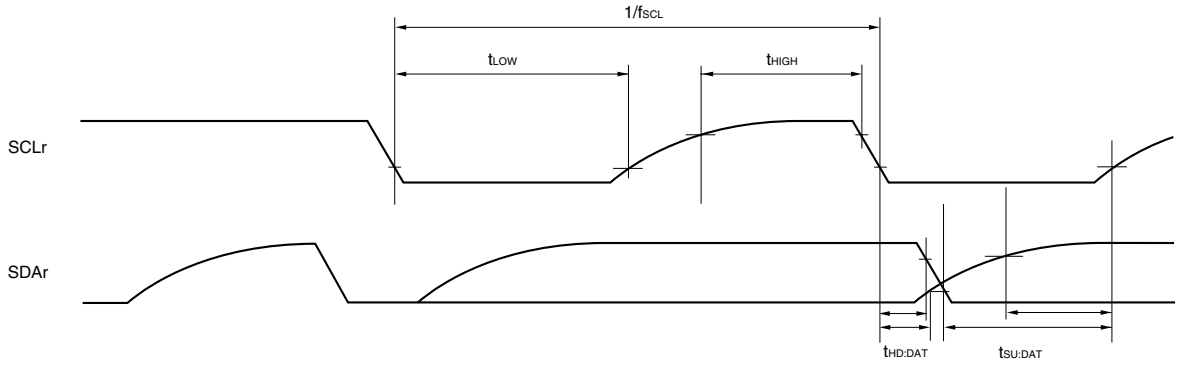
(**Remarks** is listed on the next page.)

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. R_b[Ω]:Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

2. r: IIC number (r = 00, 01, 10, 20), g: PIM, POM number (g = 0, 1)

3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10)

4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in simplified I²C mode mode.

$2.7\ V \le EV_{DD0} < 3.6\ V$, $2.3\ V \le V_b \le 2.7\ V$: $V_{IH} = 2.0\ V$, $V_{IL} = 0.5\ V$

$1.8\ V \le EV_{DD0} < 3.3\ V$, $1.6\ V \le V_b \le 2.0\ V$: $V_{IH} = 1.5\ V$, $V_{IL} = 0.32\ V$

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

2.5.2 Serial interface IICA

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

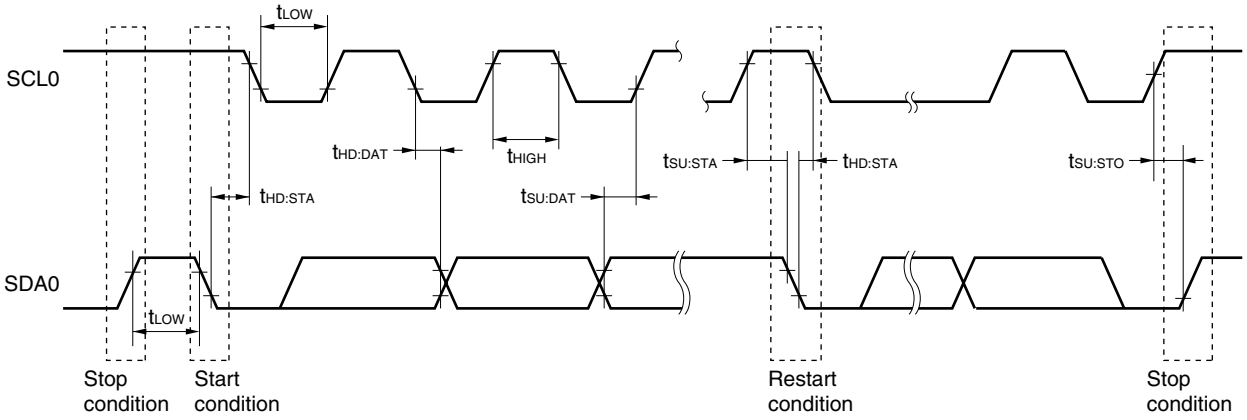
Parameter	Symbol	Conditions		Standard Mode		Fast Mode		Fast Mode Plus		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: f_{CLK} ≥ 10 MHz	2.7 V ≤ EV_{DD0} ≤ 3.6 V					0	1000	kHz
		Fast mode: f_{CLK} ≥ 3.5 MHz	1.8 V ≤ EV_{DD0} ≤ 3.6 V			0	400			kHz
		Normal mode: f_{CLK} ≥ 1 MHz	1.6 V ≤ EV_{DD0} ≤ 3.6 V	0	100					kHz
Setup time of restart condition	$t_{SU:STA}$			4.7		0.6		0.26		μs
Hold time[Note 1]	$t_{HD:STA}$			4.0		0.6		0.26		μs
Hold time when SCLA0 = "L"	t_{LOW}			4.7		1.3		0.5		μs
Hold time when SCLA0 = "H"	t_{HIGH}			4.0		0.6		0.26		μs
Data setup time (reception)	$t_{SU:DAT}$			250		100		50		ns
Data hold time (transmission)[Note 2]	$t_{HD:DAT}$			0	3.45	0	0.9	0		μs
Setup time of stop condition	$t_{SU:STO}$			4.0		0.6		0.26		μs
Bus-free time	t_{BUF}			4.7		1.3		0.5		μs

Notes 1. The first clock pulse is generated after this period when the start/restart condition is detected.
2. The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the $\overline{ACK}$ (acknowledge) timing.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ
Fast mode: C_b = 320 pF, R_b = 1.1 kΩ
Fast mode plus: C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

2.5.3 On-chip debug (UART)

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate			115.2 k		1 M	bps

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

(1) When $AV_{REF(+)}$ = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), $AV_{REF(-)}$ = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin : ANI0 to ANI12 (supply ANI pin to AV_{DD})

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 3.6 V, 1.6 V ≤ AV_{DD} ≤ 3.6 V, V_{SS} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{DD} ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV_{DD} ≤ 3.6 V	8		10 Note 1	
			1.6 V ≤ AV_{DD} ≤ 3.6 V	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±6.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±3.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±1.75	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V	3.375			μs
		ADTYP = 0, 10-bit resolution Note 1	1.8 V ≤ V_{DD} ≤ 3.6 V	6.75			
		ADTYP = 0, 8-bit resolution Note 2	1.6 V ≤ V_{DD} ≤ 3.6 V	13.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V	2.5625			
			1.8 V ≤ V_{DD} ≤ 3.6 V	5.125			
			1.6 V ≤ V_{DD} ≤ 3.6 V	10.25			
Zero-scale error Notes 3, 4	EZS	12-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			±4.0	%FSR
		10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			±2.5	
		8-bit resolution	1.6 V ≤ V_{DD} ≤ 3.6 V			±1.25	
Full-scale error Notes 3, 4	EFS	12-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			±4.0	%FSR
		10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			±2.5	
		8-bit resolution	1.6 V ≤ V_{DD} ≤ 3.6 V			±1.25	
Integral linearity error Note 3	ILE	12-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	LSB
		10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	
		8-bit resolution	1.6 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	
Differential linearity error Note 3	DLE	12-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	LSB
		10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	
		8-bit resolution	1.6 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	
Reference voltage (+)	$AV_{REF(+)}$	= AV_{REFP}	2.4 V ≤ V_{DD} ≤ 3.6 V	2.4		AV_{DD}	V
			1.8 V ≤ V_{DD} ≤ 3.6 V	1.8		AV_{DD}	
			1.6 V ≤ V_{DD} ≤ 3.6 V	1.6		AV_{DD}	
Reference voltage (–)	$AV_{REF(-)}$	= AV_{REFM}		–0.5		0.3	V
Analog input voltage	V_{AIN}			0		AV_{REFP}	V
	V_{BGR}	2.4 V ≤ V_{DD} ≤ 3.6 V		1.38	1.45	1.5	V
Consumption current	I_{ADC}	AV_{DD} = 3.6 V			460	1090	μA
V_{REF} current	I_{AVREF}	AV_{REFP} = 3.6 V			14	25	μA

Notes 1. Cannot be used for lower 2 bit of ADCR register
2. Cannot be used for lower 4 bit of ADCR register
3. Excludes quantization error (±1/2 LSB).
4. This value is indicated as a ratio (%FSR) to the full-scale value.

Caution Always use AV_{DD} pin with the same potential as the V_{DD} pin.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(2) When $AV_{REF(+)}$ = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), $AV_{REF(-)}$ = AV_{SS} (ADREFM = 0), target ANI pin : ANI0 to ANI12 (supply ANI pin to AV_{DD})

(T_A = –40 to +85°C, 1.6 V ≤ V_{DD} ≤ 3.6 V, 1.6 V ≤ AV_{DD} ≤ 3.6 V, V_{SS} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES		2.4 V ≤ AV_{DD} ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV_{DD} ≤ 3.6 V	8		10 Note 1	
			1.6 V ≤ AV_{DD} ≤ 3.6 V	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±9.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
Conversion time	tCONV	ADTYP = 0, 12-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V	3.375			μs
		ADTYP = 0, 10-bit resolution Note 1	1.8 V ≤ V_{DD} ≤ 3.6 V	6.75			
		ADTYP = 0, 8-bit resolution Note 2	1.6 V ≤ V_{DD} ≤ 3.6 V	13.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V	2.5625			
			1.8 V ≤ V_{DD} ≤ 3.6 V	5.125			
			1.6 V ≤ V_{DD} ≤ 3.6 V	10.25			
Zero-scale error Notes 3, 4	EZS	12-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			±7.0	%FSR
		10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			±3.75	
		8-bit resolution	1.6 V ≤ V_{DD} ≤ 3.6 V			±2.0	
Full-scale error Notes 3, 4	EFS	12-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			±7.0	%FSR
		10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			±3.75	
		8-bit resolution	1.6 V ≤ V_{DD} ≤ 3.6 V			±2.0	
Integral linearity error Note 3	ILE	12-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	LSB
		10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	
		8-bit resolution	1.6 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	
Differential linearity error Note 3	DLE	12-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	LSB
		10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	
		8-bit resolution	1.6 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	
Reference voltage (+)	AV_{REFP}	= AV_{DD}		1.6		3.6	V
Reference voltage (–)	AV_{REFM}	= AV_{SS}		–0.5		0.3	V
Analog input voltage	VAIN			0		AV_{REFP}	V
	VBGR	2.4 V ≤ V_{DD} ≤ 3.6 V		1.38	1.45	1.5	V
Consumption current	IADC	AV_{DD} = 3.6 V			460	1090	μA
VREF current	IAVREF	AV_{REFP} = 3.6 V			14	25	μA

Notes 1. Cannot be used for lower 2 bit of ADCR register
2. Cannot be used for lower 4 bit of ADCR register
3. Excludes quantization error (±1/2 LSB).
4. This value is indicated as a ratio (%FSR) to the full-scale value.

Caution Always use AV_{DD} pin with the same potential as the V_{DD} pin.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(3) When $AV_{REF(+)}$ = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), $AV_{REF(-)}$ = AV_{REFM}/ANI1 (ADREFM = 1), target ANI pin : ANI16 to ANI30 (supply ANI pin to EV_{DD0})

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, 1.6 V ≤ AV_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (–) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{DD} ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV_{DD} ≤ 3.6 V	8		10 Note 1	
			1.6 V ≤ AV_{DD} ≤ 3.6 V	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±9.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±2.5	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V	4.125			μs
		ADTYP = 0, 10-bit resolution Note 1	1.8 V ≤ V_{DD} ≤ 3.6 V	9.5			
		ADTYP = 0, 8-bit resolution Note 2	1.6 V ≤ V_{DD} ≤ 3.6 V	57.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V	3.3125			
			1.8 V ≤ V_{DD} ≤ 3.6 V	7.875			
			1.6 V ≤ V_{DD} ≤ 3.6 V	54.25			
Zero-scale error Notes 3, 4	EZS	12-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			±7.0	%FSR
		10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			±3.75	
		8-bit resolution	1.6 V ≤ V_{DD} ≤ 3.6 V			±2.0	
Full-scale error Notes 3, 4	EFS	12-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			±7.0	%FSR
		10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			±3.75	
		8-bit resolution	1.6 V ≤ V_{DD} ≤ 3.6 V			±2.0	
Integral linearity error Note 3	ILE	12-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	LSB
		10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	
		8-bit resolution	1.6 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	
Differential linearity error Note 3	DLE	12-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	LSB
		10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	
		8-bit resolution	1.6 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	
Reference voltage (+)	$AV_{REF(+)}$	= AV_{REFP}	2.4 V ≤ V_{DD} ≤ 3.6 V	2.4		AV_{DD}	V
			1.8 V ≤ V_{DD} ≤ 3.6 V	1.8		AV_{DD}	
			1.6 V ≤ V_{DD} ≤ 3.6 V	1.6		AV_{DD}	
Reference voltage (–)	$AV_{REF(-)}$	= AV_{REFM}		–0.5		0.3	V
Analog input voltage	V_{AIN}			0		AV_{REFP}	V
	V_{BGR}	2.4 V ≤ V_{DD} ≤ 3.6 V		1.38	1.45	1.5	V
Consumption current	I_{ADC}	AV_{DD} = 3.6 V			400	950	μA
V_{REF} current	I_{AVREF}	AV_{REFP} = 3.6 V			14	25	μA

Notes 1. Cannot be used for lower 2 bit of ADCR register
2. Cannot be used for lower 4 bit of ADCR register
3. Excludes quantization error (±1/2 LSB).
4. This value is indicated as a ratio (%FSR) to the full-scale value.

Caution Always use AV_{DD} pin with the same potential as the V_{DD} pin.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(4) When $AV_{REF(+)}$ = AV_{DD} (ADREFP1 = 0, ADREFP0 = 0), $AV_{REF(-)}$ = AV_{SS} (ADREFM = 0), target ANI pin : ANI16 to ANI30 (supply ANI pin to EV_{DD0})

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD0} ≤ 3.6 V, 1.6 V ≤ AV_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V, AV_{SS} = 0 V, Reference voltage (+) = AV_{DD}, Reference voltage (–) = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		2.4 V ≤ AV_{DD} ≤ 3.6 V	8		12	bit
			1.8 V ≤ AV_{DD} ≤ 3.6 V	8		10 Note 1	
			1.6 V ≤ AV_{DD} ≤ 3.6 V	8 Note 2			
Overall error Note 3	AINL	12-bit resolution	2.4 V ≤ AV_{DD} ≤ 3.6 V			±14.0	LSB
		10-bit resolution	1.8 V ≤ AV_{DD} ≤ 3.6 V			±7.5	
		8-bit resolution	1.6 V ≤ AV_{DD} ≤ 3.6 V			±3.75	
Conversion time	t_{CONV}	ADTYP = 0, 12-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V	4.125			μs
		ADTYP = 0, 10-bit resolution Note 1	1.8 V ≤ V_{DD} ≤ 3.6 V	9.5			
		ADTYP = 0, 8-bit resolution Note 2	1.6 V ≤ V_{DD} ≤ 3.6 V	57.5			
		ADTYP = 1, 8-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V	3.3125			μs
			1.8 V ≤ V_{DD} ≤ 3.6 V	7.875			
			1.6 V ≤ V_{DD} ≤ 3.6 V	54.25			
Zero-scale error Notes 3, 4	EZS	12-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			±9.0	%FSR
		10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ V_{DD} ≤ 3.6 V			±2.5	
Full-scale error Notes 3, 4	EFS	12-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			±9.0	%FSR
		10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			±5.0	
		8-bit resolution	1.6 V ≤ V_{DD} ≤ 3.6 V			±2.5	
Integral linearity error Note 3	ILE	12-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	LSB
		10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	
		8-bit resolution	1.6 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	
Differential linearity error Note 3	DLE	12-bit resolution	2.4 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	LSB
		10-bit resolution	1.8 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	
		8-bit resolution	1.6 V ≤ V_{DD} ≤ 3.6 V			T.B.D.	
Reference voltage (+)	$AV_{REF(+)}$	= AV_{DD}		1.6		3.6	V
Reference voltage (–)	$AV_{REF(-)}$	= AV_{SS}		–0.5		0.3	V
Analog input voltage	V_{AIN}			0		AV_{REFP}	V
	V_{BGR}	2.4 V ≤ V_{DD} ≤ 3.6 V		1.38	1.45	1.5	V
Consumption current	I_{ADC}	AV_{DD} = 3.6 V			400	950	μA
V_{REF} current	I_{AVREF}	AV_{REFP} = 3.6 V			14	25	μA

Notes 1. Cannot be used for lower 2 bit of ADCR register
2. Cannot be used for lower 4 bit of ADCR register
3. Excludes quantization error (±1/2 LSB).
4. This value is indicated as a ratio (%FSR) to the full-scale value.

Caution Always use AV_{DD} pin with the same potential as the V_{DD} pin.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

(5) When $AV_{REF(+)}$ = Internal reference voltage (1.45 V) (ADREFP1 = 1, ADREFP0 = 0), $AV_{REF(-)}$ = AV_{SS} (ADREFM = 0), target ANI pin : ANI0 to ANI12, ANI16 to ANI30

(T_A = –40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, 1.6 V ≤ AV_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V, AV_{SS0} = 0 V, Reference voltage (+) = Internal reference voltage, Reference voltage (–) = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}		8			bit
Conversion time	t_{CONV}	8-bit resolution	16			μs
Zero-scale error[Notes 1, 2]	EZS	8-bit resolution			±2.5	%FSR
Integral linearity error[Note 1]	ILE	8-bit resolution			T.B.D.	LSB
Differential linearity error[Note 1]	DLE	8-bit resolution			T.B.D.	LSB
Reference voltage (+)	$AV_{REF(+)}$	= Internal reference voltage	1.38	1.45	1.5	V
Reference voltage (–)	$AV_{REF(-)}$	= AV_{SS}	–0.5		0.3	V
Analog input voltage	V_{AIN}		0		AV_{REFP}	V
	V_{BGR}		Conversion prohibit			V
Consumption current	I_{ADC}	AV_{DD} = 3.6 V		400	950	μA
V_{REF} current	I_{AVREF}			75		μA

Notes 1. Excludes quantization error (±1/2 LSB).
2. This value is indicated as a ratio (%FSR) to the full-scale value.

Caution Always use AV_{DD} pin with the same potential as the V_{DD} pin.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

2.6.2 Temperature sensor characteristics

(T_A = –40 to +85°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V_{TMPS25}	Setting ADS register = 80H, T_A = +25°C		1.05		V
Reference output voltage	V_{CONST}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F_{VTMPS}	Temperature sensor that depends on the temperature		–3.6		mV/C
Operation stabilization wait time	t_{AMP}				2	μs

2.6.3 POR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V_{POR}	Power supply rise time	1.48	1.51	1.54	V
	V_{PDR}	Power supply fall time	1.47	1.50	1.53	V
Minimum pulse width	T_{PW}		300			μs
Detection delay time					350	μs

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

2.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode

(T_A = –40 to +85°C, $V_{PDR} \leq EV_{DD0} \leq V_{DD} \leq 3.6$ V, $V_{SS} = EV_{SS0} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	Supply voltage level	V_{LVD2}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V_{LVD3}	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V_{LVD4}	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V_{LVD5}	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		V_{LVD6}	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		V_{LVD7}	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		V_{LVD8}	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		V_{LVD9}	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
		V_{LVD10}	Power supply rise time	1.94	1.98	2.02	V
			Power supply fall time	1.90	1.94	1.98	V
		V_{LVD11}	Power supply rise time	1.84	1.88	1.91	V
			Power supply fall time	1.80	1.84	1.87	V
		V_{LVD12}	Power supply rise time	1.74	1.77	1.81	V
			Power supply fall time	1.70	1.73	1.77	V
		V_{LVD13}	Power supply rise time	1.64	1.67	1.70	V
			Power supply fall time	1.60	1.63	1.66	V
Minimum pulse width		t_{LW}		300			μs
Detection delay time						300	μs

Remark $V_{LVD(n-1)} > V_{LVDn}$: n = 3 to 13

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

LVD Detection Voltage of Interrupt & Reset Mode

(T_A = –40 to +85°C, $V_{PDR} \leq EV_{DD0} \leq V_{DD} \leq 3.6$ V, $V_{SS} = EV_{SS0} = 0$ V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Interrupt and reset mode	V_{LVD13}	V_{POC0}, V_{POC1}, V_{POC2} = 0, 0, 0, falling reset voltage: 1.6 V			1.60	1.63	1.66	V
	V_{LVD12}	LVIS0, LVIS1 = 1, 0 (+0.1 V)		Rising release reset voltage	1.74	1.77	1.81	V
				Falling interrupt voltage	1.70	1.73	1.77	V
	V_{LVD11}	LVIS0, LVIS1 = 0, 1 (+0.2 V)		Rising release reset voltage	1.84	1.88	1.91	V
				Falling interrupt voltage	1.80	1.84	1.87	V
	V_{LVD4}	LVIS0, LVIS1 = 0, 0 (+1.2 V)		Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVD11}	V_{POC0}, V_{POC1}, V_{POC2} = 0, 0, 1, falling reset voltage: 1.8 V			1.80	1.84	1.87	V
	V_{LVD10}	LVIS0, LVIS1 = 1, 0 (+0.1 V)		Rising release reset voltage	1.94	1.98	2.02	V
				Falling interrupt voltage	1.90	1.94	1.98	V
	V_{LVD9}	LVIS0, LVIS1 = 0, 1 (+0.2 V)		Rising release reset voltage	2.05	2.09	2.13	V
				Falling interrupt voltage	2.00	2.04	2.08	V
	V_{LVD2}	LVIS0, LVIS1 = 0, 0 (+1.2 V)		Rising release reset voltage	3.07	3.13	3.19	V
				Falling interrupt voltage	3.00	3.06	3.12	V
	V_{LVD8}	V_{POC0}, V_{POC1}, V_{POC2} = 0, 1, 0, falling reset voltage: 2.4 V			2.40	2.45	2.50	V
	V_{LVD7}	LVIS0, LVIS1 = 1, 0 (+0.1 V)		Rising release reset voltage	2.56	2.61	2.66	V
				Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVD6}	LVIS0, LVIS1 = 0, 1 (+0.2 V)		Rising release reset voltage	2.66	2.71	2.76	V
				Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVD5}	V_{POC0}, V_{POC1}, V_{POC2} = 0, 1, 1, falling reset voltage: 2.7 V			2.70	2.75	2.81	V
	V_{LVD4}	LVIS0, LVIS1 = 1, 0 (+0.1 V)		Rising release reset voltage	2.86	2.92	2.97	V
				Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVD3}	LVIS0, LVIS1 = 0, 1 (+0.2 V)		Rising release reset voltage	2.96	3.02	3.08	V
				Falling interrupt voltage	2.90	2.96	3.02	V

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

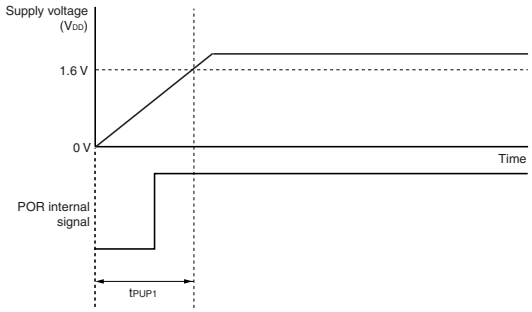
Supply Voltage Rise Time (T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum time to rise to 1.6 V (V_{DD} (MIN.))[Note] (V_{DD}: 0 V → 1.6 V)	t_{PUP1}	When $\overline{\text{RESET}}$ input is not used			3.2	ms

Note Make sure to raise the power supply in a shorter time than this.

Supply Voltage Rise Time Timing

- When RESET pin input is not used



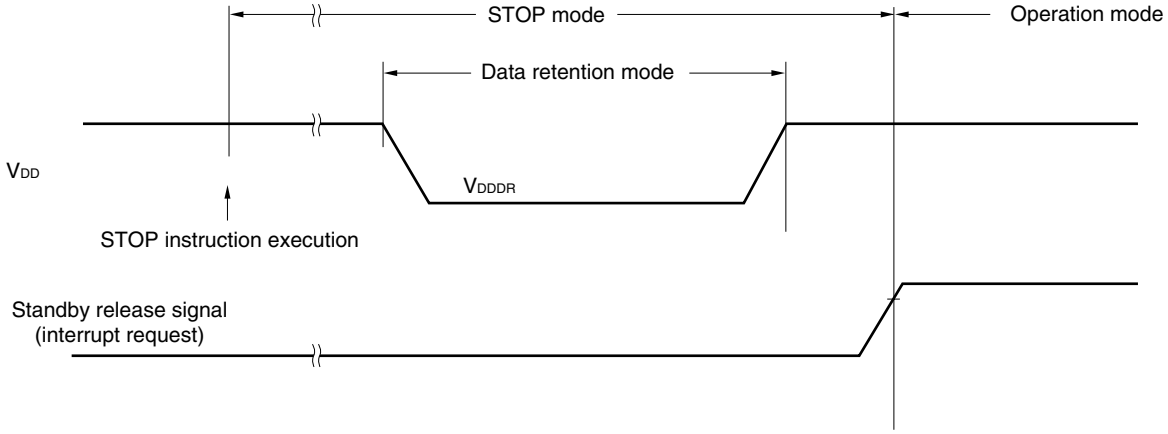
Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

2.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

(T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.47[Note]		3.6	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



2.8 Flash Memory Programming Characteristics

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	1.8 V ≤ V_{DD} ≤ 3.6 V		1		32	MHz
Number of code flash rewrites	C_{erwr}	1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.	Retained for 20 years (Self/serial programming)[Note]	1,000			Times
Number of data flash rewrites			Retained for 1 years (Self/serial programming)[Note]		1,000,000		
			Retained for 5 years (Self/serial programming)[Note]	100,000			

Note When using flash memory programmer and Renesas Electronics self programming library

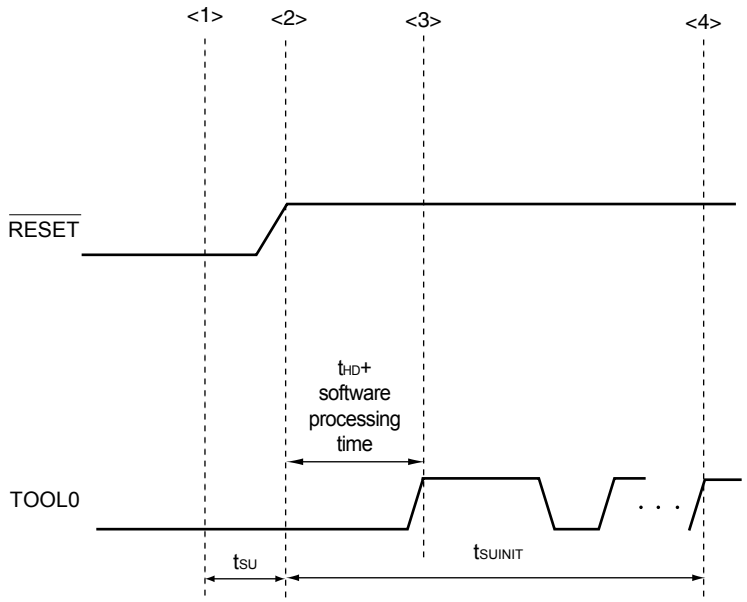
Remark When updating data multiple times, use the flash memory as one for updating data.

Caution The pins mounted depend on the product. Refer to 1.3.1 25-pin products to 1.3.4 64-pin products.

2.9 Timing Specs for Switching Modes

(T_A = –40 to +85°C, 1.8 V ≤ EV_{DD0} ≤ V_{DD} ≤ 3.6 V, V_{SS} = EV_{SS0} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when a pin reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the pin reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until a pin reset ends	t_{SU}	POR and LVD reset must end before the pin reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after a reset ends	t_{HD}	POR and LVD reset must end before the pin reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.
<2> The pins reset ends (POR and LVD reset must end before the pin reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

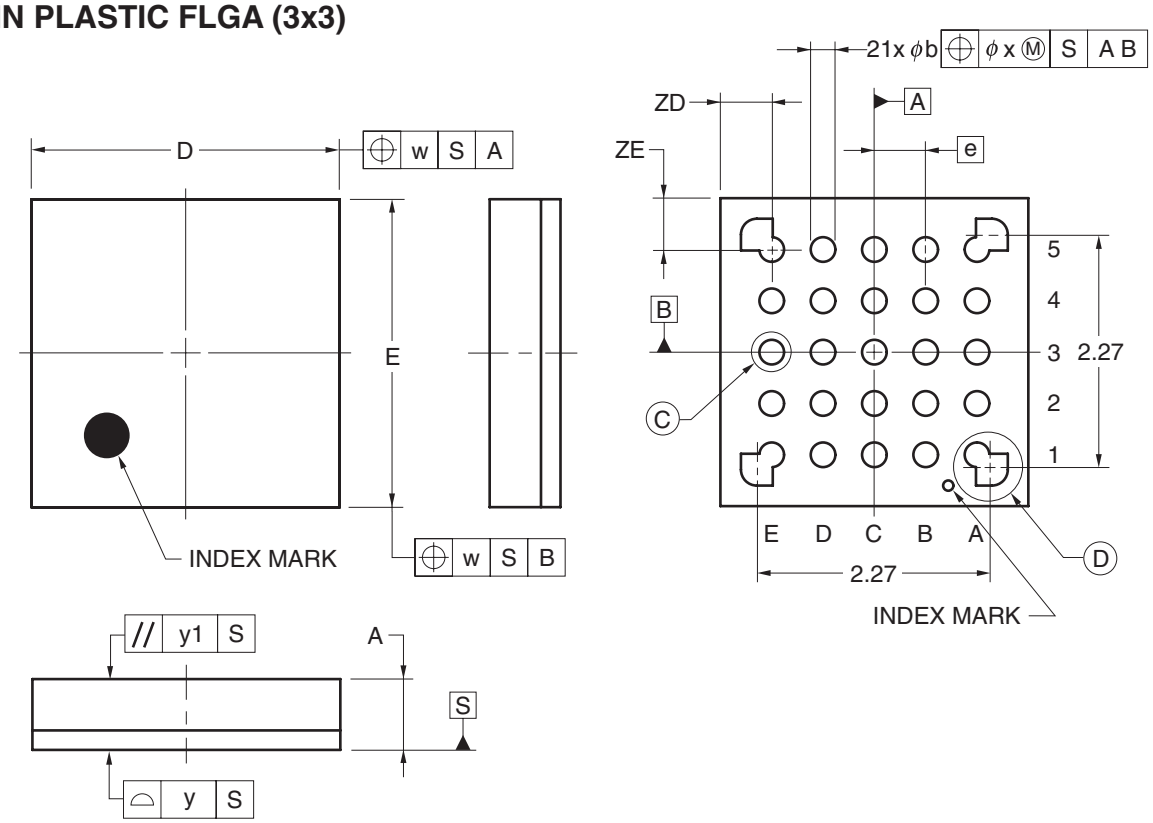
Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external and internal resets end.
t_{SU}: How long from when the TOOL0 pin is placed at the low level until a pin reset ends
t_{HD}: How long to keep the TOOL0 pin at the low level from when the external and internal resets end

3. PACKAGE DRAWINGS

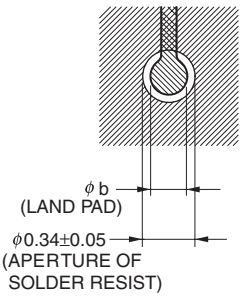
3.1 25-pin products

R5F10E8AALA, R5F10E8CALA, R5F10E8DALA, R5F10E8EALA

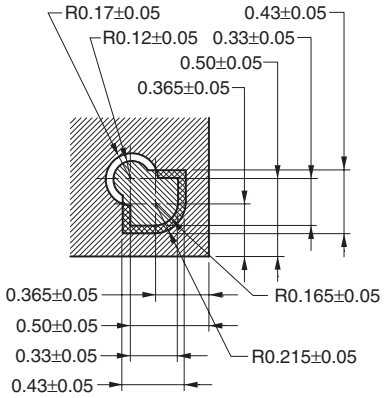
25-PIN PLASTIC FLGA (3x3)



DETAIL OF Ⓒ PART



DETAIL OF Ⓓ PART



(UNIT:mm)

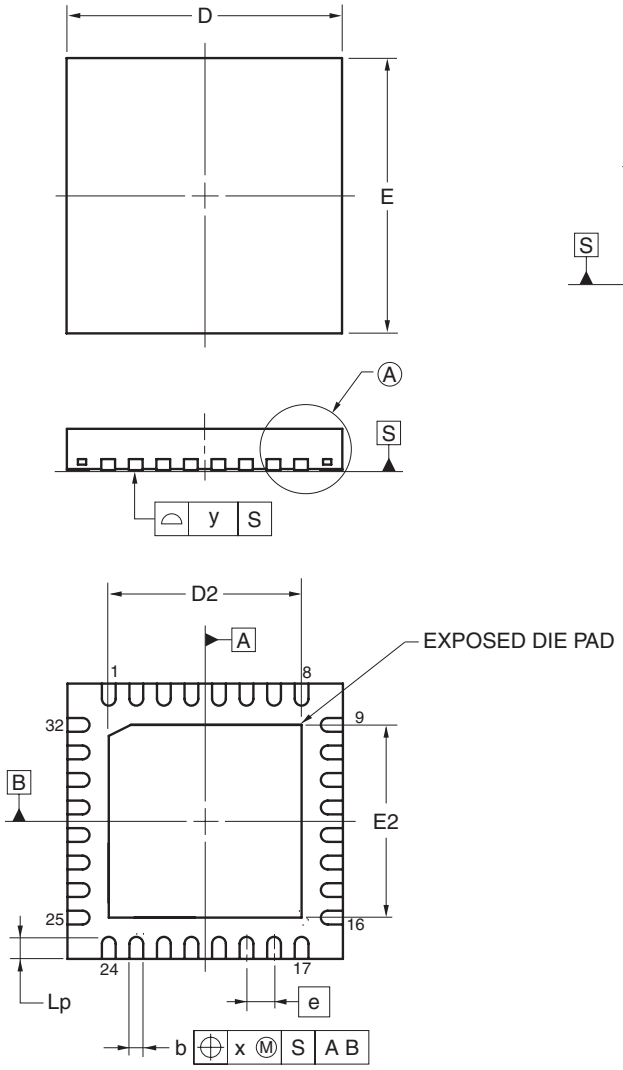
ITEM	DIMENSIONS
D	3.00±0.10
E	3.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.24±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.50
ZE	0.50

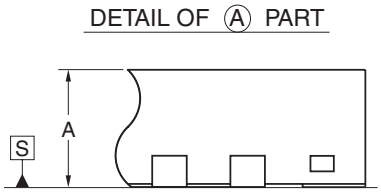
P25FC-50-2N2-1

3.2 32-pin products

R5F10EBAANA, R5F10EBCANA, R5F10EBDANA, R5F10EBEANA

32-PIN PLASTIC WQFN(5x5)





(UNIT:mm)

ITEM	DIMENSIONS
D	5.00±0.05
E	5.00±0.05
A	0.75±0.05
b	$0.25^{+0.05}_{-0.07}$
e	0.50
Lp	0.40±0.10
x	0.05
y	0.05

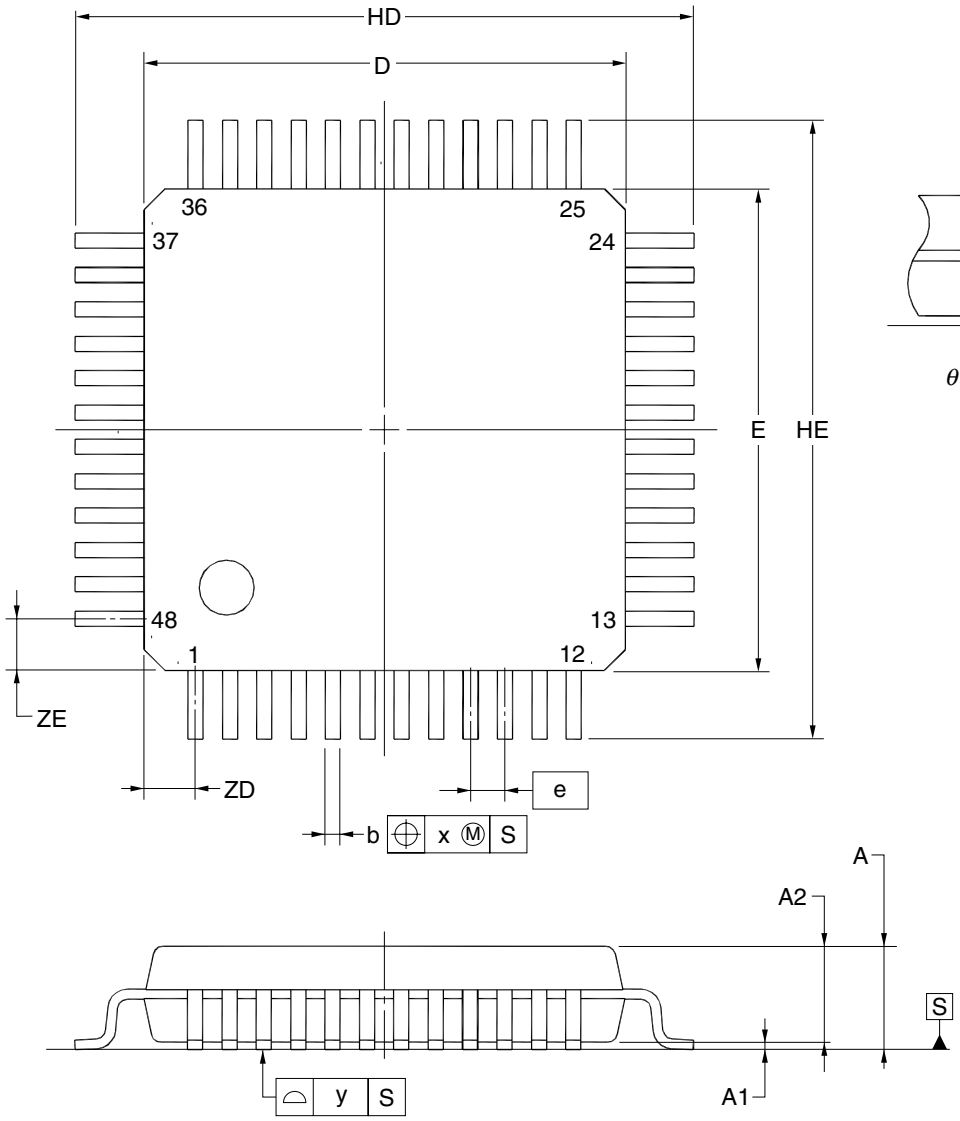
P32K8-50-3B4-2

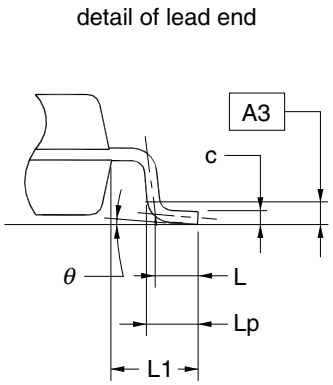
ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	3.45	3.50	3.55	3.45	3.50	3.55

3.3 48-pin products

R5F10EGAAFB, R5F10EGCAFB, R5F10EGDAFB, R5F10EGEAFB

48-PIN PLASTIC LQFP (FINE PITCH)(7x7)





(UNIT:mm)

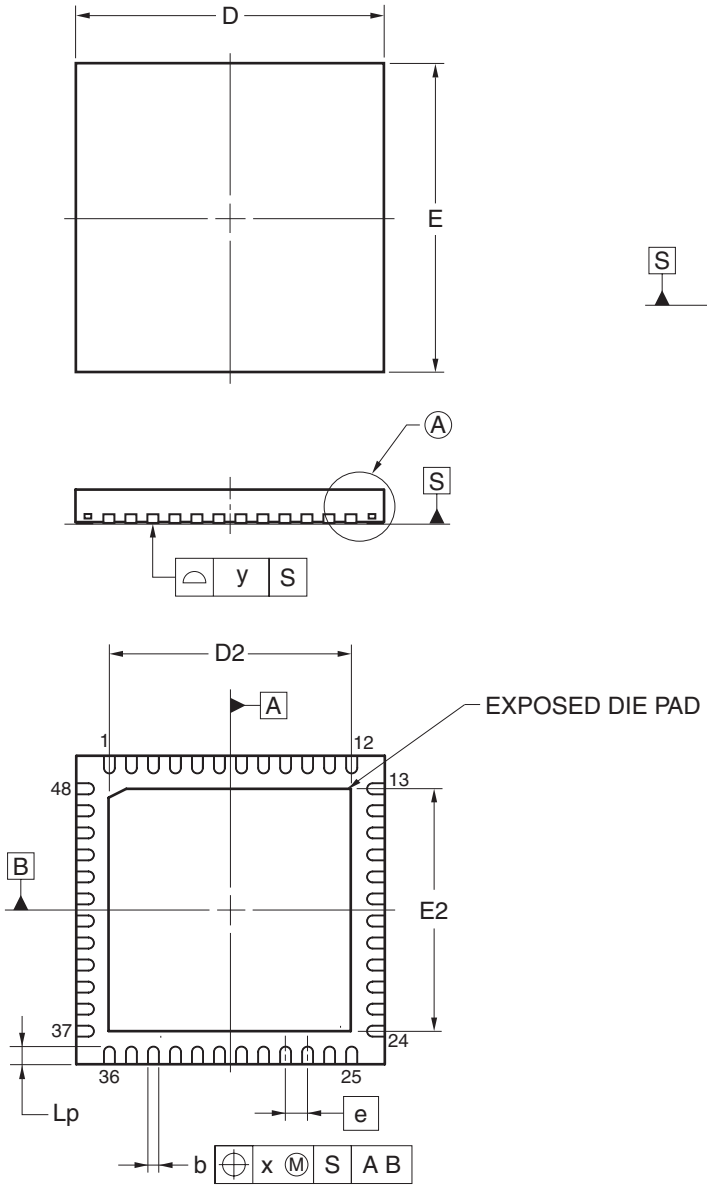
ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

P48GA-50-8EU

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

R5F10EGAANA, R5F10EGCANA, R5F10EGDANA, R5F10EGEANA

48-PIN PLASTIC WQFN(7x7)



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.05
E	7.00±0.05
A	0.75±0.05
b	$0.25^{+0.05}_{-0.07}$
e	0.50
Lp	0.40±0.10
x	0.05
y	0.05

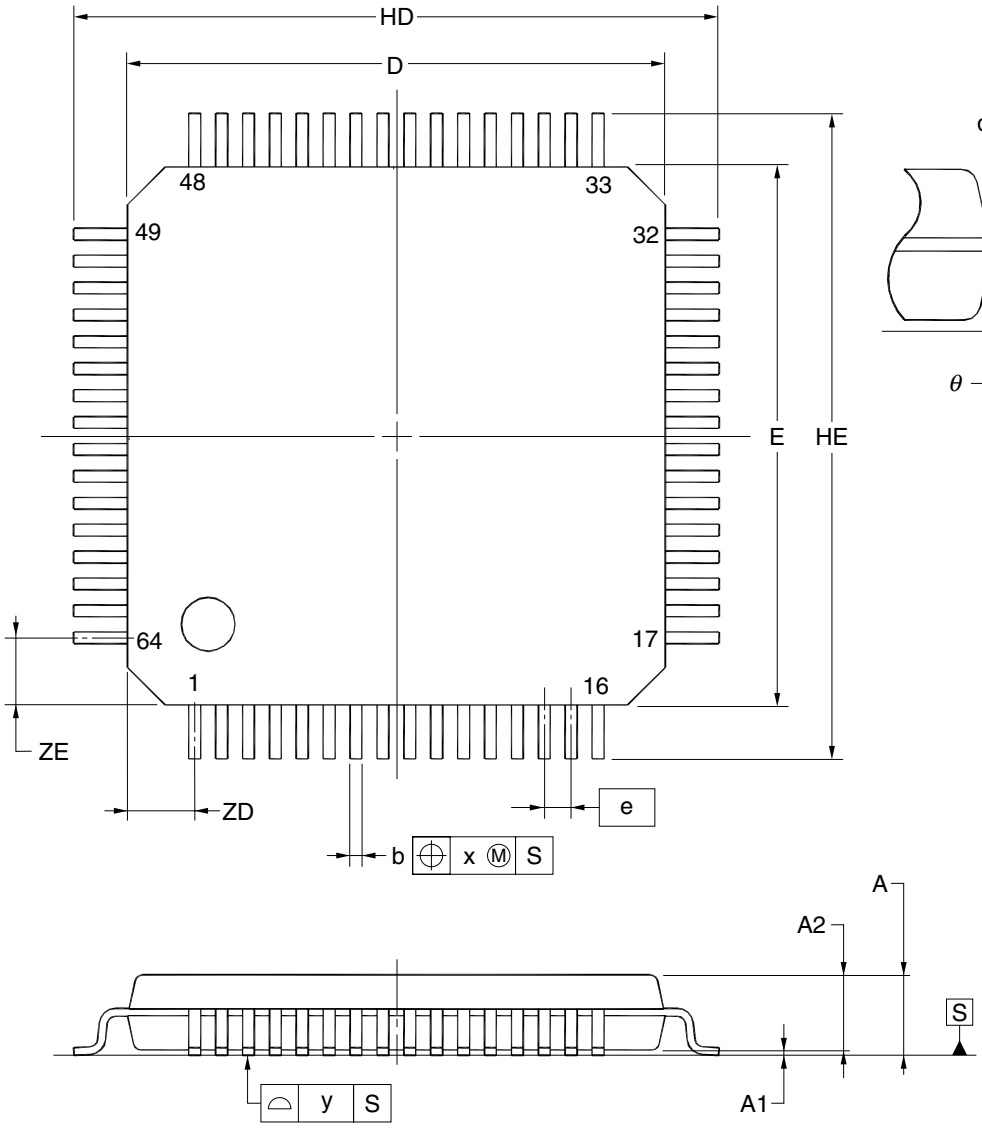
P48K8-50-5B4-3

ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	5.45	5.50	5.55	5.45	5.50	5.55

3.4 64-pin products

R5F10ELCAFB, R5F10ELDAFB, R5F10ELEAFB

64-PIN PLASTIC LQFP(FINE PITCH)(10x10)



(UNIT:mm)

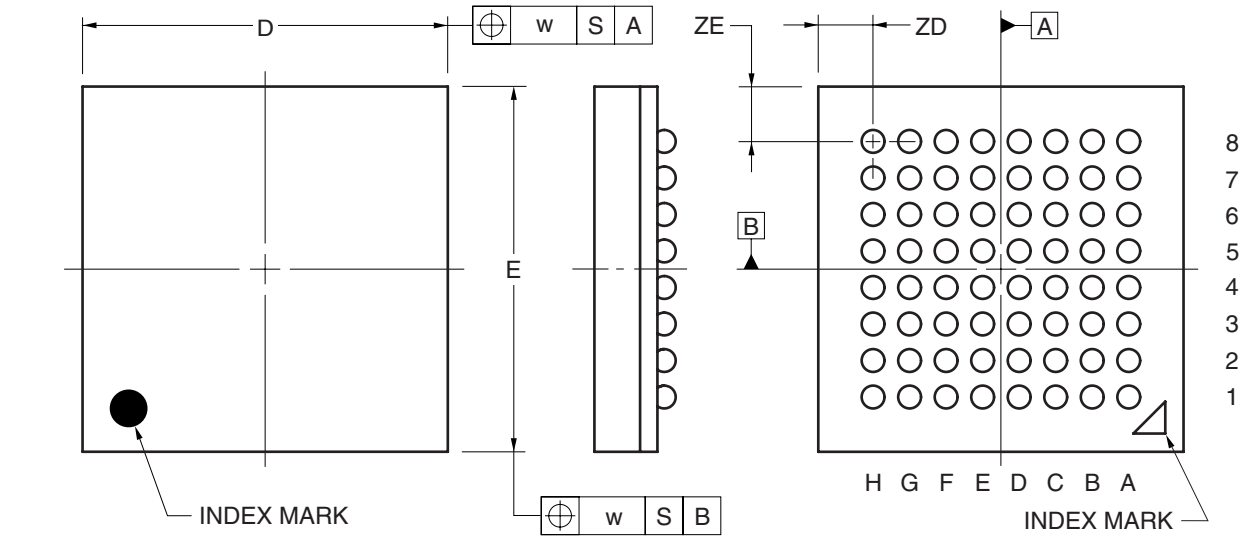
ITEM	DIMENSIONS
D	10.00±0.20
E	10.00±0.20
HD	12.00±0.20
HE	12.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	1.25
ZE	1.25

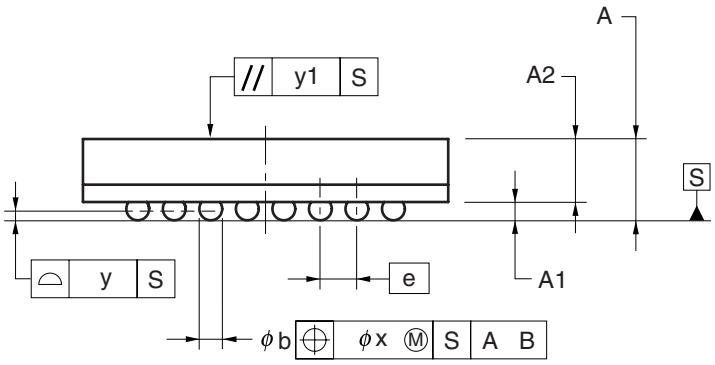
P64GB-50-UEU-1

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

R5F10ELCABG, R5F10ELDABG, R5F10ELEABG

64-PIN PLASTIC FBGA (4x4)





(UNIT:mm)

ITEM	DIMENSIONS
D	4.00±0.10
E	4.00±0.10
w	0.15
A	0.89±0.10
A1	0.20±0.05
A2	0.69
e	0.40
b	0.25±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.60
ZE	0.60

P64F1-40-AA2-1

Revision History	RL78/G1A Data Sheet

Rev.	Date	Description	
		Page	Summary
0.01	Dec 26, 2011	-	First Edition issued

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NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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