STEL-1176

Data Sheet

STEL-1176

80 MHz Decimal/BCD

0.1 Hz Resolution

CMOSNumerically

Controlled Oscillator

intel

FEATURES

- **HIGH CLOCK FREQUENCY**
  – 80 MHz MAXIMUM OVER COMMERCIAL OPERATING CONDITIONS
- **HIGH FREQUENCY RESOLUTION WITH DECIMAL FREQUENCY STEPS**
  – PRECISELY 0.1 Hz @ 80 MHz
- **VERY HIGH SPEED FREQUENCY HOPPING OR MODULATION**
  – MAX. UPDATE SPEED 250 NANOSECS.
- **PRECISION PHASE MODULATION**
  – 3 BITS FOR 8ARY PSK
- **HIGH RESOLUTION OUTPUT**
  – 12 BITS
- **HIGH SPECTRAL PURITY**
  – ALL SPURS < –72 dBc
- **PARALLEL OR BYTE-WIDE CONTROL INPUTS**
- **LOW POWER DISSIPATION**

APPLICATIONS

- **PRECISION SYNTHESIZERS**
- **INSTRUMENTATION**
- **CARRIER GENERATION**

FUNCTIONAL DESCRIPTION

The STEL-1176 Numerically Controlled Oscillator (NCO) uses digital techniques to provide a cost-effective solution for the generation of low noise, high resolution signals. The NCO devices combines low power 1.5µ CMOS technology with a unique architectural design resulting in a power efficient, high-speed sinusoidal waveform generator. This performance is enhanced by its rapid frequency switching capability and parallel control interface.

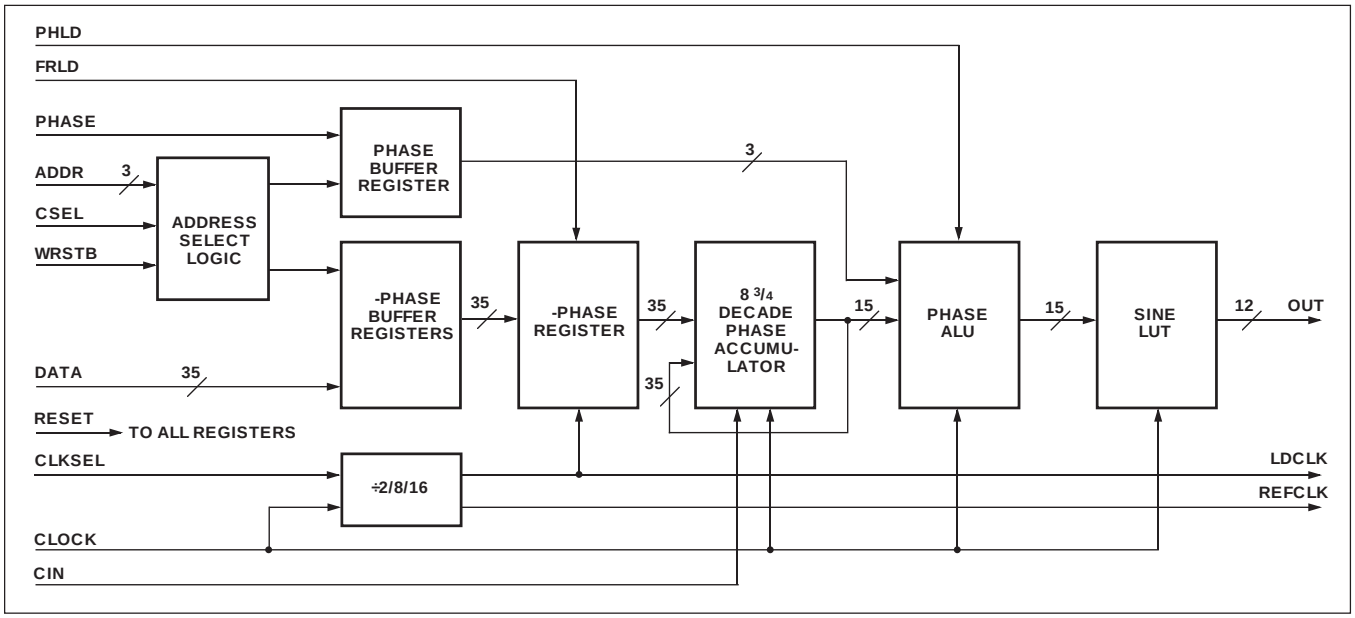
The STEL-1176 features high frequency resolution in a decimal format, with extremely low spurious signal levels and a high maximum operating frequency. The decimal frequency resolution allows frequencies to be generated in exact multiples of 0.1 Hz from a standard reference frequency, such as 10 MHz, and the divided clock output at 5 or 10 MHz is provided to facilitate this. The frequency control data format is 1-2-4-8 BCD, and the unique architecture allow the data to be loaded either as a 35-bit parallel word, for maximum speed, or as five bytes, for easy microprocessor interfacing. The STEL-1176 also features 3-bit phase modulation, allowing the output to be modulated with BPSK, QPSK or 8ary PSK data.

The output frequency can be calculated from the following equation:

$$f_o = \frac{f_c \times \Delta\text{-Phase}}{8 \times 10^8}$$

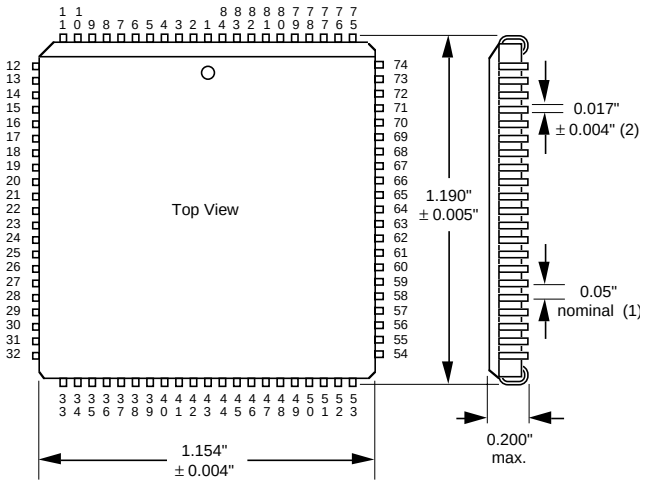
where: f_o is the frequency of the output signal
and: f_c is the clock frequency.

BLOCK DIAGRAM

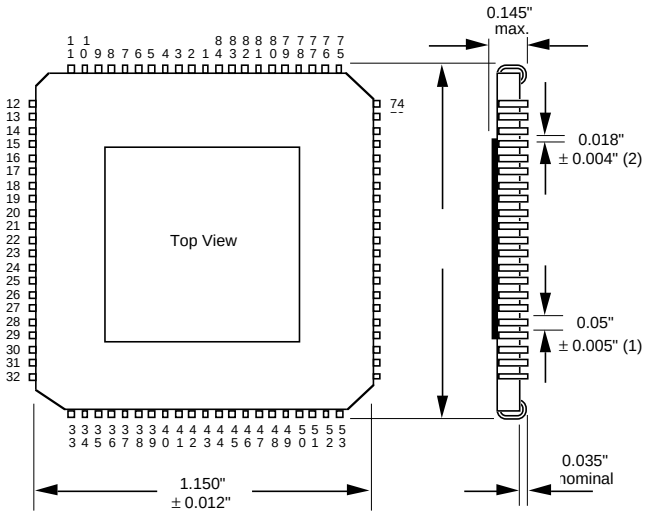


PIN CONFIGURATION

Package: 84 pin PLCC
Thermal coefficient, θ_{ja} = 30° / W



Package: 84 pin CLDCC
Thermal coefficient, θ_{ja} = 34° / W



Note: Tolerances on pin spacing are not cumulative.

PIN CONNECTIONS

1	V_{SS}	18	$DATA_6$	35	$DATA_{16}$	52	$DATA_{31}$	69	V_{SS}
2	RESET	19	V_{SS}	36	$DATA_{17}$	53	$DATA_{32}$	70	OUT_8
3	CIN	20	V_{DD}	37	$DATA_{18}$	54	V_{DD}	71	OUT_9
4	CLKSEL	21	V_{SS}	38	$DATA_{19}$	55	$DATA_{33}$	72	OUT_{10}
5	$ADDR_0$	22	V_{SS}	39	$DATA_{20}$	56	$DATA_{34}$	73	OUT_{11}
6	$ADDR_1$	23	CLOCK	40	$DATA_{21}$	57	I.C.	74	V_{DD}
7	$ADDR_2$	24	V_{SS}	41	$DATA_{22}$	58	V_{SS}	75	V_{DD}
8	WRSTB	25	$DATA_7$	42	$DATA_{23}$	59	OUT_0	76	LDCLK
9	CSEL	26	$DATA_8$	43	V_{SS}	60	OUT_1	77	V_{SS}
10	FRLD	27	$DATA_9$	44	V_{SS}	61	OUT_2	78	REFCLK
11	$DATA_0$	28	$DATA_{10}$	45	$DATA_{24}$	62	OUT_3	79	V_{SS}
12	V_{DD}	29	$DATA_{11}$	46	$DATA_{25}$	63	V_{SS}	80	PHLD
13	$DATA_1$	30	$DATA_{12}$	47	$DATA_{26}$	64	V_{SS}	81	$PHASE_0$
14	$DATA_2$	31	$DATA_{13}$	48	$DATA_{27}$	65	OUT_4	82	$PHASE_1$
15	$DATA_3$	32	$DATA_{14}$	49	$DATA_{28}$	66	OUT_5	83	$PHASE_2$
16	$DATA_4$	33	V_{DD}	50	$DATA_{29}$	67	OUT_6	84	V_{SS}
17	$DATA_5$	34	$DATA_{15}$	51	$DATA_{30}$	68	OUT_7		

Note: I.C. denotes Internal Connection. These pins must be left unconnected. Do not use for vias.

CIRCUIT DESCRIPTION

The STEL-1176 features a dual mode input port which can be set up to allow either byte-wide or parallel loading of the BCD frequency control data. The input is double buffered, and the new frequency data is loaded on the first or second rising edge of the **CLOCK** (whichever occurs while **LDCLK** is low) after the falling edge of the **FRLD** signal. A 3-bit phase modulator is also incorporated, and the phase modulation (PM) data is loaded separately on its own bus.

A BCD technique is used to create an NCO with a frequency resolution which has a decimal relationship to the clock frequency. This is achieved by providing nearly nine decades of accumulation with a range of 0 to 799,999,999. Any value within this range may be loaded into the Δ-Phase register as a frequency control word. Within this range a total of 80×10^7 values exist, so that when the NCO is operating at a clock frequency of 80 MHz, the output frequency resolution will be precisely 0.1 Hz. The 80 MHz clock is divided by eight or sixteen internally, and the divided clock is provided as an output at 10 MHz or 5 MHz. This output can be used to phase lock the 80 MHz clock generator to a reference standard.

The fifteen MSBs of the accumulator are used to address a unique lookup table. The lookup table generates a sinewave output with twelve bits of amplitude resolution. This results in a typical overall spurious performance of –72 dBc, or better.

The NCO generates a sampled sine wave where the sampling function is the clock. The practical upper limit of the NCO output frequency is about 40% of the clock frequency due to spurious components that are created by sampling. Those components are at frequencies greater than half the clock frequency, and become more difficult to remove by filtering.

The phase noise of the NCO output signal may be determined from the phase noise of the clock signal input and the ratio of the output frequency to the clock frequency. This ratio squared times the phase noise power of the clock specified in a given bandwidth is the phase noise power that may be expected in that same bandwidth relative to the output frequency.

The NCO achieves its high operating frequency by making extensive use of pipelining in its architecture. The pipeline delays within the NCO represent 37 clock cycles. The pipeline delay associated with the phase modulator is only 17 clock cycles, since the phase modulating function is at the output of the accumulator. The phase modulation may also be changed as rapidly as every clock cycle. Note that when a phase or frequency change occurs at the output the change is instantaneous, i.e., it occurs in one clock cycle, with complete phase coherence.

FUNCTION BLOCK DESCRIPTION

ADDRESS SELECT LOGIC BLOCK

This block controls the writing of data into the device via the $\mathbf{DATA_{34\text{-}0}}$ inputs and the $\mathbf{PHASE_{2\text{-}0}}$ inputs. The data is written into the device on the rising edge of the **WRSTB** input, and the mode (35-bit parallel or byte-wide) and register into which the data is written is selected by the $\mathbf{ADDR_{2\text{-}0}}$ inputs. The **CSEL** input can be used to selectively enable the writing of data from the bus.

Δ-PHASE BUFFER REGISTER BLOCK

The Δ-Phase Buffer Register Block is used to temporarily store the Δ-Phase data written into the device. This allows the data to be written asynchronously as a 35-bit word or as five bytes per 35-bit Δ-Phase word. The data is transferred from these registers into the Δ-Phase Register after a falling edge on the **FRLD** input.

PHASE BUFFER REGISTER BLOCK

The Phase Buffer Register Block is used to temporarily store the PM data written into the device. The data is transferred from this register into the Phase ALU after a falling edge on the **PHLD** input.

Δ-PHASE REGISTER BLOCK

This block controls the updating of the Δ-Phase data used in the Accumulator. The frequency data from the Δ-Phase Buffer Register Block is loaded into this block after a falling edge on the **FRLD** input.

PHASE ACCUMULATOR BLOCK

This block forms the core of the NCO function. It is a high-speed, pipelined, 35-bit parallel BCD accumulator, generating a new sum in every clock cycle. Unlike other NCOs, the arithmetic used in the STEL-1176 is BCD, making the resolution of the device decimal. The 35 bits make up $8^3/4$ decades, so that the full-scale count of the accumulator is 799,999,999. This makes the frequency resolution 1 part in 800,000,000, or 0.1 Hz in 80 MHz. A carry input (the **CIN** input) allows the resolution of the accumulator

to be expanded by means of an auxiliary NCO or phase accumulator. The overflow signal is discarded, since the required output is the modulo($8x10^8$) sum only. This represents the modulo(2π) phase angle.

PHASE ALU BLOCK
The Phase ALU performs the addition of the PM data to the Phase Accumulator output. The PM data word is 3 bits wide, and this is added to the 3 most significant bits from the Phase Accumulator to form the 15-bit modulated phase used to address the lookup table.

SINE LOOKUP TABLE BLOCK
This block is the sine memory. The 15 bits from the Phase Accumulator and ALU are used to address this memory to generate the 12-bit **OUT_{11-0}** outputs.

CLOCK DIVIDER BLOCK
The incoming system clock is divided by two and the half speed clock (**LDCLK**) is used in the Δ-Phase Register Block. The **LDCLK** is further divided by four or eight, depending on the state of the **CLKSEL** input, to provide the **REFCLK** output. This output may be used in a PLL circuit to lock the 80 MHz clock generator to a 10 MHz or 5 MHz reference standard.

INPUT SIGNALS

RESET
The **RESET** input is asynchronous and active low, and clears all the registers in the device. When **RESET** goes low, all registers are cleared within 13 nsecs, and normal operation will resume after this signal returns high. The data on the **OUT_{11-0}** bus will then be invalid for 10 clock cycles, and thereafter will remain at the value corresponding to zero phase (801H) until new frequency or phase data is loaded with the **FRLD** or **PHLD** inputs after the **RESET** returns high.

CLOCK
All synchronous functions performed within the NCO are referenced to the rising edge of the **CLOCK** input. The **CLOCK** signal should nominally be a square wave at a maximum frequency of 80 MHz. A non-repetitive **CLOCK** waveform is permissible as long as the minimum duration positive or negative pulse on the waveform is always greater than 5 nanoseconds.

CSEL
The **C**hip **Sel**ect input is used to control the writing of data into the chip. It is active low. When this input is high all data writing via the **$DATA_{7-0}$** bus is inhibited.

$DATA_{34}$ through $DATA_0$
The 35-bit **$DATA_{34-0}$** bus is used to program the 35-bit Δ-Phase Register. **$DATA_0$** is the least significant bit of the bus. The data programmed into the Δ-Phase register in this way determines the output frequency of the NCO. The data will be loaded as a parallel 35-bit word or as five bytes, depending on the state of the address bus, as shown in the address table. Each nibble (4 bits) of data starting at **$DATA_{3-0}$** represents one decade of frequency data in 1-2-4-8 BCD format. When the byte-wide mode is selected (addresses 000 to 100), the 35 data lines must be connected externally to form an 8-bit data bus as follows:

Connect **$DATA_{34-32}$** to **$DATA_{2-0}$**,
$DATA_{31-24}$ to **$DATA_{23-16}$** to **$DATA_{15-8}$** to **$DATA_{7-0}$**.

$PHASE_2$ through $PHASE_0$
The 3-bit **$PHASE_{2-0}$** bus is used to program the 3-bit Phase Register. **$PHASE_0$** is the least significant bit of the bus. **$PHASE_2$** corresponds to an incremental phase shift of 180°, **$PHASE_1$** corresponds to an incremental phase shift of 90°, and **$PHASE_0$** corresponds to an incremental phase shift of 45°.

$ADDR_2$ through $ADDR_0$
The three address lines **$ADDR_{2-0}$** control the use of the **$DATA_{34-0}$** bus for writing frequency data to the Δ-Phase Buffer Register and the **$PHASE_{2-0}$** bus for writing phase data to the Phase Buffer Register, as shown in the table:

$ADDR_2$	$ADDR_1$	$ADDR_0$	Register Field
0	0	0	Δ-Phase Bits 7-0 (LSB)[1]
0	0	1	Δ-Phase Bits 15-8[1]
0	1	0	Δ-Phase Bits 23-16[1]
0	1	1	Δ-Phase Bits 30-24[1]
1	0	0	Δ-Phase Bits 34-32[1]
1	0	1	Phase Bits 2-0
1	1	0	Δ-Phase Bits 34-0[2]
1	1	1	Δ-Phase + Phase Bits[3]

It is not necessary to reload unchanged bytes, and the byte loading sequence may be random.

Notes: 1. Byte-wide frequency loading mode.
2. Parallel frequency loading mode.
3. Loads the frequency data in the parallel mode and the phase data simultaneously.

WRSTB
The **Wr**ite **St**ro**b**e input is used to latch the data on the $\mathbf{DATA_{34-0}}$ and $\mathbf{PHASE_{2-0}}$ busses into the device. On the rising edge of the **WRSTB** input, the information on the busses is transferred to the buffer register selected by the $\mathbf{ADDR_{2-0}}$ bus.

FRLD
The **Fr**equency **L**oa**d** input is used to control the transfer of the data from the Δ-Phase Buffer Registers to the Δ-Phase Register. The data at the output of the Buffer Registers must be valid from the falling edge of **FRLD** until after the next rising edge of **LDCLK**. The data is then transferred during the subsequent cycle. The frequency of the NCO output will change 37 clock cycles after the **FRLD** command due to pipelining delays if **LDCLK** was low at the time; otherwise it will change 38 clock cycles later. The maximum frequency update rate of the device is once every 9 clock cycles.

PHLD
The **Ph**ase **L**oa**d** input is used to control the transfer of the data from the Phase Buffer Registers to the Phase ALU. The data at the output of the Buffer Register must be valid from the falling edge of **PHLD** until after the next rising edge of **LDCLK**. The data is then transferred during the subsequent cycle. The phase of the NCO output will change 17 clock cycles after the **PHLD** command due to pipelining delays if **LDCLK** was low at the time; otherwise it will change 18 clock cycles later.

CIN
The **C**arry **In**put is an arithmetic carry to the least significant bit of the Accumulator. Normal operation of the NCO requires that **CIN** be set at a logic 0. When **CIN** is set at a logic 1 the effective value of the Δ-Phase register is increased by one. This allows the resolution of the accumulator to be expanded for higher frequency resolution.

CLKSEL
The **Clo**c**k** **Sel**ect input selects the frequency of the **REFCLK** output. When **CLKSEL** is set low the frequency of **REFCLK** will be the **CLOCK** frequency divided by eight, and when it is set high the frequency will be the **CLOCK** frequency divided by sixteen.

OUTPUT SIGNALS

$\mathbf{OUT_{11-0}}$
The signal appearing on the $\mathbf{OUT_{11-0}}$ output bus is derived from the 15 most significant bits of the Phase Accumulator via the Phase ALU. The 12-bit sine function is presented in offset binary format. The value of the output for a given phase value follows the relationship when the phase modulation is zero:

$\mathbf{OUT_{11-0}}$=2047 x sin (360 x (phase+0.5)/8000)°+2048

The result is accurate to within 1 LSB. When the phase accumulator is zero, e.g., after a reset, the decimal value of the output is 2049 (801_H).

REFCLK
The **R**eference **Clo**c**k** output signal is the **CLOCK** input divided by either eight or sixteen, depending on the state of the **CLKSEL** input. When the input clock frequency is set to 80 MHz to obtain precise 0.1 Hz resolution, the frequency of the **REFCLK** signal will then be either 10 or 5 MHz. It can be used in conjunction with a phase locked loop (PLL) to lock the 80 MHz clock generator to a reference standard frequency at one of these two frequencies.

LDCLK
The **L**oad **Clo**c**k** output signal is the **CLOCK** input divided by two. This clock is used for loading the phase and frequency data from the buffer registers to the Phase ALU and Δ-Phase Register, respectively. This output can be used to determine the exact clock cycle during which these transfers will take place, as shown in the timing diagrams. The transfers will take place on the rising edge of the **CLK** following the falling edge of **FRLD** or **PHLD** when **LDCLK** is low. Since the propagation delay of this output from the rising edges of the **CLOCK** input is comparable to the clock period at 80 MHz, care should be taken when using this output to synchronize the phase and frequency changes. If this signal is not used, there is a 50% probability that the phase and frequency changes will occur one cycle of the **CLOCK** input later than specified.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

***Warning:** Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability. All voltages are referenced to V_{SS}.*

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	–40 to +125 –65 to +150	°C (Plastic package) °C (Ceramic package)
V_{DDmax}	Supply voltage on V_{DD}	–0.3 to + 7	volts
$V_{I(max)}$	Input voltage	–0.3 to V_{DD} + 0.3	volts
I_i	DC input current	± 10	mA

RECOMMENDED OPERATING CONDITIONS

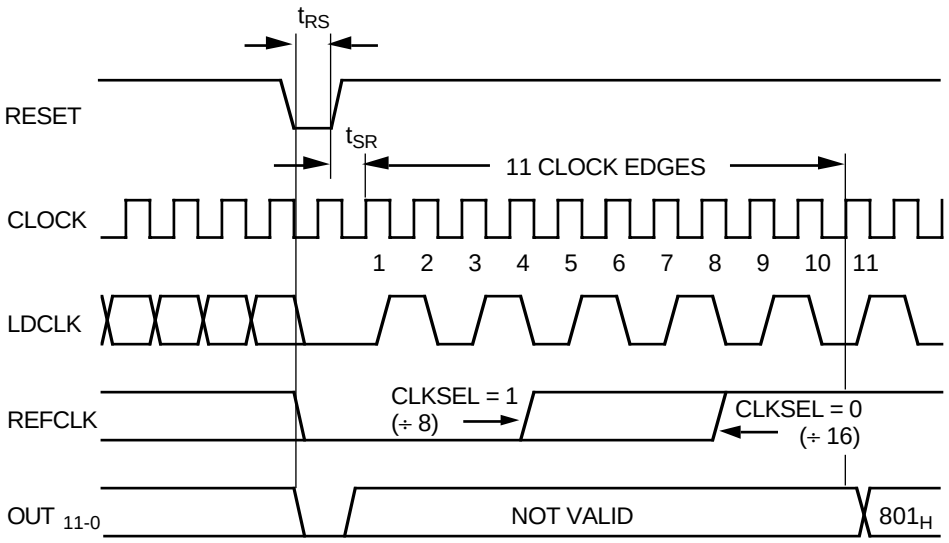
Symbol	Parameter	Range	Units	
V_{DD}	Supply Voltage	+5 ± 5% +5 ± 10%	Volts Volts	(Commercial) (Military)
T_a	Operating Temperature (Ambient)	0 to +50 –55 to +125	°C °C	(Commercial) (70° Case) (Military)

D.C. CHARACTERISTICS (Operating Conditions: V_{DD}= 5.0 V ±5%, VSS = 0 V, T_a= 0° to 50° C, Commercial

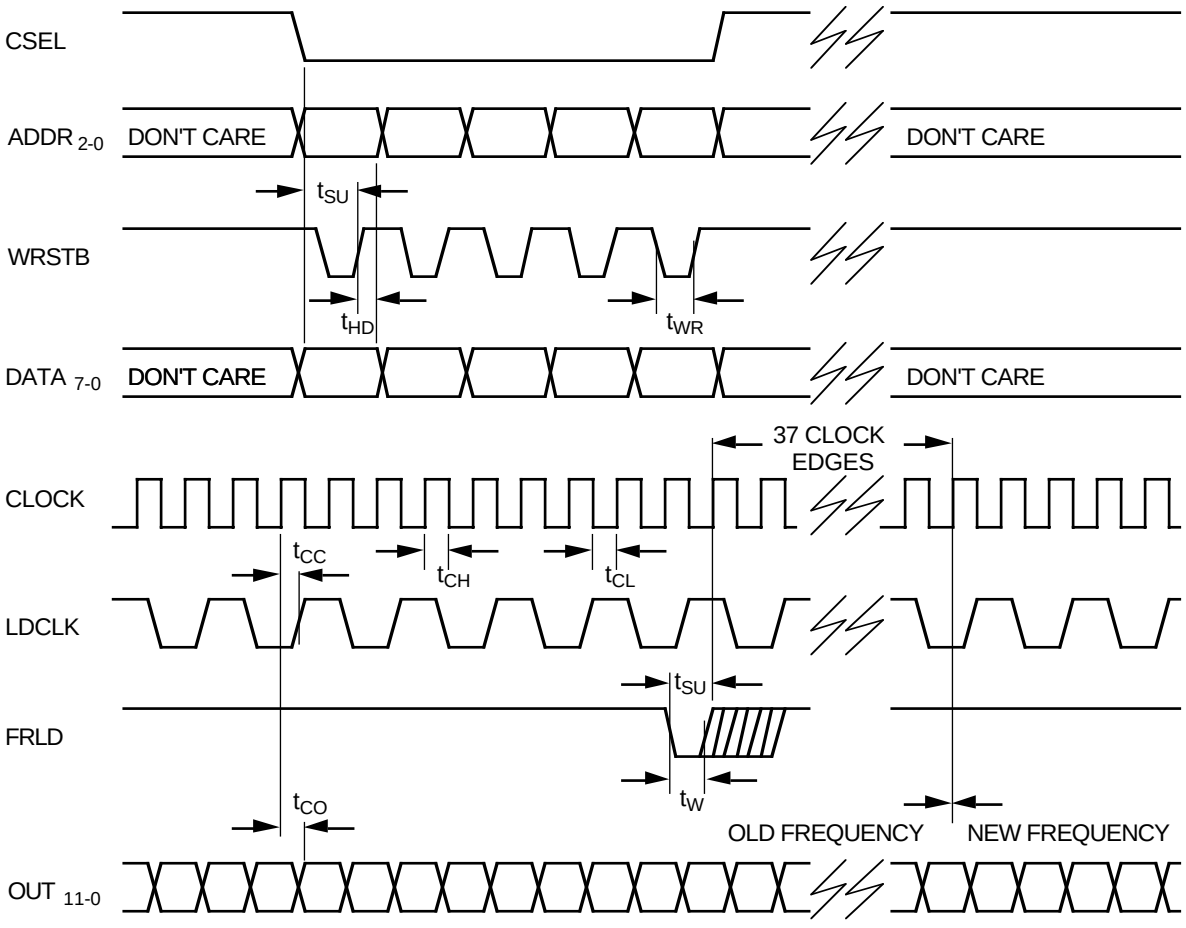
V_{DD}= 5.0 V ±10%, VSS = 0 V, Ta = –55° to 125° C, Military)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational			3.0	mA/MHz	
$V_{IH(min)}$	High Level Input Voltage					
	Standard Operating Conditions	2.0			volts	Logic '1'
	Extended Operating Conditions	2.25			volts	Logic '1'
$V_{IL(max)}$	Low Level Input Voltage			0.8	volts	Logic '0'
$I_{IH(min)}$	High Level Input Current	10	35	110	µA	**CIN** and **CSEL**, $V_{IN} = V_{DD}$
$I_{IH(min)}$	High Level Input Current			10	µA	All other inputs, $V_{IN} = V_{DD}$
$I_{IL(max)}$	Low Level Input Current			–10	µA	**CIN** and **CSEL**, $V_{IN} = V_{SS}$
$I_{IL(max)}$	Low Level Input Current	–15	–45	–130	µA	All other inputs, $V_{IN} = V_{SS}$
$V_{OH(min)}$	High Level Output Voltage	2.4	4.5		volts	I_O = –4.0 mA
$V_{OL(max)}$	Low Level Output Voltage		0.2	0.4	volts	I_O = +4.0 mA
I_{OS}	Output Short Circuit Current	20	65	130	mA	$V_{OUT} = V_{DD}$, V_{DD} = max
		–10	–45	–130	mA	$V_{OUT} = V_{SS}$, V_{DD} = max
C_{IN}	Input Capacitance		2		pF	All inputs
C_{OUT}	Output Capacitance		4		pF	All outputs

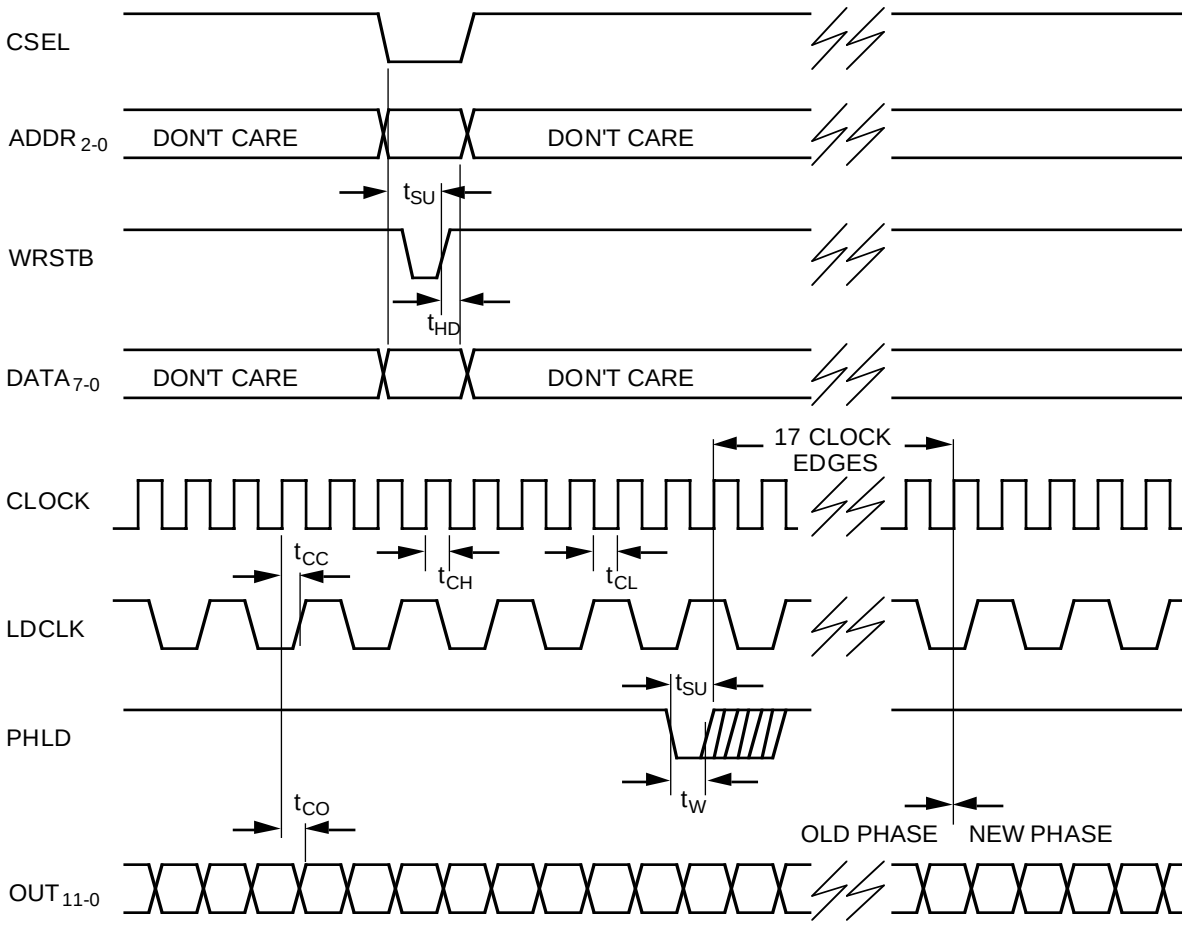
NCO RESET SEQUENCE



NCO FREQUENCY CHANGE SEQUENCE



NCO PHASE CHANGE SEQUENCE

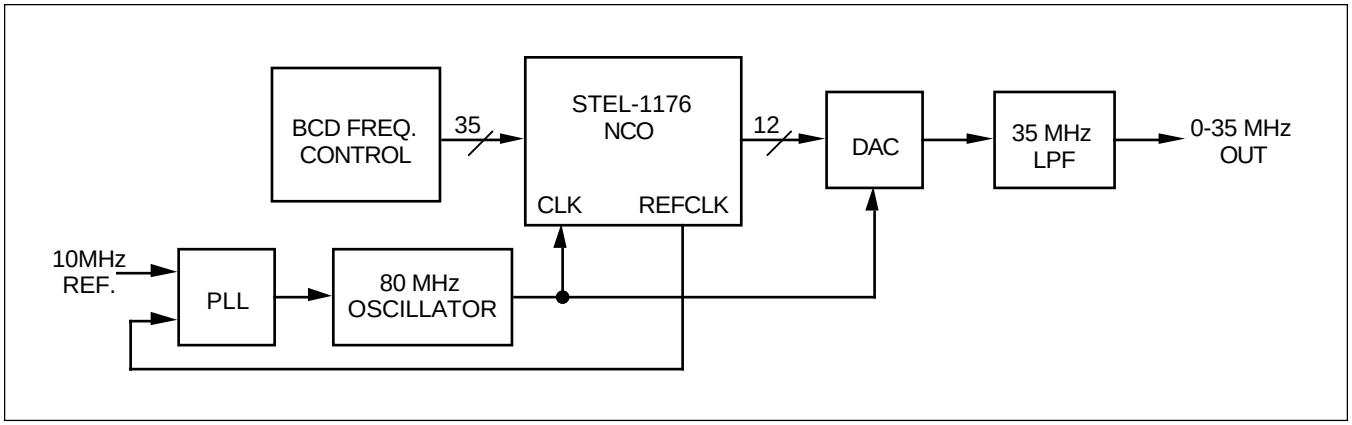


ELECTRICAL CHARACTERISTICS

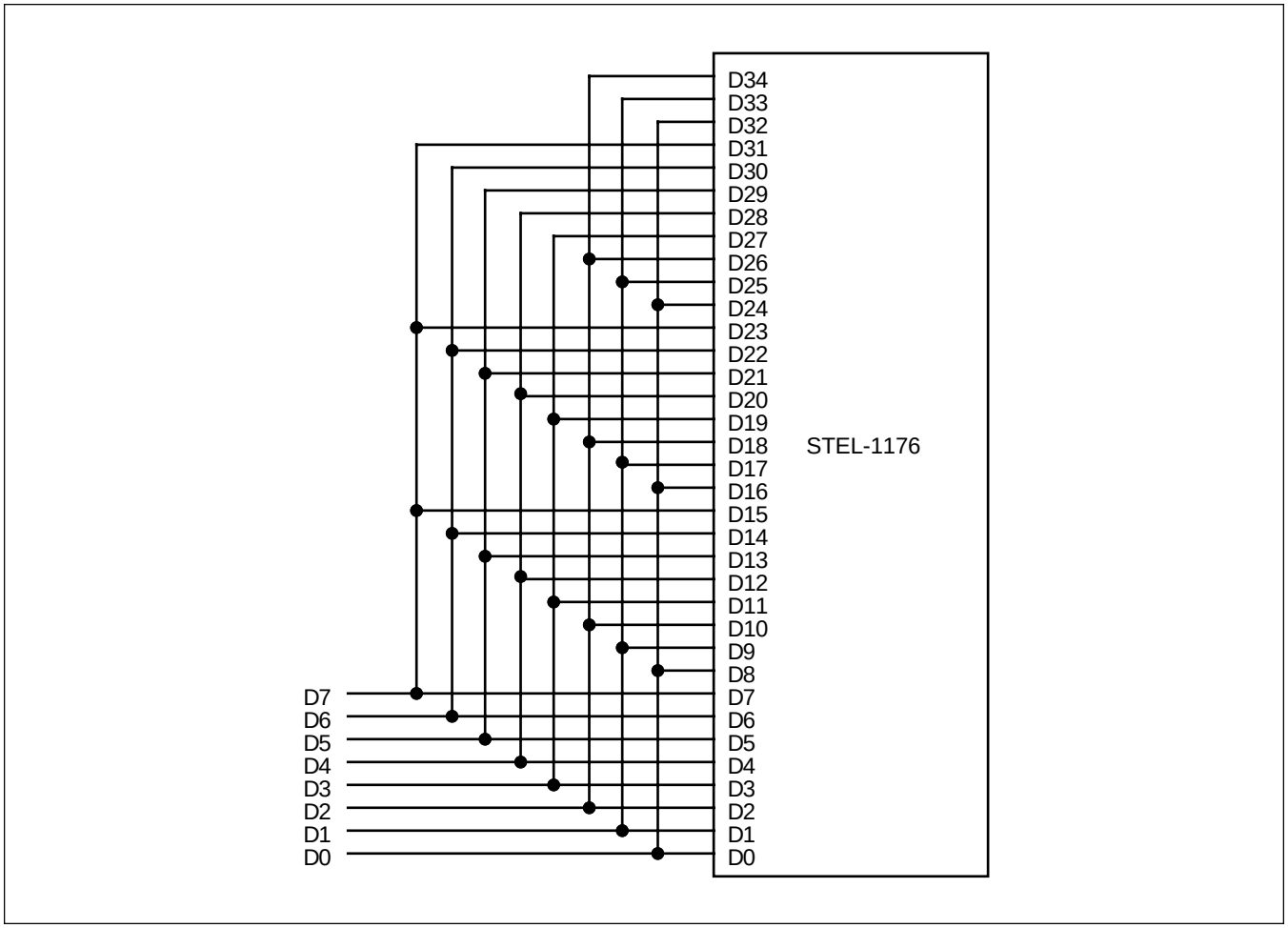
A.C. CHARACTERISTICS (Operating Conditions: V_{DD}= 5.0 V ± 5%, V_{SS}=0 V, T_a= 0° to 50° C, Commerical V_{DD}= 5.0 V ± 10%, V_{SS}=0 V, T_a=–55° to 125° C, Military)

Symbol	Parameter	Commercial			Military			Units	Conditions
		Min.	Typ.	Max.	Min.	Typ.	Max.		
t_{RS}	**RESET** pulse width	20			25			nsec.	
t_{SR}	**RESET** to **CLOCK** Setup	8			12			nsec.	
t_{SU}	**DATA**, **ADDR** or **CSEL** to **WRSTB** Setup, and **FRLD** or **PHLD** to **CLOCK** Setup	6			8			nsec.	
t_{HD}	**DATA**, **ADDR** or **CSEL** to **WRSTB** Hold, and **FRLD** or **PHLD** to **CLOCK** Hold	3			5			nsec.	
t_{CH}	**CLOCK** high	5						nsec.	f_{CLK} = 80 MHz
t_{CL}	**CLOCK** low	5						nsec.	f_{CLK} = 80 MHz
t_{CH}	**CLOCK** high				8			nsec.	f_{CLK} = 60 MHz
t_{CL}	**CLOCK** low				8			nsec.	f_{CLK} = 60 MHz
t_W	**WRSTB**, **FRLD** or **PHLD** pulse width	5			8			nsec.	
t_{CO}	**CLOCK** to output delay	7		14	3		20	nsec.	Load = 15 pF
t_{CC}	**CLOCK** to **LDCLK** delay	7		20	3		28	nsec.	Load = 15 pF
t_{CR}	**CLOCK** to **REFCLK** delay	7		17	3		25	nsec.	Load = 15 pF

APPLICATIONS INFORMATION: LOCKING THE 80 MHz CLOCK GENERATOR FOR THE STEL-1176 TO A 10 MHz REFERENCE



APPLICATIONS INFORMATION: DATA BUS CONNECTIONS FOR DATA LOADING IN THE BYTE-WIDE MODE



SPECTRAL PURITY

In many applications the NCO is used with a digital to analog converter (DAC) to generate an analog waveform which approximates an ideal sinewave. The spectral purity of this synthesized waveform is a function of many variables including the phase and amplitude quantization, the ratio of the clock frequency to output frequency, and the dynamic characteristics of the DAC.

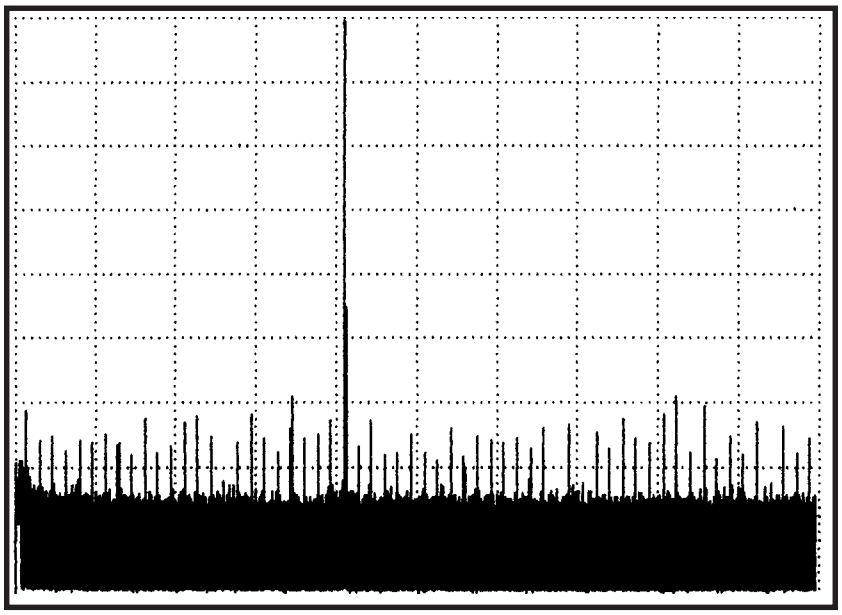
The sine signals generated by the STEL-1176 have 12 bits of amplitude resolution and 15 BCD bits of phase resolution which results in spurious levels which are theoretically at least 72 dB down. The highest output frequency the NCO can generate is half the clock frequency ($f_c/2$), and the spurious components at frequencies greater than $f_c/2$ can be removed by filtering. As the output frequency f_o of the NCO

approaches $f_c/2$, the "image" spur at $f_c - f_o$ (created by the sampling process) also approaches $f_c/2$ from above. If the programmed output frequency is very close to $f_c/2$ it will be virtually impossible to remove this image spur by filtering. For this reason, the maximum practical output frequency of the NCO should be limited to about 40% of the clock frequency.

A spectral plot of the NCO output after conversion with a DAC (Sony CX20202A-1) is shown below. In this case, the clock frequency is 80 MHz and the output frequency is programmed to 12.3456789 MHz. This 10-bit DAC gives better performance than any of the currently available 12-bit DACs at clock frequencies higher than 10 or 20 MHz. The maximum non-harmonic spur level observed over the output frequency range shown in this case is –59 dBc. The spur levels are limited by the dynamic linearity of the DAC. It is important to remember that when the output frequency exceeds 25% of the clock frequency, the second harmonic frequency will be higher than the Nyquist frequency, 50% of the clock frequency. When this happens, the image of the harmonic at the frequency $f_c - 2f_o$, which is not harmonically related to the output signal, will become intrusive since its frequency falls as the output frequency rises, eventually crossing the fundamental output when its frequency crosses through $f_c/3$. It would be necessary to select a DAC with better dynamic linearity to improve the harmonic spur levels. (The dynamic linearity of a DAC is a function of both its static linearity and its dynamic characteristics, such as settling time and slew rates.) At higher output frequencies the waveform produced by the DAC will have large output changes from sample to sample. For this reason, the settling time of the DAC should be short in comparison to the clock period. As a general rule, the DAC used should have the lowest possible glitch energy as well as the shortest possible settling time.

TYPICAL SPECTRUM

Center Frequency:	15.0 MHz
Frequency Span:	30.0 MHz
Reference Level:	–10 dBm
Resolution Bandwidth:	1 KHz
Scale:	Log, 10 dB/div
Output frequency:	12.3456789 MHz
Clock frequency:	80 MHz



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