

## Digitally Controlled Potentiometer (XDCP™)

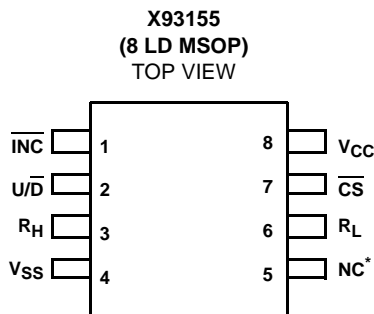
The Intersil X93155 is a digitally controlled potentiometer (XDCP). The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a 3-wire interface.

The potentiometer is implemented by a resistor array composed of 31 resistive elements and a wiper switching network. The position of the wiper element is controlled by the  $\overline{CS}$ , U/D, and INC inputs. The position of the wiper can be stored in nonvolatile memory and then be recalled upon during a subsequent power-up operation.

The device is connected as a two-terminal variable resistor and can be used in a wide variety of applications including:

- Bias and Gain Control
- LCD Contrast Adjustment

### Pinout



\*NC can be left unconnected, or connected to any voltage between  $V_{SS}$  and  $V_{CC}$ .

### Ordering Information

PART NUMBER	PART MARKING	$V_{CC}$ LIMITS (V)	$R_{TOTAL}$ (k $\Omega$ )	TEMP RANGE (°C)	PACKAGE	PKG DWG. #
X93155UM8I*	AGM	5 $\pm$ 10%	50	-40 to +85	8 Ld MSOP	M8.118
X93155UM8IZ* (Note)	DCH			-40 to +85	8 Ld MSOP (Pb-free)	M8.118

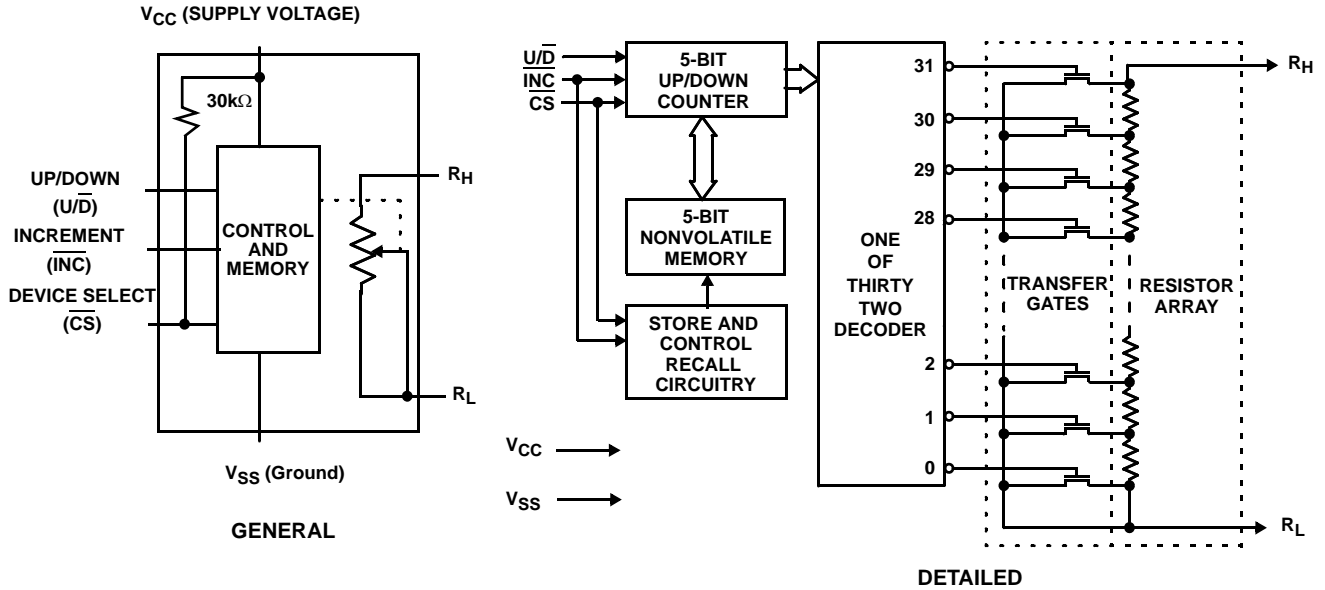
\*Add "T1" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

### Features

- Solid-state potentiometer
- Up/Down interface
- 32 wiper tap points per potentiometer
  - Wiper position stored in nonvolatile memory and recalled on power-up
- 31 resistive elements per potentiometer
  - Temperature compensated
  - Maximum resistance tolerance  $\pm$ 25%
  - Terminal voltage, 0 to  $V_{CC}$
- Low power CMOS
  - $V_{CC}$  = 5V  $\pm$ 10%
  - Active current, 200 $\mu$ A typ.
  - Standby current, 2.0 $\mu$ A max
- High reliability
  - Endurance 200,000 data changes per bit
  - Register data retention, 100 years
- $R_{TOTAL}$  value = 50k $\Omega$
- Packages
  - 8 Ld MSOP
- Pb-free available (RoHS compliant)

**Block Diagram**



**Pin Descriptions**

MSOP	SYMBOL	BRIEF DESCRIPTION
1	$\overline{\text{INC}}$	<b>Increment (<math>\overline{\text{INC}}</math>).</b> The $\overline{\text{INC}}$ input is negative-edge triggered. Toggling $\overline{\text{INC}}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the $\text{U}/\overline{\text{D}}$ input.
2	$\text{U}/\overline{\text{D}}$	<b>Up/Down (<math>\text{U}/\overline{\text{D}}</math>).</b> The $\text{U}/\overline{\text{D}}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.
3	$\text{R}_\text{H}$	<b><math>\text{R}_\text{H}</math>.</b> The $\text{R}_\text{H}$ and $\text{R}_\text{L}$ pins of the X93155 are equivalent to the end terminals of a variable resistor.
4	$\text{V}_\text{SS}$	<b>Ground.</b>
5	NC	<b>No Connection</b> (or can be connected to any voltage between $\text{V}_\text{SS}$ and $\text{V}_\text{CC}$ .)
6	$\text{R}_\text{L}$	<b><math>\text{R}_\text{L}</math>.</b> The $\text{R}_\text{H}$ and $\text{R}_\text{L}$ pins of the X93155 are equivalent to the end terminals of a variable resistor.
7	$\overline{\text{CS}}$	<b>Chip Select (<math>\overline{\text{CS}}</math>).</b> The device is selected when the $\overline{\text{CS}}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{\text{CS}}$ is returned HIGH while the $\overline{\text{INC}}$ input is also HIGH. After the store operation is complete, the X93155 will be placed in the low power standby mode until the device is selected once again.
8	$\text{V}_\text{CC}$	<b>Supply Voltage.</b>

**Absolute Maximum Ratings**

Voltage on  $\overline{CS}$ ,  $\overline{INC}$ ,  $U/\overline{D}$ ,  $R_H$ ,  $R_L$  and  $V_{CC}$   
 with respect to  $V_{SS}$  ..... -1V to +6.5V  
 Maximum resistor current ..... 2mA

**Thermal Information**

Temperature under bias. .... -65°C to +135°C  
 Storage temperature ..... -65°C to +150°C  
 Maximum reflow temperature (40s) ..... +240°C  
 Pb-free reflow profile ..... see link below  
<http://www.intersil.com/pbfree/Pb-FreeReflow.asp>

**Recommended Operating Conditions**

Temperature Range  
 Industrial ..... -40°C to +85°C  
 Supply Voltage  
 $V_{CC}$  ..... .5V  $\pm$ 10% (Note 6)

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

**NOTES:**

1. Absolute linearity is utilized to determine actual wiper resistance versus expected resistance =  $(R_{H(n)}(\text{actual}) - R_{H(n)}(\text{expected})) = \pm 1 \text{ MI}$  Maximum.  $n = 1 \dots 29$  only
2. Relative linearity is a measure of the error in step size between taps =  $R_{H(n+1)} - [R_{H(n)} + \text{MI}] = \pm 0.5 \text{ MI}$ ,  $n = 1 \dots 29$  only.
3. 1 MI = Minimum Increment =  $R_{TOT}/31$ .
4. Typical values are for  $T_A = +25^\circ\text{C}$  and nominal supply voltage.
5. Limits established by characterization and are not production tested.
6. When performing multiple write operations,  $V_{CC}$  must not decrease by more than 150mV from its initial value.
7. Parts are 100% tested at +25°C. Over-temperature limits established by characterization and are not production tested.

**Potentiometer Specifications** Over recommended operating conditions, unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS/NOTES	MIN (Note 7)	TYP (Note 4)	MAX (Note 7)	UNIT
$R_{TOT}$	End-to-end Resistance		37.5	50	62.5	k $\Omega$
$V_R$	$R_H$ , $R_L$ Terminal Voltages		0		$V_{CC}$	V
	Power Rating	$R_{TOTAL} = 50\text{k}\Omega$			1	mW (Note 5)
	Noise	Ref: 1kHz		-120		dBV (Note 5)
$I_R$	Potentiometer Current	(Note 5)			0.6	mA
	Resolution			3		%
	Absolute linearity (Note 1)	$R_{H(n)}(\text{actual}) - R_{H(n)}(\text{expected})$			$\pm 1$	MI (Note 3)
	Relative linearity (Note 2)	$R_{H(n+1)} - [R_{H(n)} + \text{MI}]$			$\pm 0.5$	MI (Note 3)
	$R_{TOTAL}$ Temperature Coefficient	(Note 5)		$\pm 35$		ppm/ $^\circ\text{C}$
$C_H/C_L/C_W$	Potentiometer Capacitances	See "Circuit #2 SPICE Macro Model" on page 4		10/10/25		pF (Note 5)

**DC Electrical Specifications** Over recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP (Note 4)	MAX (Note 7)	UNIT
$I_{CC1}$	$V_{CC}$ Active Current (Increment)	$\overline{CS} = V_{IL}$ , $U/\overline{D} = V_{IL}$ or $V_{IH}$ and $\overline{INC} = 0.4\text{V}$ @ max. $t_{CYC}$		200	300	$\mu\text{A}$
$I_{CC2}$	$V_{CC}$ Active Current (Store) (EEPROM Store)	$\overline{CS} = V_{IH}$ , $U/\overline{D} = V_{IL}$ or $V_{IH}$ and $\overline{INC} = V_{IH}$ @ max. $t_{WR}$			1400	$\mu\text{A}$
$I_{SB}$	Standby Supply Current	$\overline{CS} = V_{CC} - 0.3\text{V}$ , $U/\overline{D}$ and $\overline{INC} = V_{SS}$ or $V_{CC} - 0.3\text{V}$			2.0	$\mu\text{A}$
$I_{LI}$	$\overline{CS}$	$V_{\overline{CS}} = V_{CC}$			$\pm 1$	$\mu\text{A}$

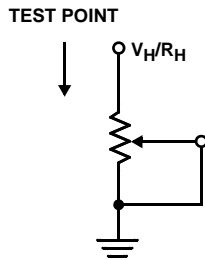
**DC Electrical Specifications** Over recommended operating conditions unless otherwise specified. (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP (Note 4)	MAX (Note 7)	UNIT
$I_{LI}$	$\overline{CS}$	$V_{CC} = 5V, \overline{CS} = 0$	120	200	250	$\mu A$
$I_{LI}$	$\overline{INC}, U/\overline{D}$ Input Leakage Current	$V_{IN} = V_{SS} \text{ to } V_{CC}$			$\pm 1$	$\mu A$
$V_{IH}$	$\overline{CS}, \overline{INC}, U/\overline{D}$ Input HIGH Voltage		$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V
$V_{IL}$	$\overline{CS}, \overline{INC}, U/\overline{D}$ Input LOW Voltage		-0.5		$V_{CC} \times 0.1$	V
$C_{IN}$ (Note 5)	$\overline{CS}, \overline{INC}, U/\overline{D}$ Input Capacitance	$V_{CC} = 5V, V_{IN} = V_{SS}, T_A = +25^\circ C, f = 1MHz$			10	pF

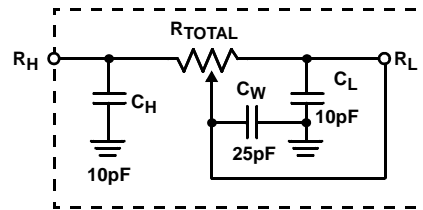
**Endurance and Data Retention**

PARAMETER	MIN	UNIT
Minimum endurance	200,000	Data changes per bit
Data retention	100	Years

**Test Circuit #1**



**Circuit #2 SPICE Macro Model**



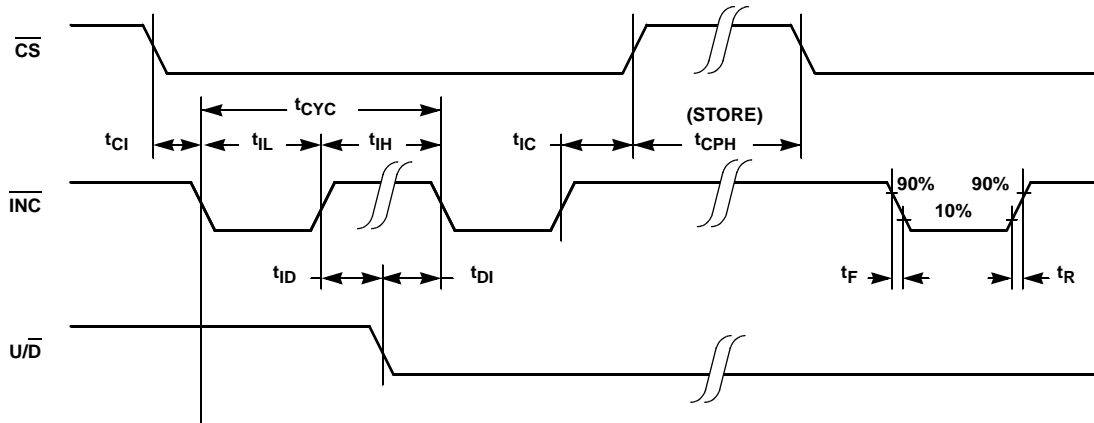
**AC Conditions of Test**

Input pulse levels	0V to 5V
Input rise and fall times	10ns
Input reference levels	1.5V

**AC Electrical Specifications** Over recommended operating conditions, unless otherwise specified.

SYMBOL	PARAMETER	MIN (Note 7)	TYP (Note 4)	MAX (Note 7)	UNIT
$t_{CI}$	$\overline{CS}$ to $\overline{INC}$ Setup	100			ns
$t_{DI}$	$\overline{INC}$ HIGH to $U/\overline{D}$ Change	100			ns
$t_{DI}$	$U/\overline{D}$ to $\overline{INC}$ Setup	100			ns
$t_{IL}$	$\overline{INC}$ LOW Period	1			$\mu s$
$t_{IH}$	$\overline{INC}$ HIGH Period	1			$\mu s$
$t_{IC}$	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1			$\mu s$
$t_{CPH}$	$\overline{CS}$ Deselect Time (No Store)	250			ns
$t_{CPH}$	$\overline{CS}$ Deselect Time (Store)	10			ms
$t_{CYC}$	$\overline{INC}$ Cycle Time	2			$\mu s$
$t_R, t_F$ (Note 5)	$\overline{INC}$ Input Rise and Fall time			500	$\mu s$
$t_R V_{CC}$ (Note 5)	$V_{CC}$ Power-up Rate	1		50	V/ms
$t_{WR}$	Store Cycle		5	10	ms

## AC Timing



## Power-up and Power-down Requirements

There are no restrictions on the power-up or power-down conditions of  $V_{CC}$  and the voltages applied to the potentiometer pins provided that  $V_{CC}$  is always more positive than or equal to  $V_H$  and  $V_L$ , i.e.,  $V_{CC} \geq V_H, V_L$ . The  $V_{CC}$  ramp rate specification is always in effect.

## Pin Descriptions

### $R_H$ and $R_L$

The  $R_H$  and  $R_L$  pins of the X93155 are equivalent to the end terminals of a variable resistor. The minimum voltage is  $V_{SS}$  and the maximum is  $V_{CC}$ . The terminology of  $R_H$  and  $R_L$  references the relative position of the terminal in relation to wiper movement direction selected by the  $U/\bar{D}$  input.

### Up/Down ( $U/\bar{D}$ )

The  $U/\bar{D}$  input controls the direction of the wiper movement and whether the counter is incremented or decremented.

### Increment ( $\bar{INC}$ )

The  $\bar{INC}$  input is negative-edge triggered. Toggling  $\bar{INC}$  will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the  $U/\bar{D}$  input.

### Chip Select ( $\bar{CS}$ )

The device is selected when the  $\bar{CS}$  input is LOW. The current counter value is stored in nonvolatile memory when  $\bar{CS}$  is returned HIGH while the  $\bar{INC}$  input is also HIGH. After the store operation is complete, the X93155 will be placed in the low power standby mode until the device is selected once again.

## Principles of Operation

There are three sections of the X93155: the input control, counter and decode section; the nonvolatile memory; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the

resistor array to the wiper output. Under the proper conditions the contents of the counter can be stored in nonvolatile memory and retained for future use. The resistor array is comprised of 31 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the connection at that point to the wiper. The wiper is connected to the  $R_L$  terminal, forming a variable resistor from  $R_H$  to  $R_L$ .

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

If the wiper is moved several positions, multiple taps are connected to the wiper for up to  $10\mu s$ . The 2-terminal resistance value for the device can temporarily change by a significant amount if the wiper is moved several positions.

When the device is powered-down, the last wiper position stored will be maintained in the nonvolatile memory. When power is restored, the contents of the memory are recalled and the wiper is set to the value last stored.

## Instructions and Programming

The  $\bar{INC}$ ,  $U/\bar{D}$  and  $\bar{CS}$  inputs control the movement of the wiper along the resistor array. With  $\bar{CS}$  set LOW, the device is selected and enabled to respond to the  $U/\bar{D}$  and  $\bar{INC}$  inputs. HIGH to LOW transitions on  $\bar{INC}$  will increment or decrement (depending on the state of the  $U/\bar{D}$  input) a five bit counter. The output of this counter is decoded to select one of thirty two wiper positions along the resistive array.

The value of the counter is stored in nonvolatile memory whenever  $\bar{CS}$  transitions HIGH while the  $\bar{INC}$  input is also HIGH. In order to avoid an accidental store during power-up,  $\bar{CS}$  must go HIGH with  $V_{CC}$  during initial power-up. When left open, the  $\bar{CS}$  pin is internally pulled up to  $V_{CC}$  by an internal  $30k\Omega$  resistor.

The system may select the X93155, move the wiper and deselect the device without having to store the latest wiper

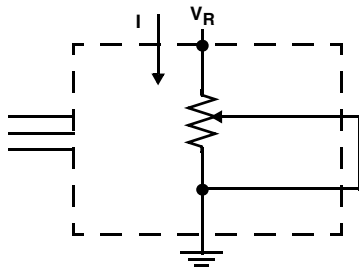
position in nonvolatile memory. After the wiper movement is performed as previously described and once the new position is reached, the system must keep  $\overline{INC}$  LOW while taking  $\overline{CS}$  HIGH. The new wiper position will be maintained until changed by the system or until a power-up/down cycle recalled the previously stored data. In order to recall the stored position of the wiper on power-up, the  $\overline{CS}$  pin must be held HIGH.

This procedure allows the system to always power-up to a preset value stored in nonvolatile memory; then during system operation, minor adjustments could be made. The adjustments might be based on user preference, system parameter changes due to temperature drift, or other system trim requirements.

The state of  $U/\overline{D}$  may be changed while  $\overline{CS}$  remains LOW. This allows the host system to enable the device and then move the wiper up and down until the proper trim is attained.

**Mode Selection**

$\overline{CS}$	$\overline{INC}$	$U/\overline{D}$	MODE
L		H	Wiper Up
L		L	Wiper Down
	H	X	Store Wiper Position
H	X	X	Standby Current
	L	X	No Store, Return to Standby
	L	H	Wiper Up (not recommended)
	L	L	Wiper Down (not recommended)



Two terminal variable resistor.

**Symbol Table**

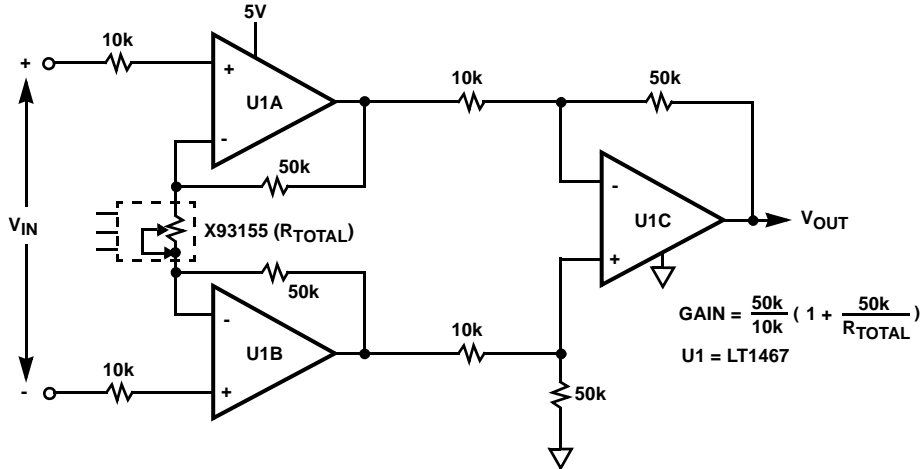
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

**Applications Information**

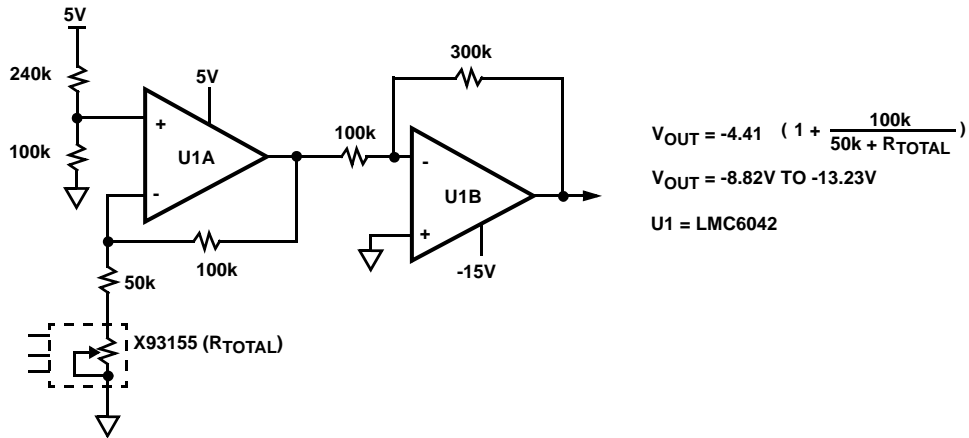
Electronic digitally controlled (XDCCP) potentiometers provide three powerful application advantages:

1. The variability and reliability of a solid-state potentiometer
2. The flexibility of computer-based digital controls
3. The retentivity of nonvolatile memory used for the storage of multiple potentiometer settings or data

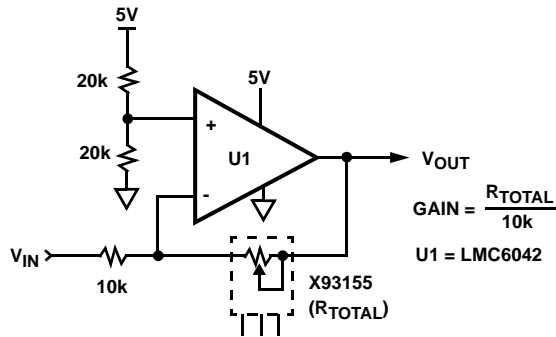
**Low Voltage High Impedance Instrumentation Amplifier**



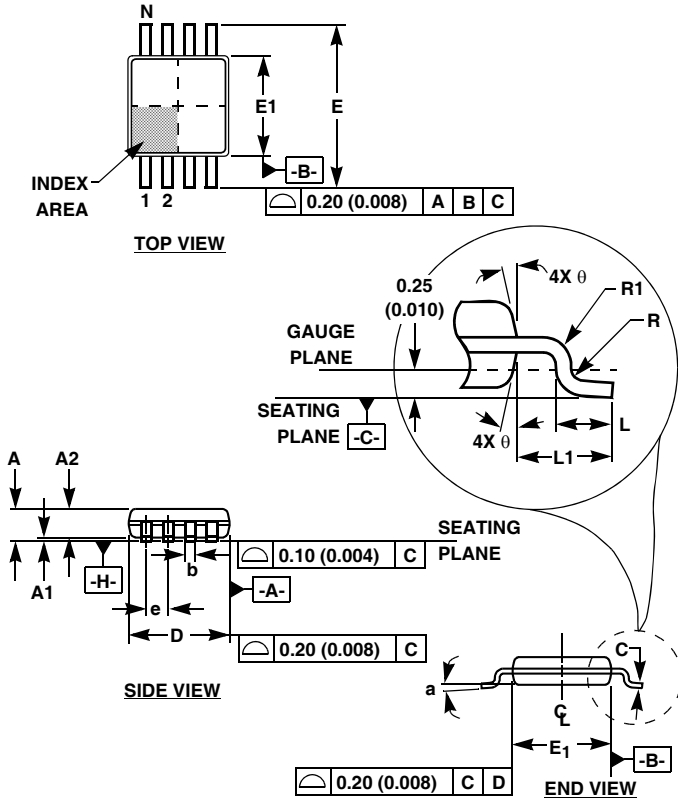
**Micro-Power LCD Contrast Control**



**Single Supply Variable Gain Amplifier**



Mini Small Outline Plastic Packages (MSOP)



M8.118 (JEDEC MO-187AA)  
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.010	0.014	0.25	0.36	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.026 BSC		0.65 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	8		8		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
theta	5°	15°	5°	15°	-
alpha	0°	6°	0°	6°	-

Rev. 2 01/03

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension "D" does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E1" does not include interlead flash or protrusions and are measured at Datum Plane. [-H-] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (0.004) at seating Plane.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A-] and [-B-] to be determined at Datum plane [-H-].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.  
Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

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