SONY

CXK5T81000ATN/AYN -10LLX/12LLX

131072-word × 8-bit High Speed CMOS Static RAM *Preliminary*

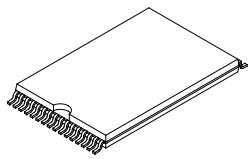
Description

The CXK5T81000ATN/AYN is a high speed CMOS static RAM organized as 131072-words by 8-bits.

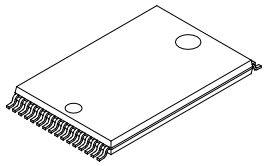
Special feature are low power consumption and high speed.

The CXK5T81000ATN/AYN is a suitable RAM for portable equipment with battery back up.

CXK5T81000ATN
32 pin TSOP (Plastic)



CXK5T81000AYN
32 pin TSOP (Plastic)



Features

- Extended operating temperature range: –25 to +85°C
- Wide supply voltage range operation: 2.7 to 3.6V
- Fast access time: (Access time)

3.0V operation	-10LLX	100ns	(Max.)
	-12LLX	120ns	(Max.)
3.3V operation	-10LLX	85ns	(Max.)
	-12LLX	100ns	(Max.)

- Low standby current: 28µA (Max.)
- Low data retention current: 24µA (Max.)
- Low power data retention: 2.0V (Min.)
- Package 8mm × 13.4mm 32 pin TSOP package

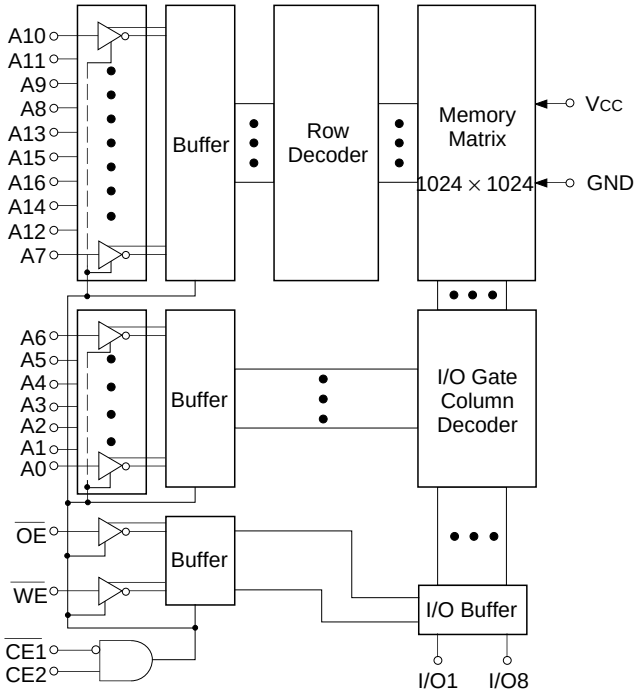
Function

131072-word × 8-bit static RAM

Structure

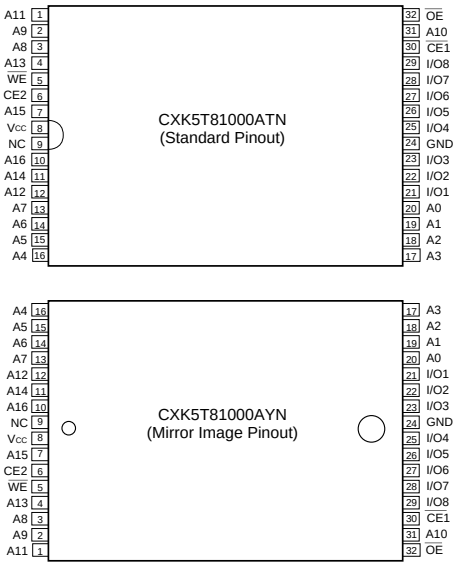
Silicon gate CMOS IC

Block Diagram



PE96726-PS

Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A16	Address input
I/O1 to I/O8	Data input output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
V_{CC}	Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings (Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.5 to +4.6	V
Input voltage	V_{IN}	–0.5*1 to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$	–0.5*1 to V_{CC} + 0.5	V
Allowable power dissipation	P_D	0.7	W
Operating temperature	Topr	–25 to +85	°C
Storage temperature	Tstg	–55 to +150	°C
Soldering temperature · time	Tsolder	235 · 10	°C · s

*1 V_{IN}, $V_{I/O}$ = –3.0V Min. for pulse width less than 50ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O pin	V_{CC} Current
H	×	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}, I_{CC3}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}, I_{CC3}
L	H	×	L	Write	Data in	I_{CC1}, I_{CC2}, I_{CC3}

× : "H" or "L"

DC Recommended Operating Conditions (Ta = –25 to +85°C, GND = 0V)

Item	Symbol	V_{CC} = 2.7 to 3.6V			V_{CC} = 3.3V ± 0.3V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	V_{CC}	2.7	3.3	3.6	3.0	3.3	3.6	V
Input high voltage	V_{IH}	2.4	—	V_{CC} + 0.3	2.2	—	V_{CC} + 0.3	
Input low voltage	V_{IL}	–0.3*2	—	0.4	–0.3*2	—	0.6	

*2 V_{IL} = –3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

• DC Characteristics (V_{CC} = 2.7 to 3.6V, GND = 0V, Ta = –25 to +85°C)

Item	Symbol	Test conditions		Min.	Typ.*1	Max.	Unit
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}		–1	—	+1	µA
Output leakage current	I_{LO}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to V_{CC}		–1	—	+1	µA
Operating power supply current	I_{CC1}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} V_{IN} = V_{IH} or V_{IL} I_{OUT} = 0mA		—	1	3	mA
Average operating current	I_{CC2}	Min. cycle duty = 100% I_{OUT} = 0mA	10LLX	—	25*2	35*3	mA
			12LLX	—	25	35	
	I_{CC3}	Cycle time 1µs duty = 100% I_{OUT} = 0mA $\overline{CE1}$ ≤ 0.2V CE2 ≥ Vcc – 0.2V V_{IL} ≤ 0.2V V_{IH} ≥ Vcc – 0.2V		—	5	10	mA
Standby current	I_{SB1}	CE2 ≤ 0.2V or { $\overline{CE1}$ ≥ Vcc – 0.2V, CE2 ≥ Vcc – 0.2V }	–25 to +85°C	—	—	28	µA
			–25 to +70°C	—	—	14	
			+25°C	—	0.48	—	
	I_{SB2}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}		—	0.12	1.4	mA
Output high voltage	V_{OH}	I_{OH} = –2.0mA		2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 2.0mA		—	—	0.4	V

*1 V_{CC} = 3.3V, Ta = 25°C

*2 I_{CC2} = 30mA for 3.3V operation (V_{CC} = 3.3V ± 0.3V)

*3 I_{CC2} = 40mA for 3.3V operation (V_{CC} = 3.3V ± 0.3V)

I/O capacitance (Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	—	8	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	10	pF

Note) This parameter is sampled and is not 100% tested.

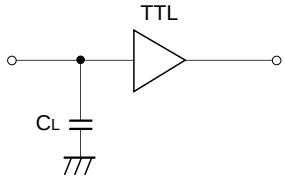
AC Characteristics

• AC test conditions

(Ta = –25 to +85°C)

Item		Conditions	
		V_{CC} = 2.7 to 3.6V	V_{CC} = 3.3V ± 0.3V
Input pulse high level		V_{IH} = 2.4V	V_{IH} = 2.2V
Input pulse low level		V_{IL} = 0.4V	V_{IL} = 0.6V
Input rise time		tr = 5ns	tr = 5ns
Input fall time		tf = 5ns	tf = 5ns
Input and output reference level		1.4V	1.4V
Output load conditions	-10LLX	C_L*1 = 100pF, 1TTL	C_L*1 = 30pF, 1TTL
	-12LLX	C_L*1 = 100pF, 1TTL	C_L*1 = 100pF, 1TTL

• Test circuit



*1 C_L includes scope and jig capacitances.

• **Read cycle** ($\overline{WE}$ = "H")

Item	Symbol	V_{CC} = 2.7 to 3.6V				V_{CC} = 3.3V ± 0.3V				Unit
		-10LLX		-12LLX		-10LLX		-12LLX		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	100	—	120	—	85	—	100	—	ns
Address access time	t_{AA}	—	100	—	120	—	85	—	100	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	100	—	120	—	85	—	100	ns
Chip enable access time (CE2)	t_{CO2}	—	100	—	120	—	85	—	100	ns
Output enable to output valid	t_{OE}	—	50	—	60	—	40	—	50	ns
Output hold from address change	t_{OH}	10	—	10	—	10	—	10	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1} t_{LZ2}	10	—	10	—	10	—	10	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}	5	—	5	—	5	—	5	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}*1 t_{HZ2}*1	—	40	—	40	—	35	—	40	ns
Output disable to output in high Z ($\overline{OE}$)	t_{OHZ}*1	—	35	—	35	—	30	—	35	ns

*1 t_{HZ1}, t_{HZ2} and t_{OHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

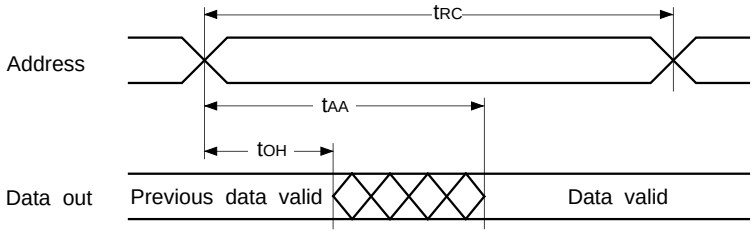
• **Write cycle**

Item	Symbol	V_{CC} = 2.7 to 3.6V				V_{CC} = 3.3V ± 0.3V				Unit
		-10LLX		-12LLX		-10LLX		-12LLX		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	100	—	120	—	85	—	100	—	ns
Address valid to end of write	t_{AW}	80	—	100	—	70	—	80	—	ns
Chip enable to end of write	t_{CW}	80	—	100	—	70	—	80	—	ns
Data to write time overlap	t_{DW}	40	—	50	—	35	—	40	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	70	—	70	—	60	—	70	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}	5	—	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*2	—	40	—	40	—	35	—	40	ns

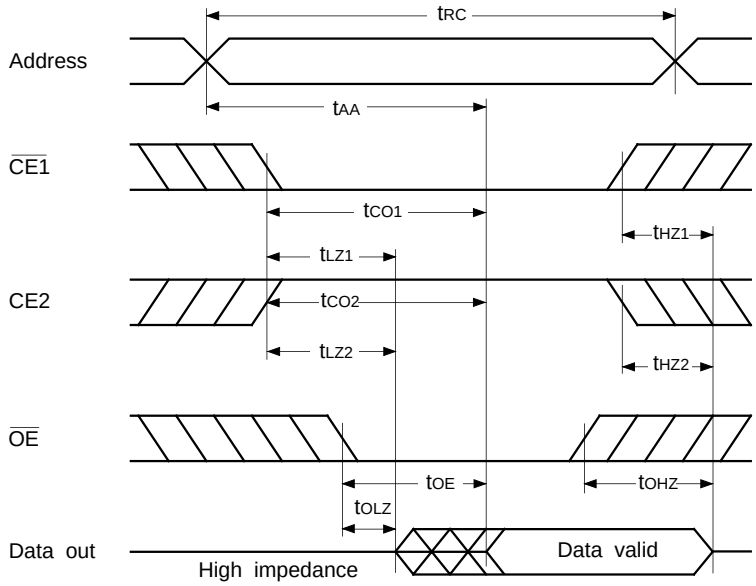
*2 t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage level.

Timing Waveform

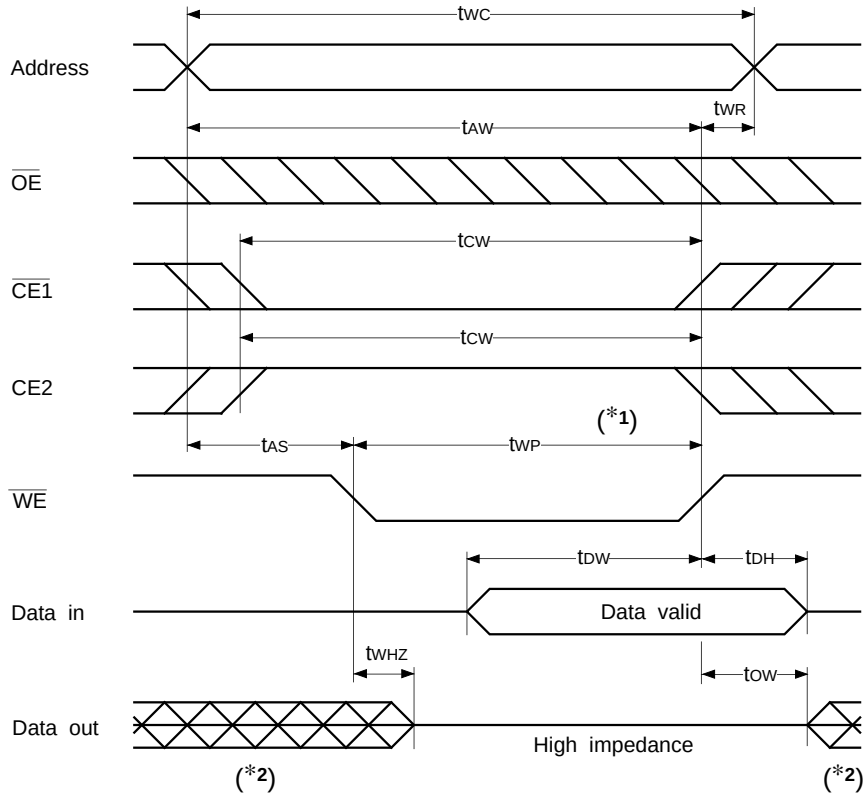
• **Read cycle (1) :** $\overline{CE1}$ = $\overline{OE}$ = V_{IL}, CE2 = V_{IH}, $\overline{WE}$ = V_{IH}



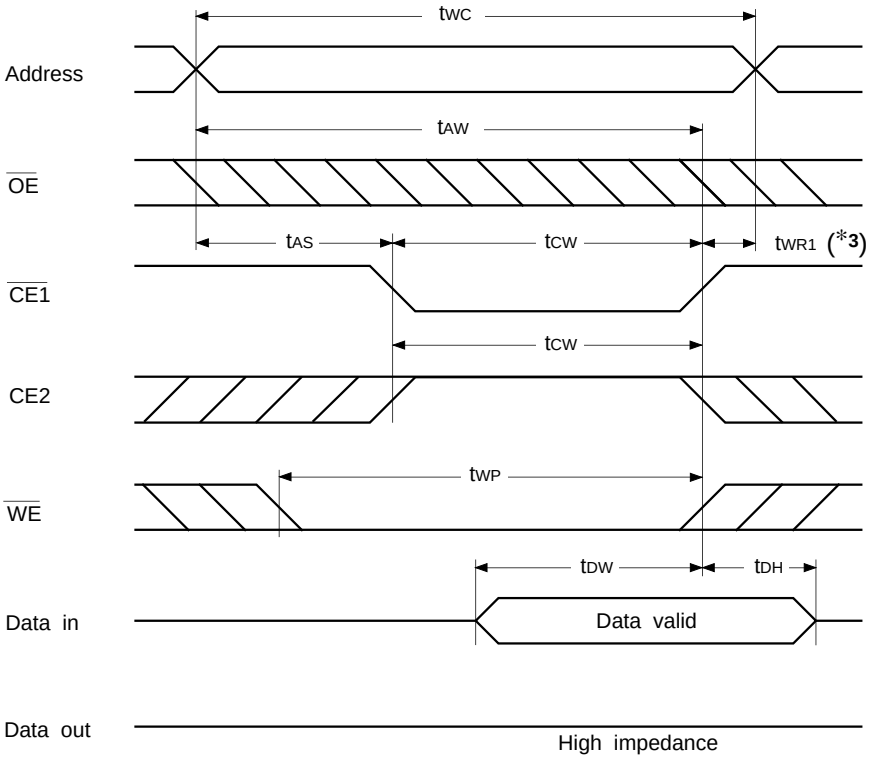
• **Read cycle (2) :** $\overline{WE}$ = V_{IH}



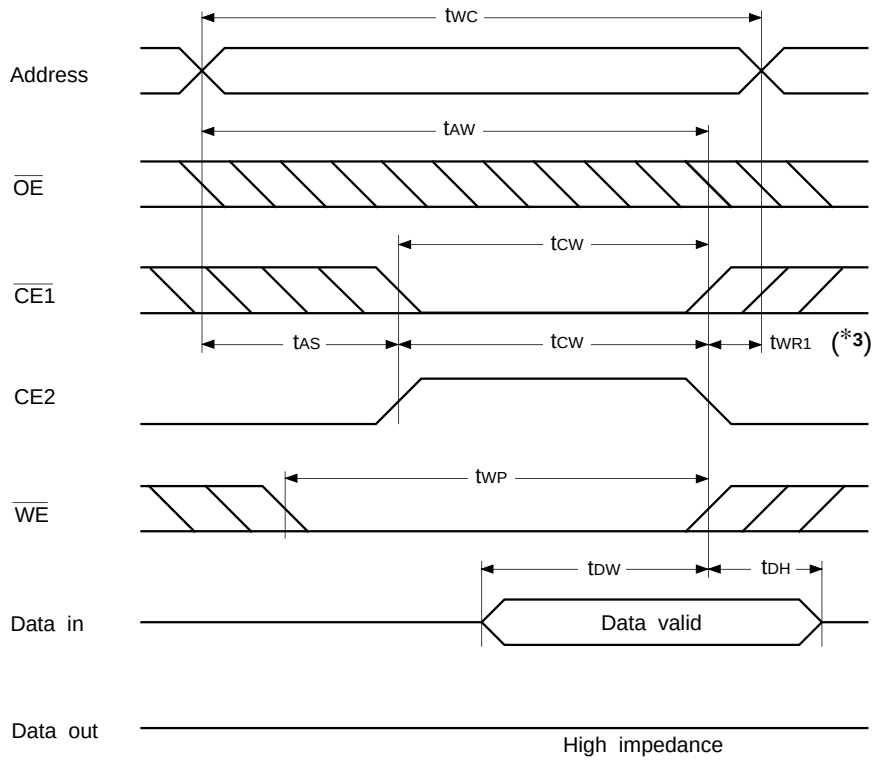
• **Write cycle (1) :** $\overline{WE}$ control



• **Write cycle (2) :** $\overline{CE1}$ control



• **Write cycle (3) :** CE2 control



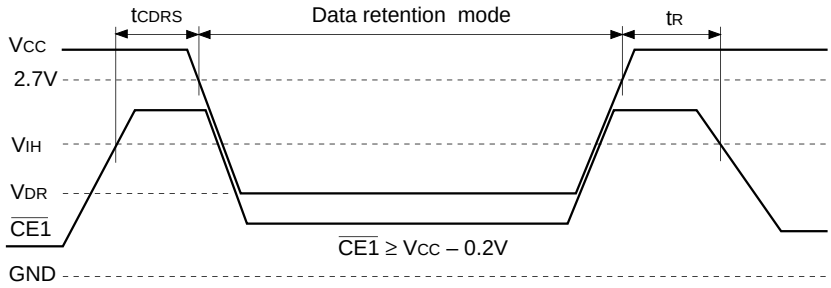
*1 Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.

*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

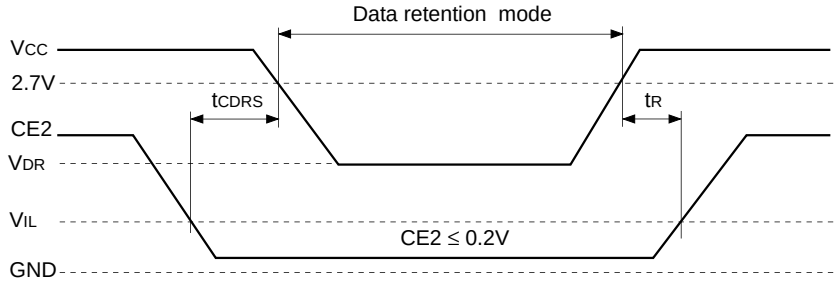
*3 t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

Data retention waveform

• **Low supply voltage data retention waveform (1)** ($\overline{CE1}$ contol)



• **Low supply voltage data retention waveform (2)** (CE2 contol)



Data Retention Characteristics (Ta = –25 to +85°C)

Item	Symbol	Test conditions		Min.	Typ.	Max.	Unit
Data retention voltage	V_{DR}	*1		2.0	—	3.6	V
Data retention current	I_{CCDR1}	V_{CC} = 3.0V*1	–25 to +85°C	—	—	24	µA
			–25 to +70°C	—	—	12	
			+25°C	—	0.4	—	
	I_{CCDR2}	V_{CC} = 2.0 to 3.6V*1		—	0.48*2	28	µA
Data retention setup time	t_{CDRS}	Chip disable to data retention mode		0	—	—	ns
Recovery time	t_R			5	—	—	ns

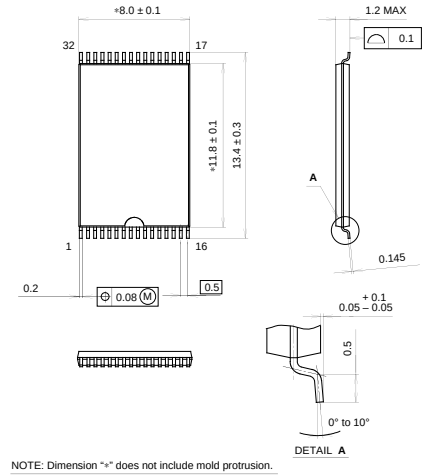
*1 $\overline{CE1}$ ≥ Vcc – 0.2V, CE2 ≥ Vcc – 0.2V ($\overline{CE1}$ control) or CE2 ≤ 0.2V (CE2 control)

*2 V_{CC} = 3.3V, Ta = 25°C

Package Outline Unit: mm

CXK5T81000ATN

32PIN TSOP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

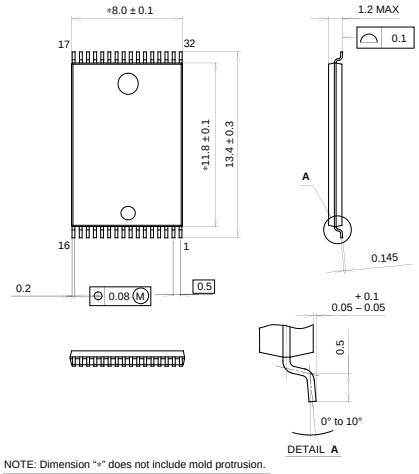
SONY CODE	TSOP-32P-L02
EIAJ CODE	TSOP032-P-0813.4-C
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.2g

CXK5T81000AYN

32PIN TSOP (PLASTIC)



NOTE: Dimension "*" does not include mold protrusion.

SONY CODE	TSOP-32P-L02R
EIAJ CODE	TSOP032-P-0813.4-D
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.2g