



## STB9NB50

### N-CHANNEL 500V - 0.75 $\Omega$ - 8.6A D<sup>2</sup>PAK STripFET™ POWER MOSFET

| TYPE     | V <sub>DSS</sub> | R <sub>DS(on)</sub> | I <sub>D</sub> |
|----------|------------------|---------------------|----------------|
| STB9NB50 | 500 V            | <0.85 $\Omega$      | 8.6 A          |

- TYPICAL R<sub>DS(on)</sub> = 0.75  $\Omega$
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100 °C
- VERY LOW INTRINSIC CAPACITANCE
- GATE CHARGE MINIMIZED
- LOW LEAKAGE CURRENT
- APPLICATION ORIENTED
- FOR THROUGH-HOLE VERSION CONTACT SALES OFFICE

#### DESCRIPTION

This Power Mosfet is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

#### APPLICATIONS

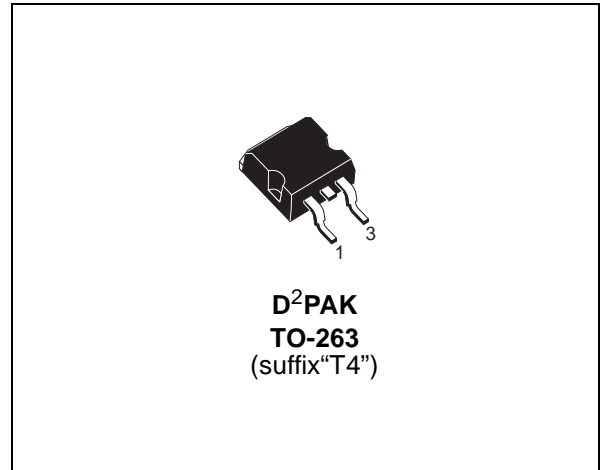
- HIGH CURRENT, HIGH SPEED SWITCHING
- SWITCH MODE POWER SUPPLY (SMPS)
- DC-AC CONVERTER FOR WELDING EQUIPMENT AND UNINTERRUPTABLE POWER SUPPLY (UPS)

#### ABSOLUTE MAXIMUM RATINGS

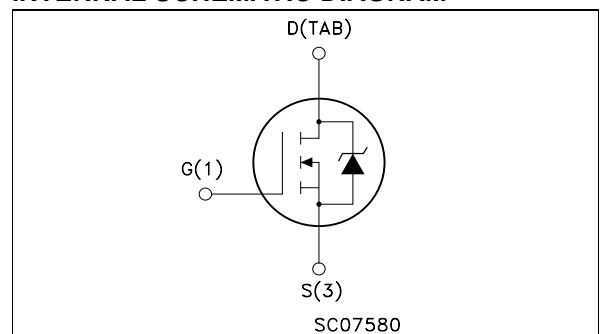
| Symbol              | Parameter   | Value      | Unit |
|---------------------|---|------------|------|
| V <sub>DS</sub>     | Drain-source Voltage (V <sub>GS</sub> = 0)            | 500        | V    |
| V <sub>DGR</sub>    | Drain-gate Voltage (R <sub>GS</sub> = 20 k $\Omega$ ) | 500        | V    |
| V <sub>GS</sub>     | Gate- source Voltage                                  | $\pm 30$   | V    |
| I <sub>D</sub>      | Drain Current (continuous) at T <sub>C</sub> = 25°C   | 8.6        | A    |
| I <sub>D</sub>      | Drain Current (continuous) at T <sub>C</sub> = 100°C  | 5.4        | A    |
| I <sub>DM</sub> (●) | Drain Current (pulsed)                                | 34.4       | A    |
| P <sub>tot</sub>    | Total Dissipation at T <sub>C</sub> = 25°C            | 125        | W    |
|                     | Derating Factor                                       | 1.0        | W/°C |
| dv/dt (2)           | Peak Diode Recovery voltage slope                     | 4.5        | V/ns |
| T <sub>stg</sub>    | Storage Temperature                                   | -60 to 150 | °C   |
| T <sub>j</sub>      | Max. Operating Junction Temperature                   | 150        | °C   |

(●) Pulse width limited by safe operating area.

(2) I<sub>SD</sub>  $\leq$  9A, di/dt  $\leq$  200A/ $\mu$ s, V<sub>DD</sub>  $\leq$  V<sub>(BR)DSS</sub>, T<sub>j</sub>  $\leq$  T<sub>JMAX</sub>.



#### INTERNAL SCHEMATIC DIAGRAM



## STB9NB50

### THERMAL DATA

|                |  |     |      |      |
|----------------|--|-----|------|------|
| $R_{thj-case}$ | Thermal Resistance Junction-case               | Max | 1    | °C/W |
| $R_{thj-amb}$  | Thermal Resistance Junction-ambient            | Max | 62.5 | °C/W |
| $R_{thc-sink}$ | Thermal Resistance Case-sink                   | Typ | 0.5  | °C/W |
| $T_j$          | Maximum Lead Temperature For Soldering Purpose |     | 300  | °C   |

### AVALANCHE CHARACTERISTICS

| Symbol   | Parameter  | Max Value | Unit |
|----------|--|-----------|------|
| $I_{AR}$ | Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max)                       | 8.6       | A    |
| $E_{AS}$ | Single Pulse Avalanche Energy (starting $T_j = 25\text{ °C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ ) | 520       | mJ   |

### ELECTRICAL CHARACTERISTICS ( $T_{case} = 25\text{ °C}$ unless otherwise specified)

#### OFF

| Symbol        | Parameter  | Test Conditions  | Min. | Typ. | Max.      | Unit                           |
|---------------|--|--|------|------|-----------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source Breakdown Voltage                   | $I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0$  | 500  |      |           | V                              |
| $I_{DSS}$     | Zero Gate Voltage Drain Current ( $V_{GS} = 0$ ) | $V_{DS} = \text{Max Rating}$<br>$V_{DS} = \text{Max Rating}$ , $T_C = 125\text{ °C}$ |      |      | 1<br>50   | $\mu\text{A}$<br>$\mu\text{A}$ |
| $I_{GSS}$     | Gate-body Leakage Current ( $V_{DS} = 0$ )       | $V_{GS} = \pm 30\text{ V}$   |      |      | $\pm 100$ | nA                             |

#### ON (1)

| Symbol       | Parameter                         | Test Conditions   | Min. | Typ. | Max. | Unit     |
|--------------|-----------------------------------|---|------|------|------|----------|
| $V_{GS(th)}$ | Gate Threshold Voltage            | $V_{DS} = V_{GS}$ $I_D = 250\text{ }\mu\text{A}$                    | 3    | 4    | 5    | V        |
| $R_{DS(on)}$ | Static Drain-source On Resistance | $V_{GS} = 10\text{ V}$ $I_D = 4.3\text{ A}$                         |      | 0.75 | 0.85 | $\Omega$ |
| $I_{D(on)}$  | On State Drain Current            | $V_{DS} > I_{D(on)} \times R_{DS(on)max}$<br>$V_{GS} = 10\text{ V}$ | 8.6  |      |      | A        |

### DYNAMIC

| Symbol         | Parameter                     | Test Conditions   | Min. | Typ. | Max. | Unit |
|----------------|-------------------------------|---|------|------|------|------|
| $g_{fs}^{(*)}$ | Forward Transconductance      | $V_{DS} > I_{D(on)} \times R_{DS(on)max}$ ,<br>$I_D = 4.3\text{ A}$ | 4.5  | 5.7  |      | S    |
| $C_{iss}$      | Input Capacitance             | $V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0$              |      | 1250 | 1625 | pF   |
| $C_{oss}$      | Output Capacitance            |   |      | 175  | 236  | pF   |
| $C_{rss}$      | Reverse Transfer Capacitances |   |      | 20   | 27   | pF   |

**ELECTRICAL CHARACTERISTICS** (continued)

**SWITCHING ON**

| Symbol               | Parameter                       | Test Conditions   | Min. | Typ.     | Max.     | Unit     |
|----------------------|---------------------------------|---|------|----------|----------|----------|
| $t_{d(on)}$<br>$t_r$ | Turn-on Delay Time<br>Rise Time | $V_{DD} = 250V$ $I_D = 4.3 A$<br>$R_G = 4.7 \Omega$ $V_{GS} = 10 V$<br>(see test circuit, Figure 3) |      | 19<br>11 | 30<br>15 | ns<br>ns |
| $Q_g$                | Total Gate Charge               | $V_{DD}=400V$ $I_D=8.6A$ $V_{GS}=10V$   |      | 32       | 45       | nC       |
| $Q_{gs}$             | Gate-Source Charge              |   |      | 10.6     |          | nC       |
| $Q_{gd}$             | Gate-Drain Charge               |   |      | 13.7     |          | nC       |

**SWITCHING OFF**

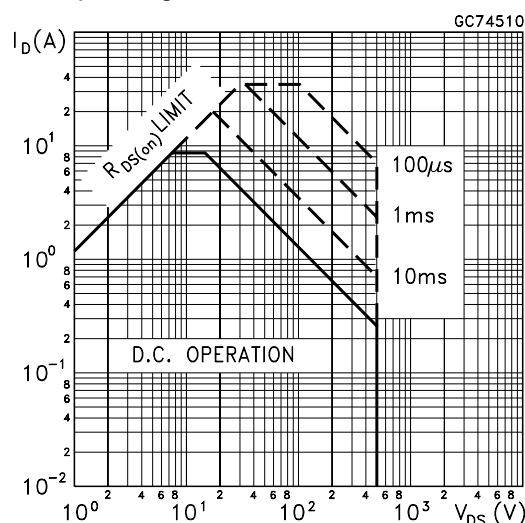
| Symbol                           | Parameter   | Test Conditions  | Min. | Typ.             | Max.           | Unit           |
|----------------------------------|---|--|------|------------------|----------------|----------------|
| $t_r(V_{off})$<br>$t_f$<br>$t_c$ | Off-voltage Rise Time<br>Fall Time<br>Cross-over Time | $V_{DD} = 400 V$ $I_D = 8.6 A$<br>$R_G = 4.7 \Omega$ $V_{GS} = 10 V$<br>(see test circuit, Figure 5) |      | 11.5<br>11<br>20 | 17<br>16<br>28 | ns<br>ns<br>ns |

**SOURCE DRAIN DIODE**

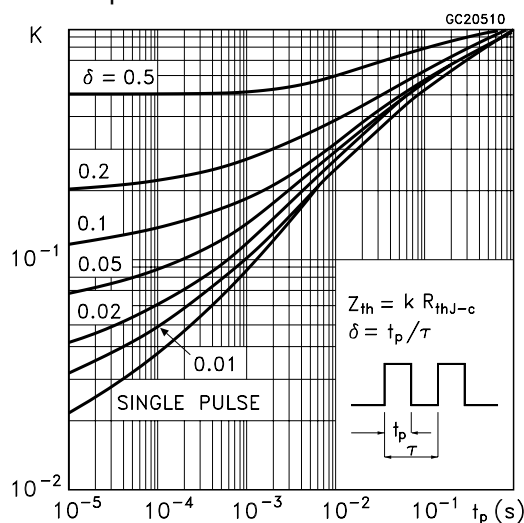
| Symbol                            | Parameter  | Test Conditions  | Min. | Typ.               | Max. | Unit               |
|-----------------------------------|--|--|------|--------------------|------|--------------------|
| $I_{SD}$                          | Source-drain Current   |  |      |                    | 8.6  | A                  |
| $I_{SDM} (\bullet)$               | Source-drain Current (pulsed)  |  |      |                    | 34.4 | A                  |
| $V_{SD} (*)$                      | Forward On Voltage   | $I_{SD} = 8.6 A$ $V_{GS} = 0$  |      |                    | 1.6  | V                  |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse Recovery Time<br>Reverse Recovery Charge<br>Reverse Recovery Current | $I_{SD} = 8.6 A$ $di/dt = 100 A/\mu s$<br>$V_{DD} = 100V$ $T_j = 150 \text{ }^\circ C$<br>(see test circuit, Figure 3) |      | 420<br>3.5<br>16.5 |      | ns<br>$\mu C$<br>A |

(\*) Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.  
 (•) Pulse width limited by safe operating area.

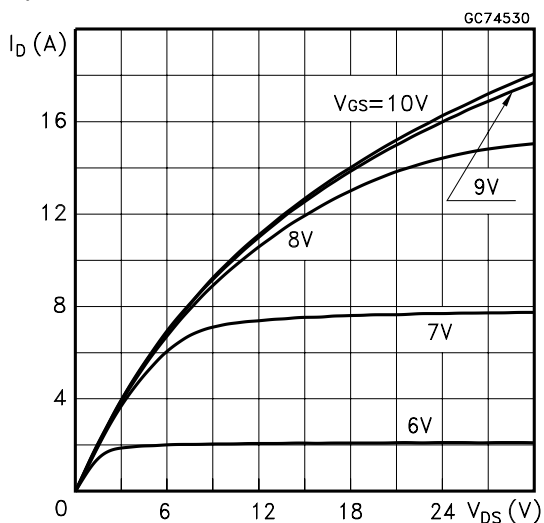
**Safe Operating Area**



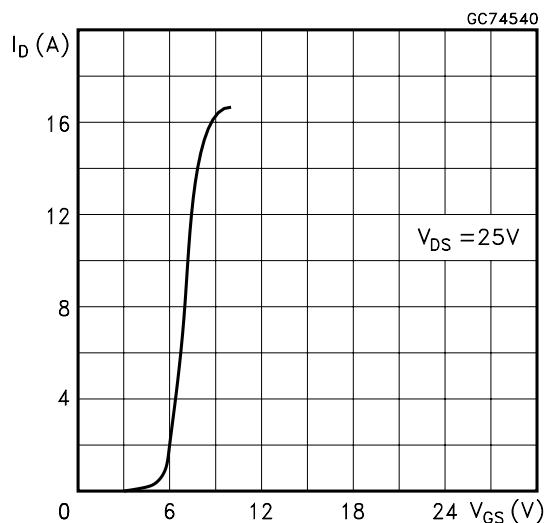
**Thermal Impedance**



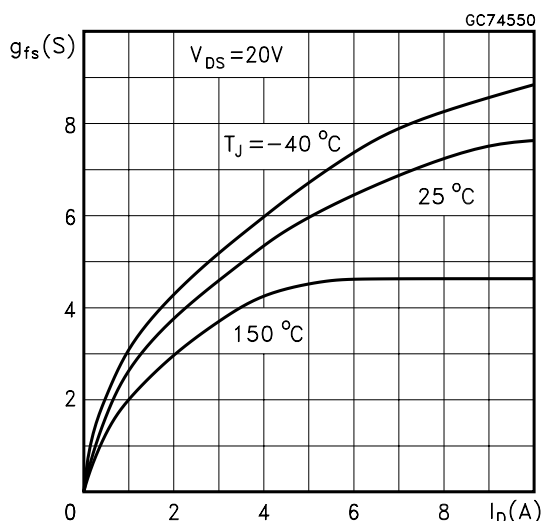
**Output Characteristics**



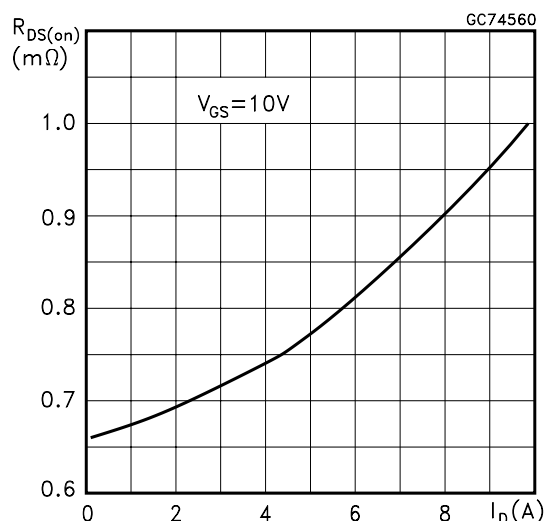
**Transfer Characteristics**



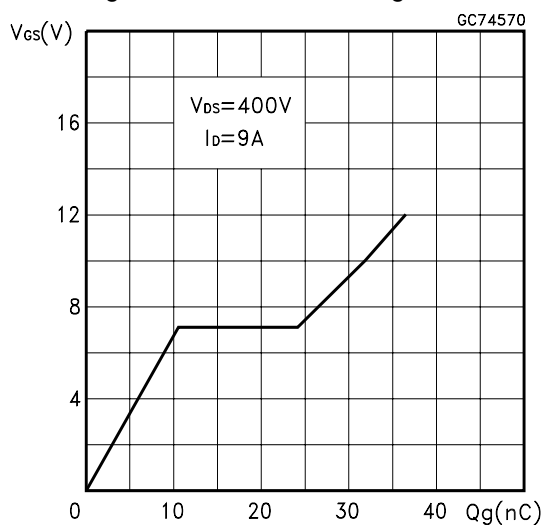
**Transconductance**



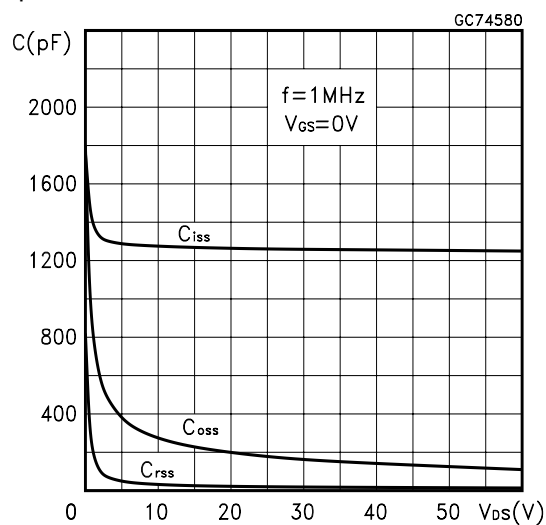
**Static Drain-source On Resistance**



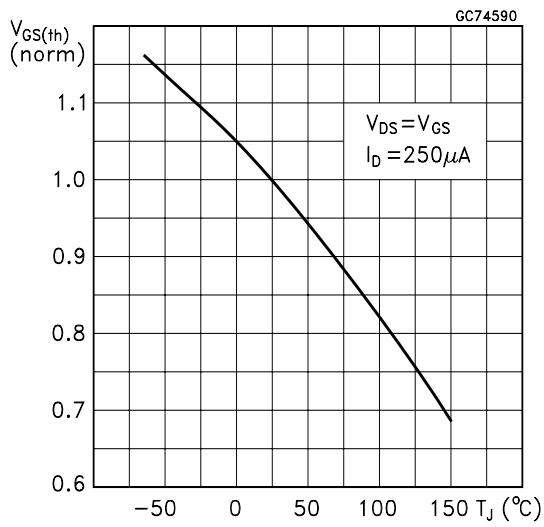
**Gate Charge vs Gate-source Voltage**



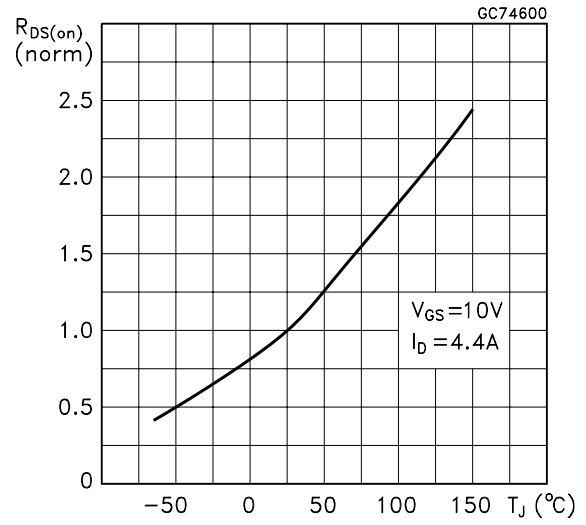
**Capacitance Variations**



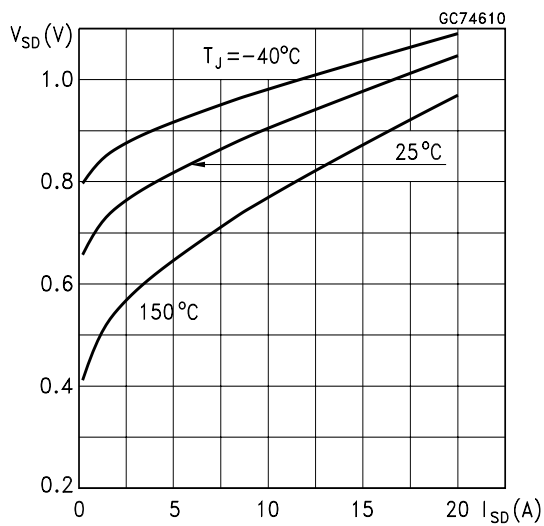
Normalized Gate Threshold Voltage vs Temperature



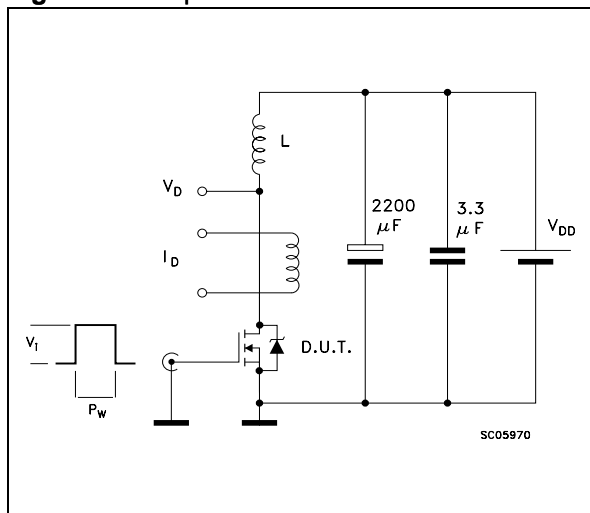
Normalized On Resistance vs Temperature



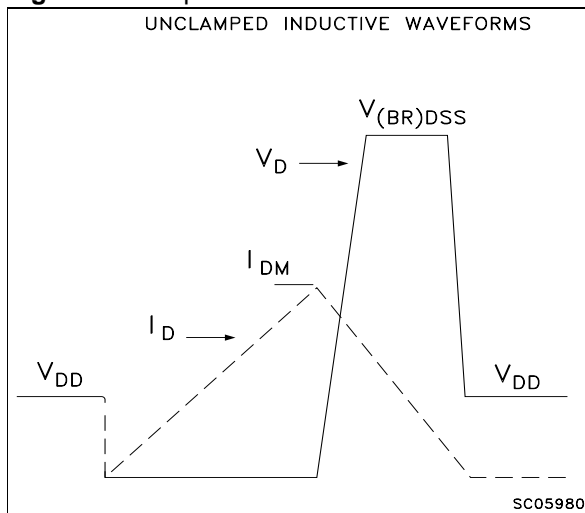
Source-drain Diode Forward Characteristics



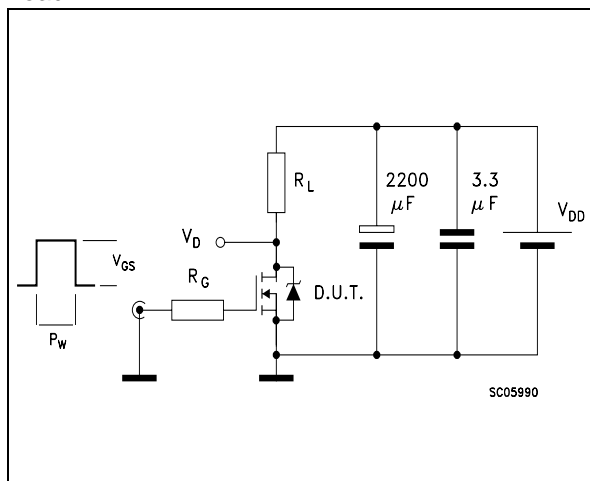
**Fig. 1: Unclamped Inductive Load Test Circuit**



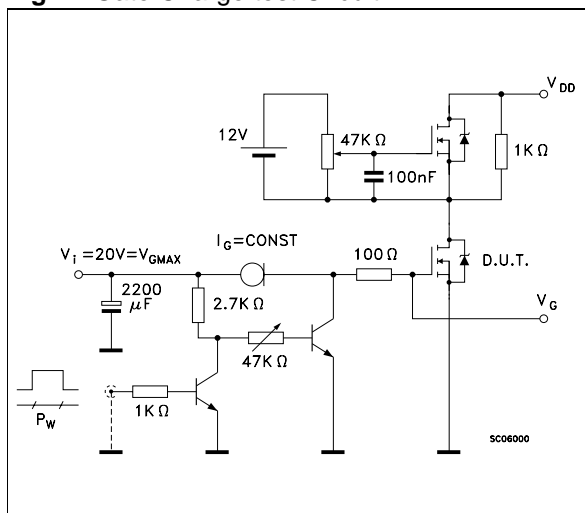
**Fig. 2: Unclamped Inductive Waveform**



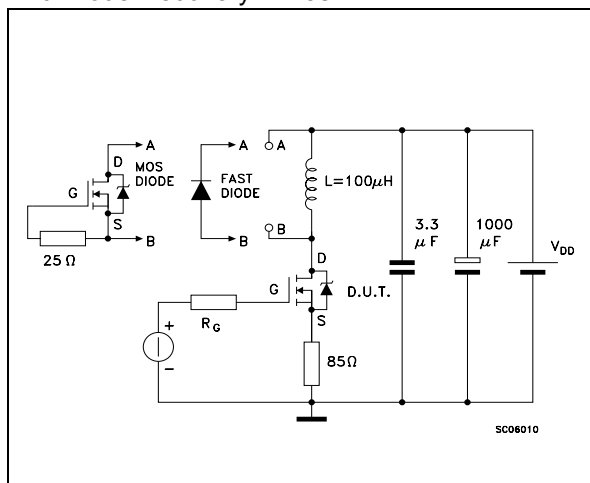
**Fig. 3: Switching Times Test Circuits For Resistive Load**



**Fig. 4: Gate Charge test Circuit**

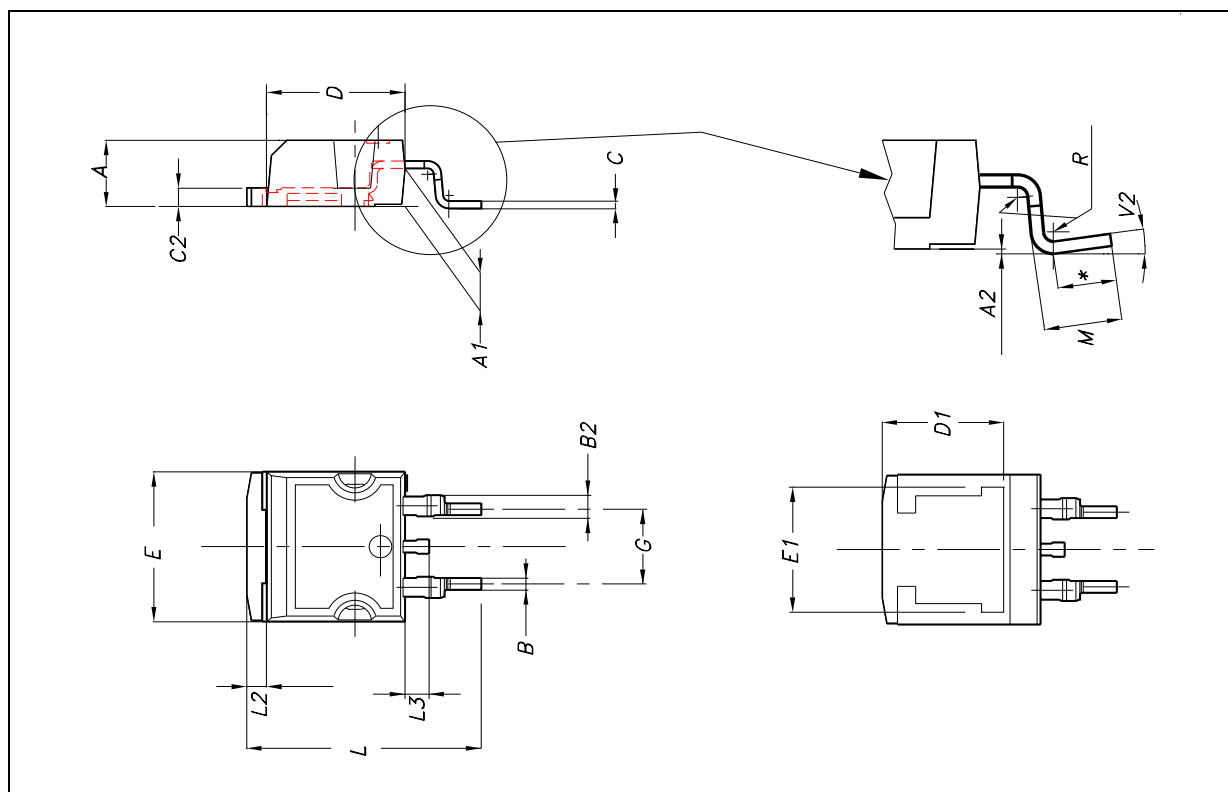


**Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**



D<sup>2</sup>PAK MECHANICAL DATA

| DIM. | mm.  |     |       | inch  |       |       |
|------|------|-----|-------|-------|-------|-------|
|      | MIN. | TYP | MAX.  | MIN.  | TYP.  | MAX.  |
| A    | 4.4  |     | 4.6   | 0.173 |       | 0.181 |
| A1   | 2.49 |     | 2.69  | 0.098 |       | 0.106 |
| A2   | 0.03 |     | 0.23  | 0.001 |       | 0.009 |
| B    | 0.7  |     | 0.93  | 0.027 |       | 0.036 |
| B2   | 1.14 |     | 1.7   | 0.044 |       | 0.067 |
| C    | 0.45 |     | 0.6   | 0.017 |       | 0.023 |
| C2   | 1.23 |     | 1.36  | 0.048 |       | 0.053 |
| D    | 8.95 |     | 9.35  | 0.352 |       | 0.368 |
| D1   |      | 8   |       |       | 0.315 |       |
| E    | 10   |     | 10.4  | 0.393 |       |       |
| E1   |      | 8.5 |       |       | 0.334 |       |
| G    | 4.88 |     | 5.28  | 0.192 |       | 0.208 |
| L    | 15   |     | 15.85 | 0.590 |       | 0.625 |
| L2   | 1.27 |     | 1.4   | 0.050 |       | 0.055 |
| L3   | 1.4  |     | 1.75  | 0.055 |       | 0.068 |
| M    | 2.4  |     | 3.2   | 0.094 |       | 0.126 |
| R    |      | 0.4 |       |       | 0.015 |       |
| V2   | 0°   |     | 8°    |       |       |       |



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