Large Current External FET Controller Type Switching Regulators

Step-up/down, High-efficiency Switching Regulators (Controller type)

BD8303MUV

No.09028EAT02

● General Description

ROHM's highly-efficient step-up/down switching regulator BD8303MUV generates step-up/down output including 3.3 V / 5 V from 1 cell of lithium battery, 4 batteries, or 2 cells of Li batteries with just one inductor.
This IC adopts an original step-up/down drive system and creates a higher efficient power supply than conventional Sepic-system or H-bridge system switching regulators.

● Features

1)Highly-efficient step-up/down DC/DC converter to be constructed just with one inductor.
2) Supports a wide range of power supply voltage range (input voltage: 2.7 V - 14.0 V)
3) Supports high-current application with external Nch FET.
4) Incorporates soft-start function.
5) Incorporates timer latch system short protecting function.
6) High heat radiation surface mounted package QFN16 pin, 3 mm × 3 mm

● Application

General portable equipment like DVC, single-lens reflex cameras, portable DVDs, or mobile PCs

● Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Maximum applied power voltage	VCC	15	V
	VREG	7	V
	Between BOOT 1, 2 and SW 1, 2	7	V
	Between BOOT 1, 2 and GND	20	V
	SW1, 2	15	V
Power dissipation	Pd	620	mW
Operating temperature range	Topr	−25 to +85	°C
Storage temperature range	Tstg	−55 to +150	°C
Junction temperature	Tjmax	+150	°C

When installed on a 70.0 mm × 70.0 mm × 1.6 mm glass epoxy board. The rating is reduced by 4.96 mW/°C at Ta = 25°C or more.

● Operating Conditions (Ta = 25°C)

Parameter	Symbol	Standard value			Unit
		MIN	TYP	MAX	
Power supply voltage	VCC	2.7	−	14	V
Output voltage	VOUT	1.8	−	12	V
Oscillation frequency	fosc	0.2	0.6	1.0	MHz

* These specifications are subject to change without advance notice for modifications and other reasons.

● Electrical Characteristics
(Unless otherwise specified, Ta = 25 °C, VCC = 7.4 V)

Parameter		Symbol	Target Value			Unit	Conditions
			Minimum	Typical	Maximum		
[Low voltage input malfunction preventing circuit]							
Detection threshold voltage		V_{UV}	-	2.4	2.6	V	VREG monitor
Hysteresis range		ΔV_{UVhy}	50	100	200	mV	
[Oscillator]							
Oscillation frequency		fosc	480	600	720	kHz	R_T=51kΩ
[Regulator]							
Output voltage		VREG	4.7	5.1	5.5	V	
[Error AMP]							
INV threshold voltage		VINV	0.9875	1.00	1.0125	V	
Input bias current		IINV	-50	0	50	nA	Vcc=12.0V , I_{INV}=6.0V
Soft-start time		Tss	2.4	4.0	5.6	msec	R_T=51kΩ
Output source current		I_{EO}	10	20	30	μA	V_{INV}=0.8V , V_{FB} =1.5V
Output sink current		I_{EI}	0.6	1.3	3	mA	V_{INV}=1.2V , V_{FB} =1.5V
[PWM comparator]							
SW1 Max Duty		Dmax1	85	90	95	%	HG1 ON
SW2 Max Duty		Dmax2	85	90	95	%	LG2 ON
SW2 Min Duty		Dmin2	5	10	15	%	LG2 OFF
[Output]							
HG1, 2 High side ON resistance		R_{ON}Hp	-	4	8	Ω	
HG1, 2 Low side ON resistance		R_{ON}Hn	-	4	8	Ω	
LG1, 2 High side ON resistance		R_{ON}Lp	-	4	8	Ω	
LG1, 2 Low side ON resistance		R_{ON}Ln	-	4	8	Ω	
HG1-LG1 dead time		Tdead1	50	100	200	nsec	
HG2-LG2 dead time		Tdead2	50	100	200	nsec	
[STB]							
STB pin control voltage	Operation	V_{STB}H	2.5	-	VCC	V	
	No-operation	V_{STB}L	-0.3	-	0.3	V	
STB pin pull-down resistance		R_{STB}	250	400	700	kΩ	
[Circuit current]							
Standby current	VCC pin	I_{STB}	-	-	1	μA	
Circuit current at operation VCC		Icc1	-	650	1000	μA	V_{INV}=1.2V
Circuit current at operation BOOT1,2		Icc2	-	120	240	μA	V_{INV}=1.2V

● Reference Data

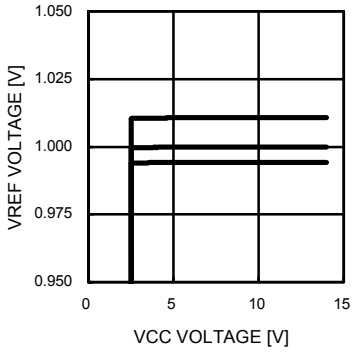


Fig.1 Standard voltage - Power supply property

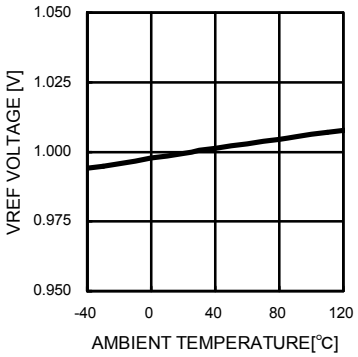


Fig.2 Standard voltage - Temperature property

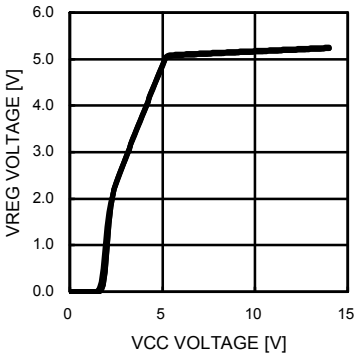


Fig.3 VREG voltage - Power supply property

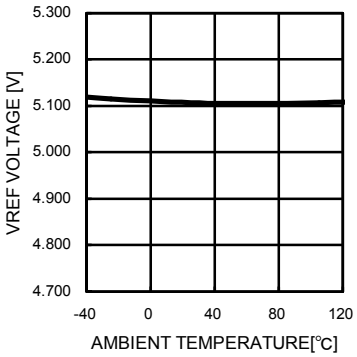


Fig.4 VREG voltage – Temperature property

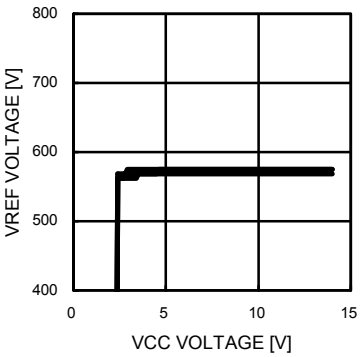


Fig.5 Oscillation frequency – Power supply property

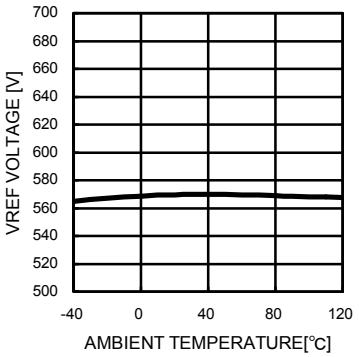


Fig.6 Oscillation frequency - Temperature property

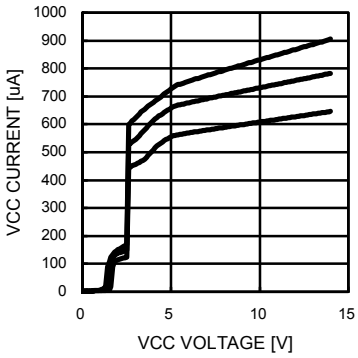


Fig.7 ICC - Power supply property

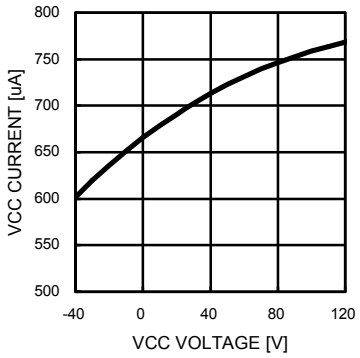


Fig.8 ICC - Temperature property

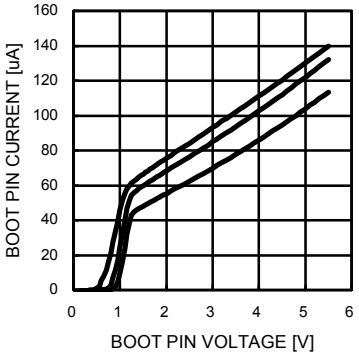


Fig.9 IBOOT - Power supply property

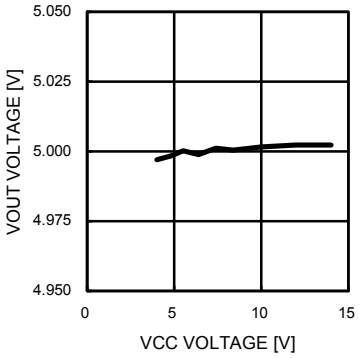


Fig.10 Line regulation

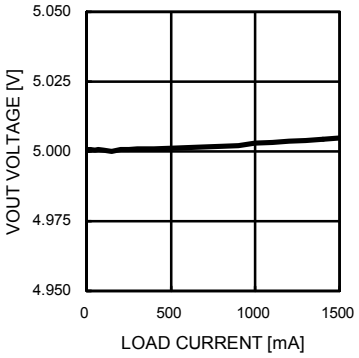


Fig.11 Load regulation

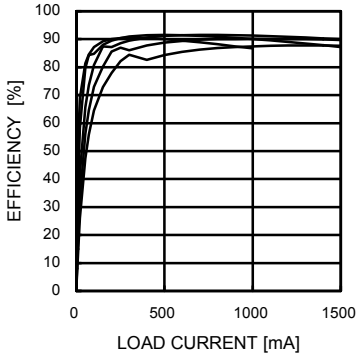


Fig.12 MAX Duty / MIN Duty temperature property

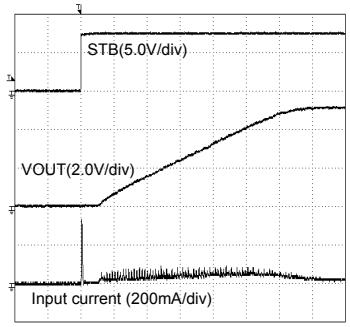


Fig.13 Starting waveform
(Example of Application Circuit [2])
L=10uH, Cout = 47 uH, fosc = 750 kHz, unloaded

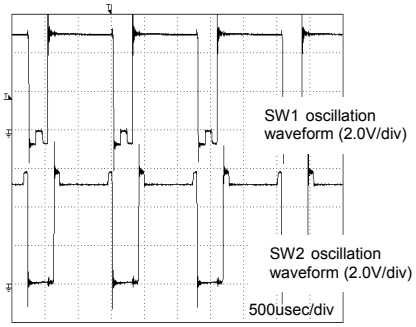


Fig.14 Oscillation waveform
VCC = 5.0 V, Vout = 5.0 V
I LOAD = 1000 mA

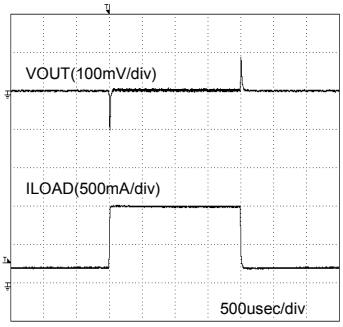


Fig.15 Load variation waveform
(Example of Application Circuit [2])
VCC = 7.4 V, Vout = 5.0 V,
I LOAD = 200 mA←→1000 mA :40 mA/usec

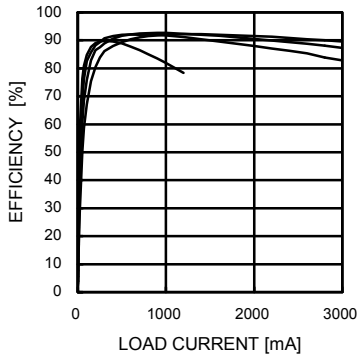


Fig.16
Efficiency data (VOUT = 3.3 V)
Example of Application Circuit [1]

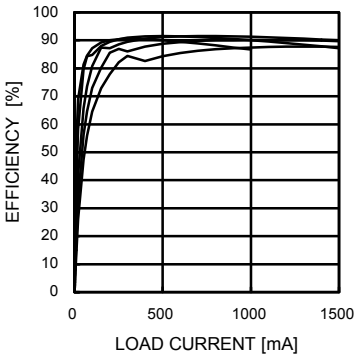


Fig.17
Efficiency data (VOUT = 5.0 V)
Example of Application Circuit [2]

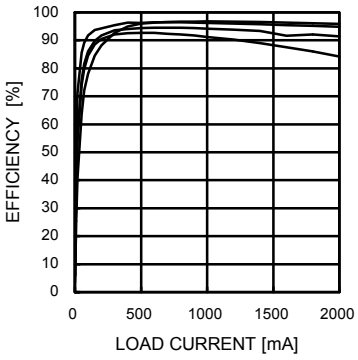


Fig.18
Efficiency data (VOUT = 8.4 V)
Example of Application Circuit [3]

● Package Heat Reduction Curve

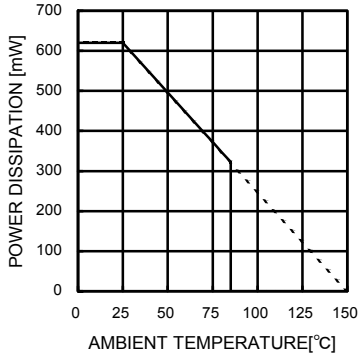


Fig.19 heat reduction curve (IC alone)
When used at Ta = 25°C or more, it is reduced by 4.96 mW/°C.

● Description of Pins

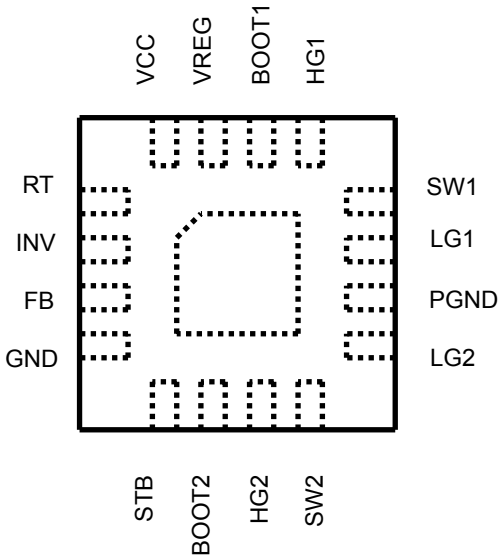


Fig. 20 Pin layout

Pin No.	Pin Name	Function
1	RT	Oscillation frequency set terminal
2	INV	Error AMP input terminal
3	FB	Error AMP output terminal
4	GND	Ground terminal
5	STB	ON/OFF terminal
6	BOOT2	Output side high-side driver input terminal
7	HG2	Output side high-side FET gate drive terminal
8	SW2	Output side coil connecting terminal
9	LG2	Output side low-side FET gate drive terminal
10	PGND	Driver part ground terminal
11	LG1	Input side low-side FET gate drive terminal
12	SW1	Input side coil connecting terminal
13	HG1	Input side high-side FET gate drive terminal
14	BOOT1	Input side high-side driver input terminal
15	VREG	5 V internal regulator output terminal
16	VCC	Power input terminal

● Block Diagram

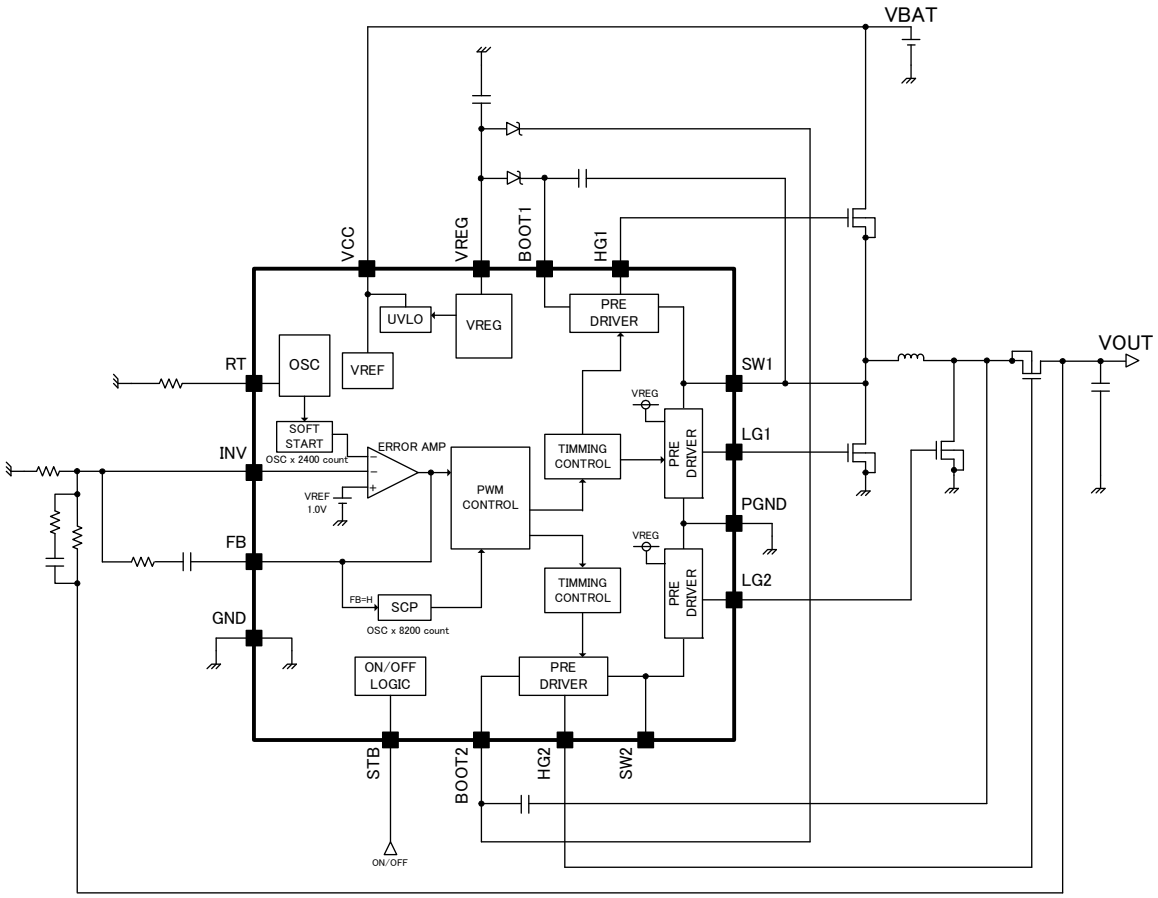


Fig. 21 Block diagram

● Description of Blocks

1. VREF

This block generates ERROR AMP reference voltage.
The reference voltage is 1.0 V.

2. VREG

5.0 V output voltage regulator. Used as power supply for IC internal circuit and BOOT pin supply.
Follows power supply voltage when it is 5.0 V or below and also drops output voltage.
For external oscillation preventive capacitor, 1.0 uF is recommended.

3. UVLO

Circuit for preventing low voltage malfunction

Prevents malfunction of the internal circuit at activation of the power supply voltage or at low power supply voltage.
Monitors VREG pin voltage to turn off DC/DC converter output by changing output voltage of HG1, 2 and LG1, 2 pin to L-logic when VREG voltage is 2.4 V or below, and reset the timer latch of the internal SCP circuit and soft-start circuit.

4. SCP

Timer latch system short-circuit protection circuit

When the INV pin is the set 1.0 V or lower voltage, the internal SCP circuit starts counting.
The internal counter is in synch with OSC; the latch circuit activates after the counter counts about 8200 oscillations to turn off DC/DC converter output (about 13.6 msec when RT = 51 kΩ).
To reset the latch circuit, turn off the STB pin once. Then, turn it on again or turn on the power supply voltage again.

5. OSC

Oscillation circuit to change frequency by external resistance of the RT pin (1 pin).
When RT = 51 kΩ, operation frequency is set at 600 kHz.

6. ERROR AMP

Error amplifier for detecting output signals and output PWM control signals

The internal reference voltage is set at 1.0 V.

7. PWM COMP

Voltage-pulse width converter for controlling output voltage corresponding to input voltage

Comparing the internal SLOPE waveform with the ERROR AMP output voltage, PWM COMP controls the pulse width and outputs to the driver.

Also controls Max Duty and Min Duty.

Max Duty and Min Duty are set at the primary side and the secondary side of the inductor respectively, which are as follows:

Primary side (SW1)	HG1 Max Duty	:	About 90 %,
	HG1 Min Duty	:	0 %
Secondary side (SW 2)	LG2 Max Duty	:	About 90 %,
	LG2 Min Duty	:	About 10 %,

8. SOFT START

Circuit for preventing in-rush current at startup by bringing the output voltage of the DC/DC converter into a soft-start

Soft-start time is in synch with the internal OSC, and the output voltage of the DC/DC converter reaches the set voltage after about 2400 oscillations (About 4 msec when RT = 51 kΩ).

9. Nch DRIVER

CMOS inverter circuit for driving external Nch FET.

Dead time is provided for preventing feedthrough during switching of HG1 = L → LG1 = H, HG2 = L → LG2 = H and LG1 = L → HG1 = H, LG2 = L → HG2 = H.
The dead time is set at about 100 nsec in the internal circuit.

10. ON/OFF LOGIC

Voltage applied on STB pin (5 pin) to control ON/OFF of IC. Turned ON when a voltage of 2.5 V or higher is applied and turned OFF when the terminal is open or 0 V is applied.
Incorporates approximately 400 kΩ pull-down resistance.

● Example of Application Circuit

* Example of application circuit: VCC = 2.7 – 5.5V, Vout = 3.3V, Iout = 100 mA – 2000 mA

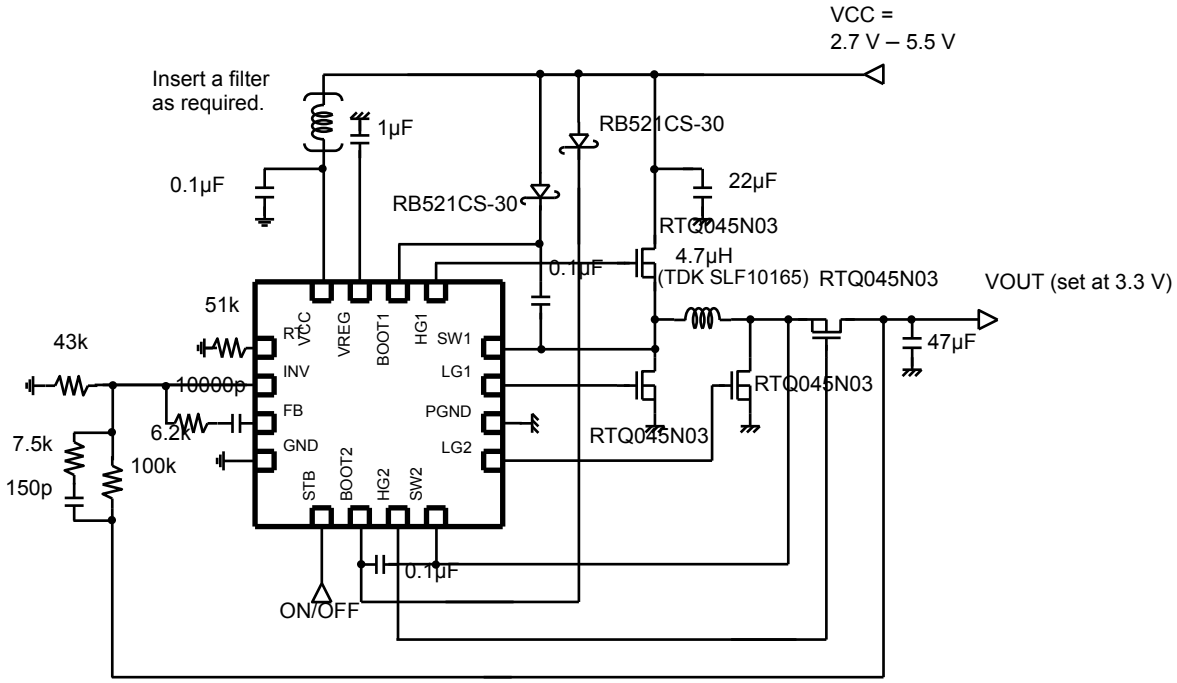


Fig. 22 Example of application circuit (1)

* Example of application circuit: VCC=2.7 – 14 V, Vout＝5.0 V, Iout＝100 mA – 1500 mA

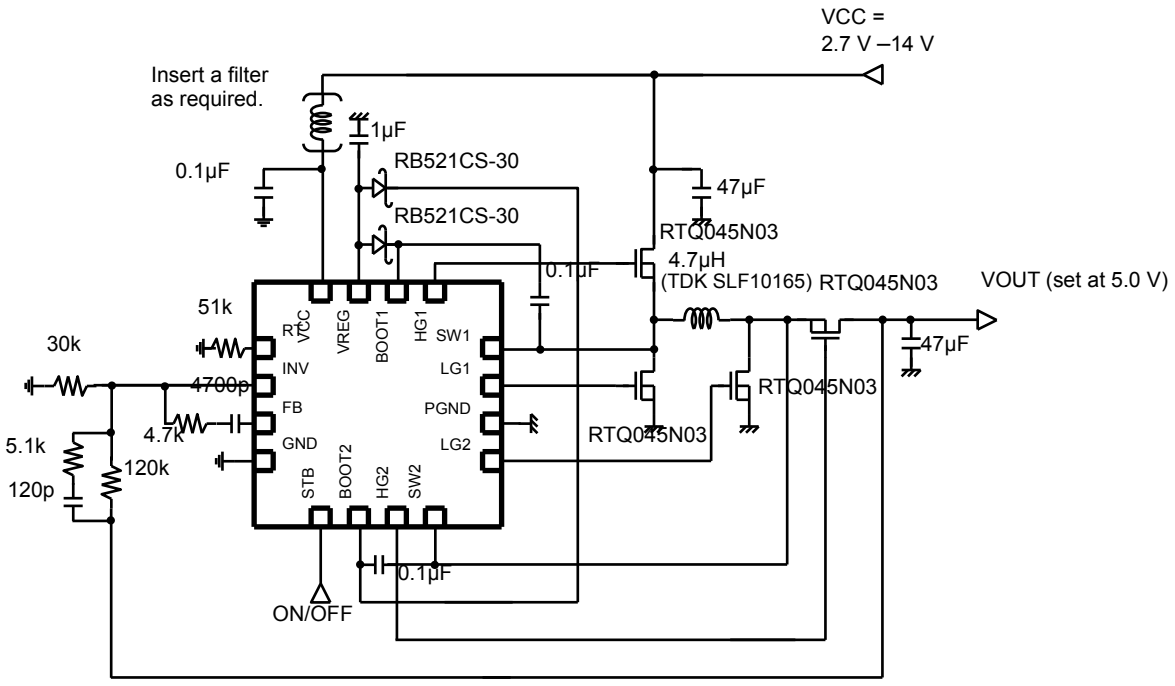


Fig. 23 Example of application circuit (2)

* Example of application circuit: VCC=4.0 – 14 V, Vout＝8.4 V, Iout＝100 mA – 1500 mA

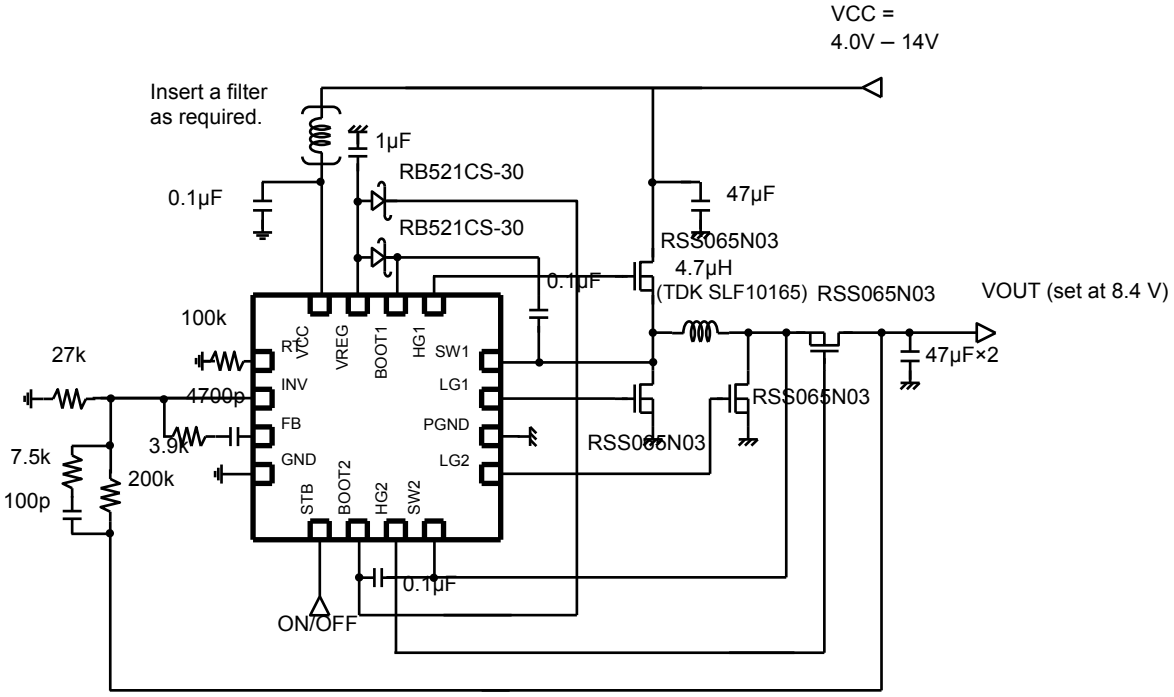


Fig. 24 Example of application circuit (3)

* Example of application circuit:VCC=2.7 – 14 V, Vout＝12 V, Iout＝100 mA – 1500 mA

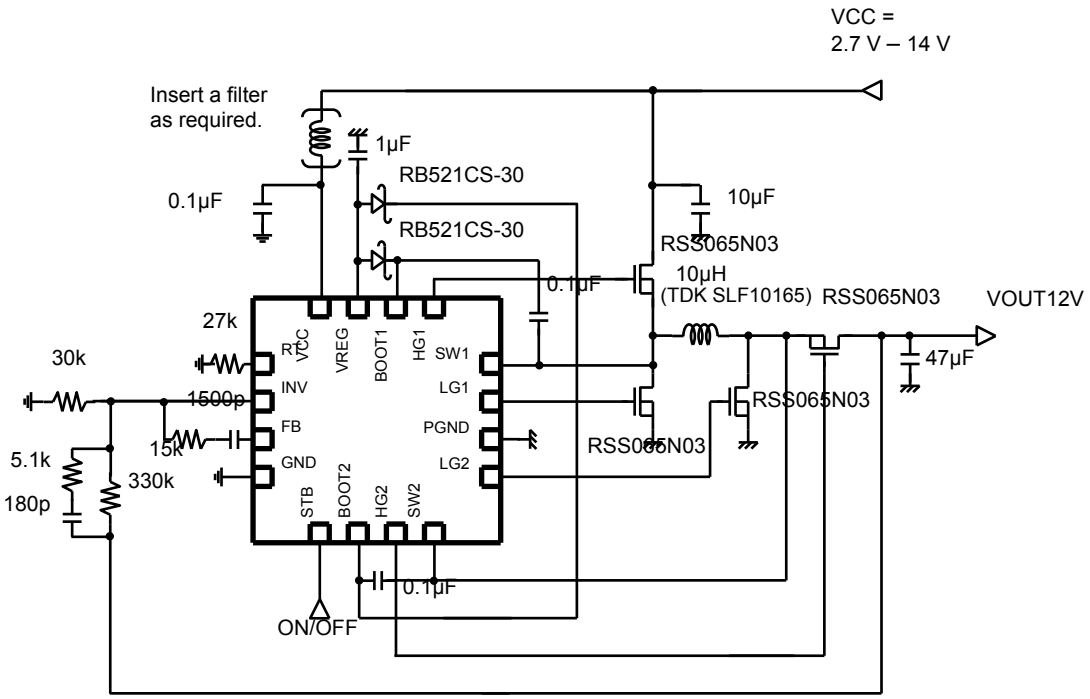


Fig. 25 Example of application circuit (4)

● Selection of parts for applications

(1) Output inductor

A shielded inductor that satisfies the current rating (current value, Ipeak as shown in the drawing below) and has a low DCR (direct current resistance component) is recommended.
Inductor values affect output ripple current greatly.
Ripple current can be reduced as the coil L value becomes larger and the switching frequency becomes higher as the equations shown below.

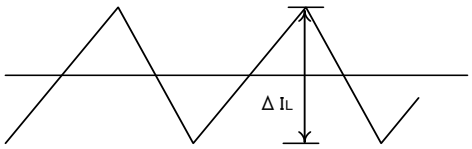


Fig. 26Ripple current

Ipeak =Iout ×(Vout/VIN) /η＋ ΔIL/2 [A] (1)

$$\Delta IL = \frac{(Vin-Vout)}{L} \times \frac{Vout}{Vin} \times \frac{1}{f} \quad [A] \quad \text{(in step-down mode)} \qquad (2)$$

$$\Delta IL = \frac{|(Vin-Vout)|}{L} \times \frac{Vout \times 2 \times 0.8}{(Vin+Vout)} \times \frac{1}{f} \quad [A] \quad \text{((in step-up/down mode)} \qquad (3)$$

$$\Delta IL = \frac{(Vout-Vin)}{L} \times \frac{Vin}{Vout} \times \frac{1}{f} \quad [A] \quad \text{(in step-up mode)} \qquad (4)$$

(η: Efficiency, ΔIL: Output ripple current, f: Switching frequency)

As a guide, output ripple current should be set at about 20 to 50% of the maximum output current.

* Current over the coil rating flowing in the coil brings the coil into magnetic saturation, which may lead to lower efficiency or output oscillation. Select an inductor with an adequate margin so that the peak current does not exceed the rated current of the coil.

(2) Output capacitor

A ceramic capacitor with low ESR is recommended for output in order to reduce output ripple.
There must be an adequate margin between the maximum rating and output voltage of the capacitor, taking the DC bias property into consideration.
Output ripple voltage when ceramic capacitor is used is obtained by the following equation.

$$Vpp = \Delta IL \times \frac{1}{2\pi \times f \times Co} + \Delta IL \times R_{ESR} \quad [V] \quad \cdots \quad (5)$$

$$Vpp = \Delta IL \times \frac{1}{2\pi \times f \times Co} + \Delta IL \times R_{ESR} \quad [V] \quad \cdots (5)$$

Setting must be performed so that output ripple is within the allowable ripple voltage.

(3) External FET

An external FET which satisfies the following items and has small Ciss (input capacitance), Qg (total gate charge quantity) and ON resistance should be selected. There must be an adequate margin between the turn OFF time of MOS and the dead time to prevent through-current.

Drain-source voltage rating: (Output voltage + BodyDiode Vf of MOS or higher)
Gate-source voltage rating: 7.0 V or higher
Drain-source current rating: IPEAK of Output inductor paragraph or higher

(5) BOOT-SW capacitor

The capacitor between BOOT and SW should be designed so that the gate drive voltage will not be below Vgs necessary for the FET to use, taking circuit current input to the BOOT pin into consideration. There must be an adequate margin between the maximum rating and gate drive voltage.

Gate drive voltage

= (VREG voltage) − (Vf of Di) − (Voltage drop by BOOT pin consumption) [V] (6)

Voltage drop by BOOT pin consumption

= (Iboot × (1 / fosc) + Qg of external FET) / Cboot [V] (7)

(6) REG-BOOT diode

A Schottky diode which satisfies the following items and has less forward pressure drop (Vf) should be selected.

Average rectified current: There must be an adequate margin against the current consumed by MOSFET switching.

DC inverse voltage: Input voltage or higher

(3) Setting of oscillation frequency

Oscillation frequency can be set using a resistance value connected to the RT pin (1 pin).

Oscillation frequency is set at 600 kHz when RT = 51 kΩ, and frequency is inversely proportional to RT value.

See Fig. 27 for the relationship between RT and frequency.

Soft-start time changes along with oscillation frequency.

See Fig. 28 for the relationship between RT and soft-start time.

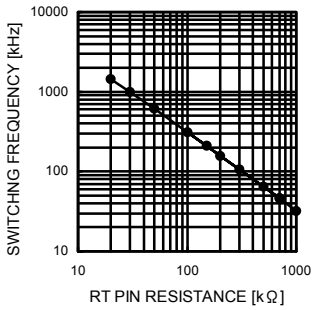


Fig. 27 Oscillation frequency – RT pin resistance

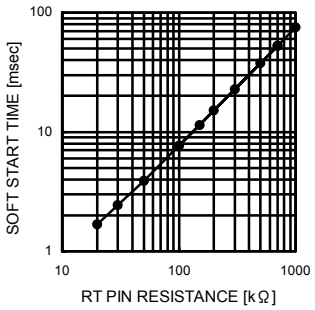
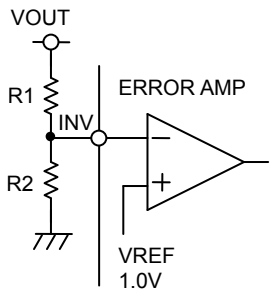


Fig. 28 Soft-start time – RT pin resistance

* Note that the above example of frequency setting is just a design target value, and may differ from the actual equipment.

(4) Output voltage setting

The internal reference voltage of the ERROR AMP is 1.0 V. Output voltage should be obtained by referring to Equation (8) of Fig. 29.



$$Vo = \frac{(R1+R2)}{R2} \times 1.0\ [V] \ldots (8)$$

Fig. 29 Setting of feedback resistance

(9) Determination of external phase compensation

Condition for stable application

The condition for feedback system stability under negative feedback is as follows:

- Phase delay is 135 °or less when gain is 1 (0 dB) (Phase margin is 45° or higher)

Since DC/DC converter application is sampled according to the switching frequency, the GBW of the whole system (frequency at which gain is 0 dB) must be set to be equal to or lower than 1/5 of the switching frequency.

In summary, target property of applications is as follows:

- Phase delay must be 135°or lower when gain is 1 (0 dB) (Phase margin is 45° or higher).
- The GBW at that time (frequency when gain is 0 dB) must be equal to or lower than 1/5 of the switching frequency.

For this reason, switching frequency must be increased to improve responsiveness.

One of the points to secure stability by phase compensation is to cancel secondary phase delay (-180°) generated by LC resonance by the secondary phase lead (i.e. put two phase leads).
Since GBW is determined by the phase compensation capacitor attached to the error amplifier, when it is necessary to reduce GBW, the capacitor should be made larger.

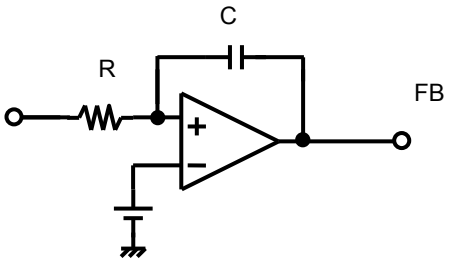
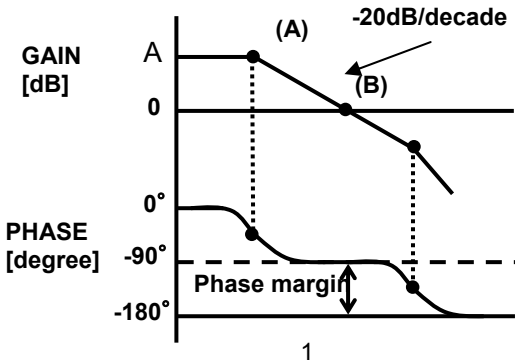


Fig.30 General integrator

Error AMP is a low-pass filter because phase compensation such as (1) and (2) is performed. For DC/DC converter application, R is a parallel feedback resistance.



$$\text{Point (A)}\quad fp=\frac{1}{2\pi RCA}\ [\text{Hz}] \qquad (9)$$

$$\text{Point (B)}\quad f_{GBW}=\frac{1}{2\pi RC}\ [\text{Hz}] \qquad (10)$$

Fig.31 Frequency property of integrator

Phase compensation when output capacitor with low ESR such as ceramic capacitor is used is as follows:

When output capacitor with low ESR (several tens of mΩ) is used for output, secondary phase lead (two phase leads) must be put to cancel secondary phase lead caused by LC.

One of the examples of phase compensation methods is as follows:

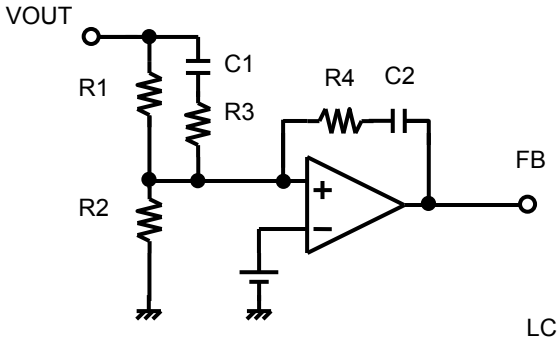


Fig.32 Example of setting of phase compensation

$$\text{Phase lead } fz1=\frac{1}{2\pi R1C1}\ [\text{Hz}] \qquad (11)$$

$$\text{Phase lead } fz2=\frac{1}{2\pi R4C2}\ [\text{Hz}] \qquad (12)$$

$$\text{Phase delay } fp1=\frac{1}{2\pi R3C1}\ [\text{Hz}] \qquad (13)$$

$$\text{LC resonance frequency}=\frac{1}{2\pi\sqrt{(LC)}}\ [\text{Hz}] \qquad (14)$$

For setting of phase-lead frequency, both of them should be put near LC resonance frequency.
When GBW frequency becomes too hjgh due to the secondary phase lead, it may get stabilized by putting the primary phase delay in a frequency slightly higher than the LC resonance frequency to compensate it.

● Example of Board Layout

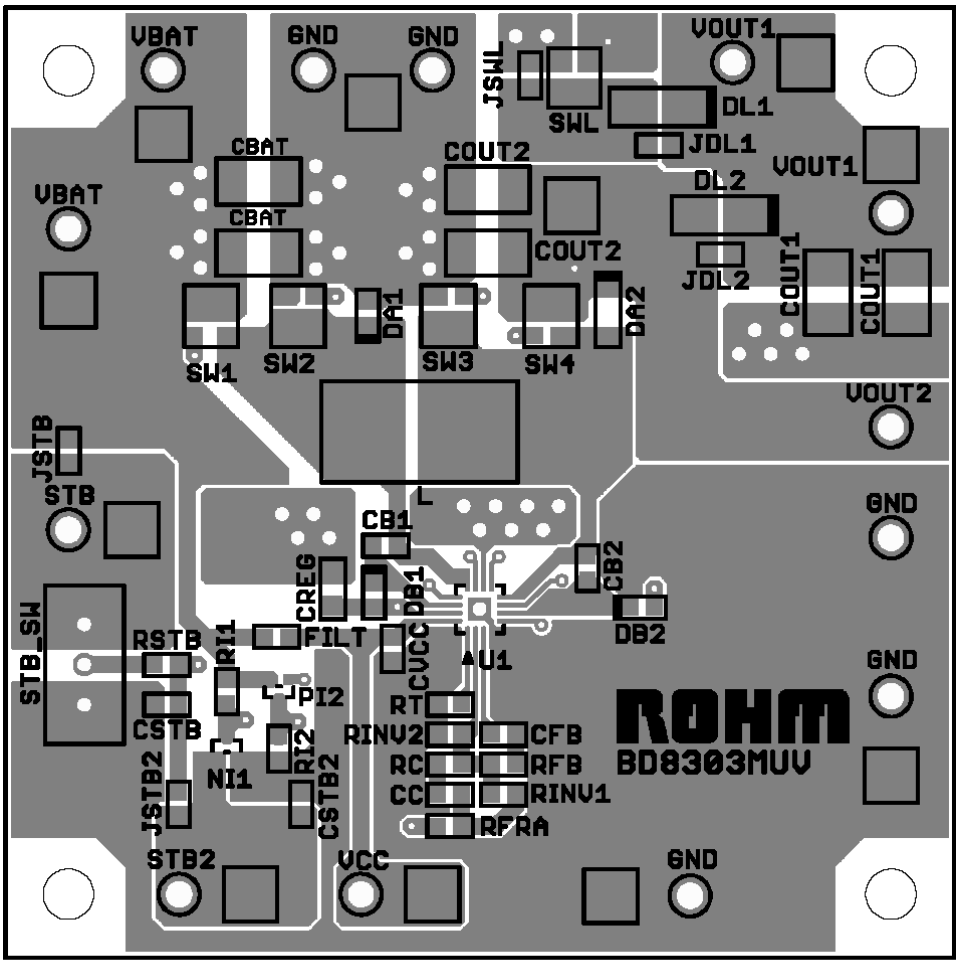


Fig.33 Example of Board Layout

● I/O Equivalence Circuit

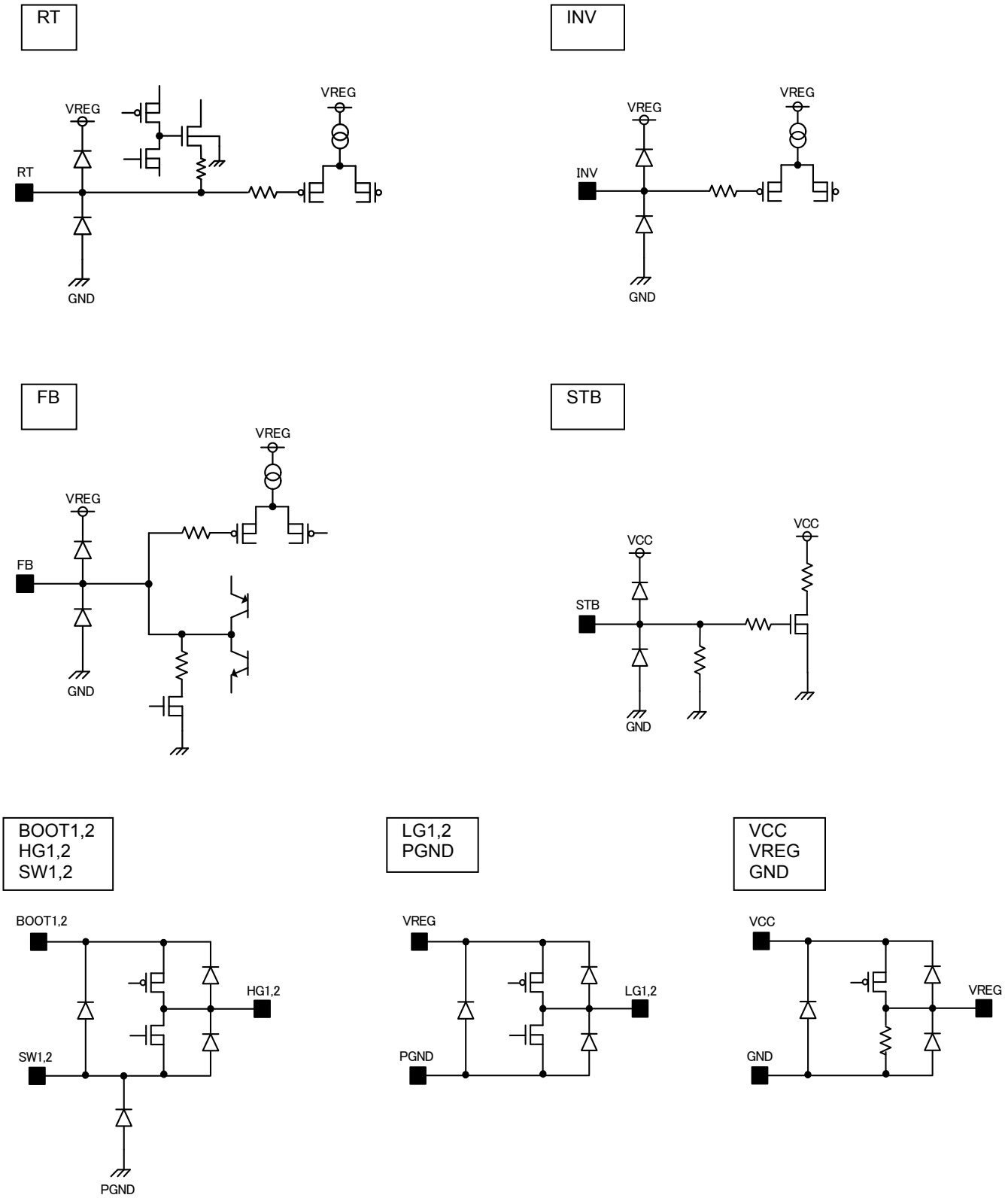


Fig.34 I/O equivalence circuit

● Precautions for Use

1) Absolute Maximum Rating
We dedicate much attention to the quality control of these products, however the possibility of deterioration or destruction exists if the impressed voltage, operating temperature range, etc., exceed the absolute maximum ratings. In addition, it is impossible to predict all destructive situations such as short-circuit modes, open circuit modes, etc. If a special mode exceeding the absolute maximum rating is expected, please review matters and provide physical safety means such as fuses, etc.

2) GND Potential
Keep the potential of the GND pin below the minimum potential at all times.

3) Thermal Design
Work out the thermal design with sufficient margin taking power dissipation (Pd) in the actual operation condition into account.

4) Short Circuit between Pins and Incorrect Mounting
Attention to IC direction or displacement is required when installing the IC on a PCB. If the IC is installed in the wrong way, it may break. Also, the threat of destruction from short-circuits exists if foreign matter invades between outputs or the output and GND of the power supply.

5) Operation under Strong Electromagnetic Field
Be careful of possible malfunctions under strong electromagnetic fields.

6) Common Impedance
When providing a power supply and GND wirings, show sufficient consideration for lowering common impedance and reducing ripple (i.e., using thick short wiring, cutting ripple down by LC, etc.) as much as you can.

7) Thermal Protection Circuit (TSD Circuit)
This IC contains a thermal protection circuit (TSD circuit). The TSD circuit serves to shut off the IC from thermal runaway and does not aim to protect or assure operation of the IC itself. Therefore, do not use the TSD circuit for continuous use or operation after the circuit has tripped.

8) Rush Current at the Time of Power Activation
Be careful of the power supply coupling capacity and the width of the power supply and GND pattern wiring and routing since rush current flows instantaneously at the time of power activation in the case of CMOS IC or ICs with multiple power supplies.

9) IC Terminal Input
This is a monolithic IC and has P+ isolation and a P substrate for element isolation between each element. P-N junctions are formed and various parasitic elements are configured using these P layers and N layers of the individual elements.
For example, if a resistor and transistor are connected to a terminal as shown on Fig.-8:
○ The P-N junction operates as a parasitic diode when GND > (Terminal A) in the case of a resistor or when GND > (Pin B) in the case of a transistor (NPN)
○ Also, a parasitic NPN transistor operates using the N layer of another element adjacent to the previous diode in the case of a transistor (NPN) when GND > (Pin B).
The parasitic element consequently rises under the potential relationship because of the IC's structure. The parasitic element pulls interference that could cause malfunctions or destruction out of the circuit. Therefore, use caution to avoid the operation of parasitic elements caused by applying voltage to an input terminal lower than the GND (P board), etc.

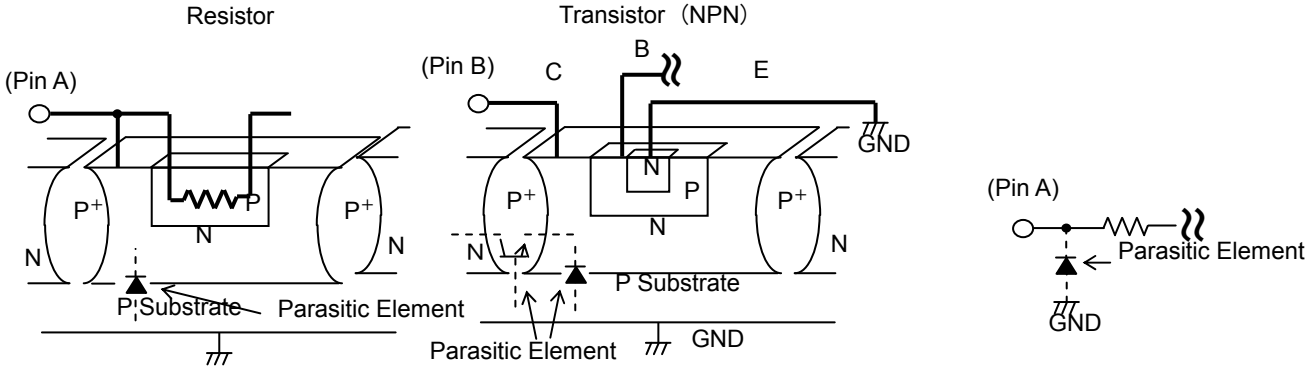


Fig.35 Example of simple structure of Bipolar IC

● **Ordering part number**

B	D	8	3	0	3	M	U	V	-	E	2

Part No. (BD)

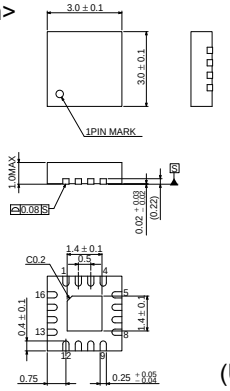
Part No. (8303)

Package
MUV: VQFN016V3030

Packaging and forming specification
E2: Embossed tape and reel

VQFN016V3030

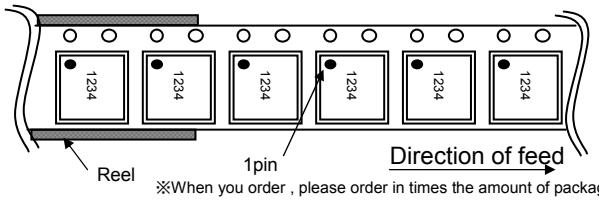
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

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