

PCF2120

Quartz oscillator

Rev. 01 — 5 February 2008

Product data sheet

1. General description

The PCF2120 is a CMOS quartz oscillator optimized for low power consumption. The 32 kHz output signal is gated using an enable signal.

2. Features

- Clock operating voltage: 1.5 V to 5.5 V
- Low backup current: typical 0.85 μ A at $V_{DD} = 3.0$ V and $T_{amb} = 25$ °C
- 32.768 kHz output for peripheral devices
- Two integrated oscillator capacitors
- Push-pull output
- Internal power-on reset

3. Applications

- Portable instruments
- Industrial products
- Battery powered products

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		[1] 1.5	-	5.5	V
I_{DD}	supply current	clock output disabled				
		$V_{DD} = 2.0$ V; $T_{amb} = 25$ °C	-	210	450	nA
		$V_{DD} = 3.0$ V; $T_{amb} = -40$ °C to +85 °C	-	265	650	nA
		clock output enabled at 32 kHz				
		$V_{DD} = 2.0$ V; $T_{amb} = 25$ °C	-	615	900	nA
		$V_{DD} = 3.0$ V; $T_{amb} = -40$ °C to +85 °C	-	875	1100	nA
T_{stg}	storage temperature		-65	-	+150	°C

[1] For reliable oscillator start-up at power-up: $V_{DD} > V_{DD(min)} + 0.3$ V.

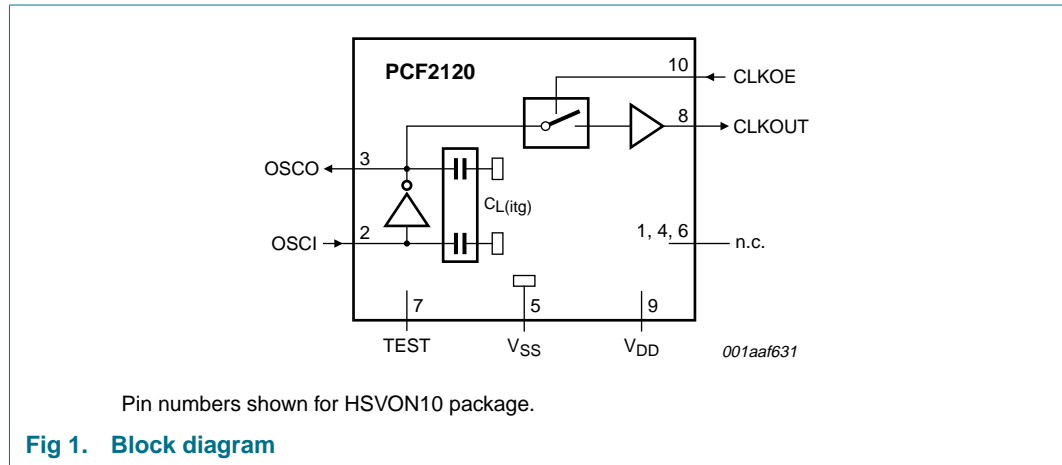
5. Ordering information

Table 2. Ordering information

Type number	Package		Version
	Name	Description	
PCF2120TK	HVSON10	plastic thermal enhanced very thin small outline package; no leads; 10 terminals; body 3 × 3 × 0.85 mm	SOT650-1
PCF2120U ^[1]	-	wire bond die; 7 bonding pads; 0.57 × 1.1 × 0.2 mm	PCF2120U

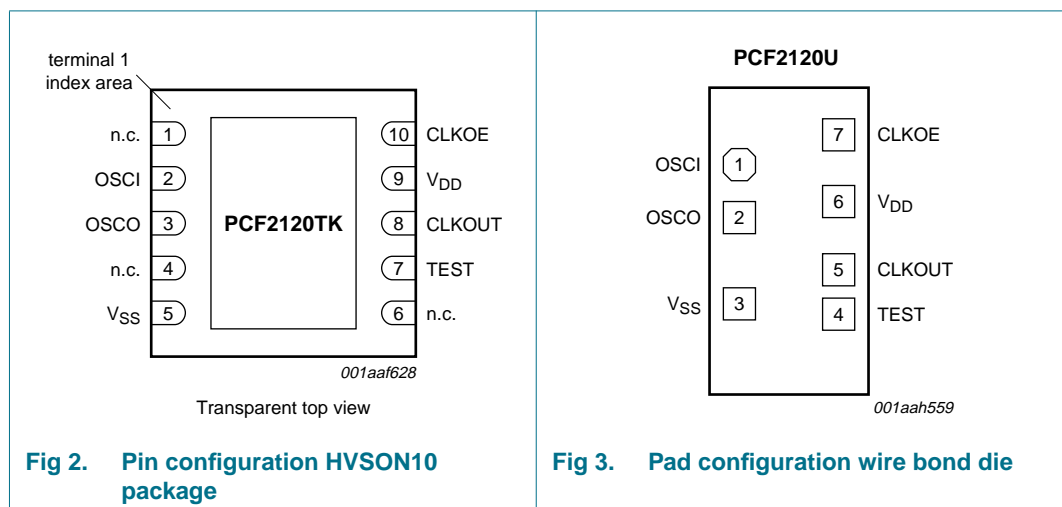
[1] Packing method: sawn wafer on Film Frame Carrier (FFC).

6. Block diagram



7. Pinning information

7.1 Pinning



7.2 Pin description

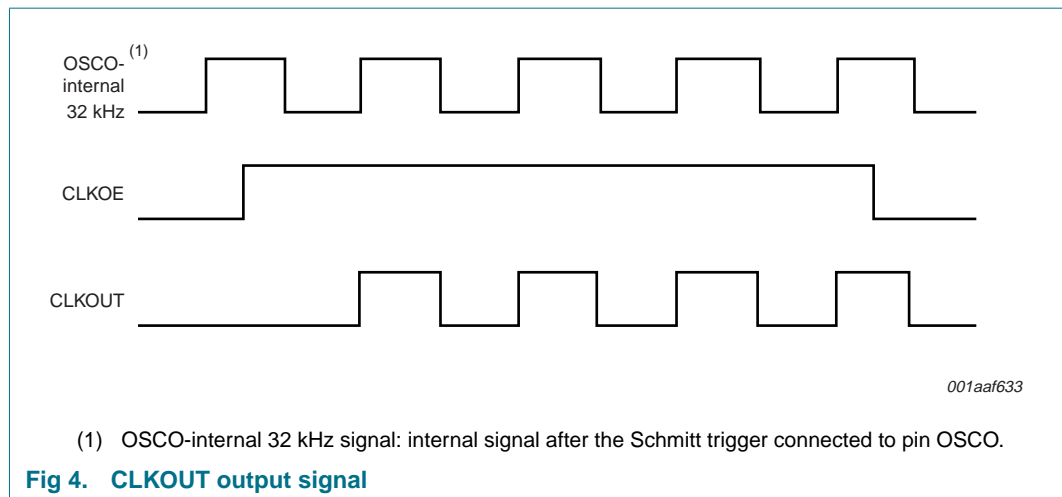
Table 3. Pin description

Symbol	Pin	Pad	Description
	HVSON10	Wire bond die	
n.c.	1	-	not connected
OSCI	2	1	oscillator input
OSCO	3	2	oscillator output
n.c.	4	-	not connected
V _{SS}	5	3	ground
n.c.	6	-	not connected
TEST	7	4	test pin
CLKOUT	8	5	clock output (push-pull)
V _{DD}	9	6	supply voltage
CLKOE	10	7	clock output enable input

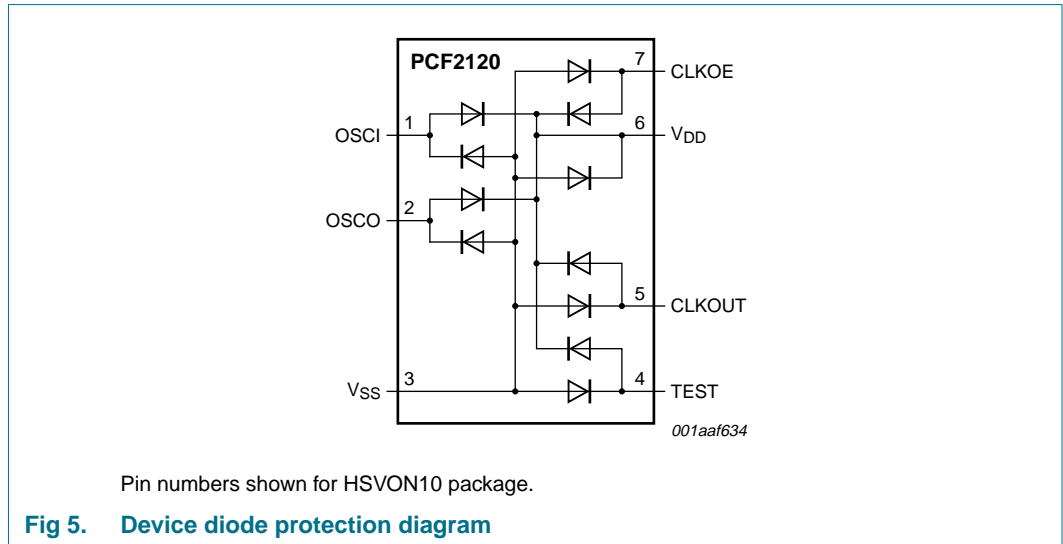
8. Functional description

The 32 kHz quartz oscillator is optimized for directly connecting to a 32 kHz tuning fork quartz crystal. No additional tuning capacitors are required. Laser tuning of the quartz or quartz selection for matching is used to tune the oscillator if required.

A digital 32 kHz signal is available on pin CLKOUT. The signal on pin CLKOE is used to gate and synchronize the 32 kHz CLKOUT signal. Pin CLKOUT is a CMOS push-pull output. If disabled, it goes to LOW level.



9. Internal circuitry



10. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DD}	supply voltage		-0.5	+6.5	V	
I_{DD}	supply current		-50	+50	mA	
V_I	input voltage		-0.5	+6.5	V	
V_O	output voltage		-0.5	+6.5	V	
I_I	input current	at any input	-10	+10	mA	
I_O	output current	at any output	-10	+10	mA	
P_{tot}	total power dissipation		-	300	mW	
T_{stg}	storage temperature		-65	+150	°C	
V_{esd}	electrostatic discharge voltage	HBM	[1]	-	±2000	V
		MM	[2]	-	±200	V
		CDM	[3]	-	±2000	V
I_{lu}	latch-up current		[4]	-	100	mA

[1] Human Body Model (HBM) according to JESD22-A114.

[2] Machine Model (MM) according to JESD22-A115.

[3] Charged-Device Model (CDM) according to JESD22-C101.

[4] Latch-up testing according to JESD78.

11. Static characteristics

Table 5. Static characteristics

$V_{DD} = 1.5\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ °C to }+85\text{ °C}$; $f_{osc} = 32.768\text{ kHz}$; quartz $R_s = 40\text{ k}\Omega$; $C_L = 8\text{ pF}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_{DD}	supply voltage		[1] 1.5	-	5.5	V
I_{DD}	supply current	clock output disabled				
		$T_{amb} = 25\text{ °C}$				
		$V_{DD} = 5.0\text{ V}$	-	300	550	nA
		$V_{DD} = 3.0\text{ V}$	-	235	500	nA
		$V_{DD} = 2.0\text{ V}$	-	210	450	nA
		$T_{amb} = -40\text{ °C to }+85\text{ °C}$				
		$V_{DD} = 5.0\text{ V}$	-	345	750	nA
		$V_{DD} = 3.0\text{ V}$	-	265	650	nA
		$V_{DD} = 2.0\text{ V}$	-	230	600	nA
		clock output enabled at 32 kHz	[2]			
		$T_{amb} = 25\text{ °C}$				
		$V_{DD} = 5.0\text{ V}$	-	1310	1700	nA
		$V_{DD} = 3.0\text{ V}$	-	845	1100	nA
		$V_{DD} = 2.0\text{ V}$	-	615	900	nA
		$T_{amb} = -40\text{ °C to }+85\text{ °C}$				
		$V_{DD} = 5.0\text{ V}$	-	1385	1700	nA
		$V_{DD} = 3.0\text{ V}$	-	875	1100	nA
		$V_{DD} = 2.0\text{ V}$	-	635	900	nA
Inputs						
Pin OSCI						
V_I	input voltage		-0.5	-	$V_{DD} + 0.5$	V
Pin CLKOE						
V_I	input voltage		-0.5	-	$V_{DD} + 0.5$	V
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	-	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS}	-1	0	+1	μA
Outputs						
Pin OSCO						
V_O			-0.5	-	$V_{DD} + 0.5$	V
Pin CLKOUT						
V_O	output voltage		-0.5	-	$V_{DD} + 0.5$	V
I_{OL}	LOW-level output current	$V_{OL} = 0.4\text{ V}$; $V_{DD} = 5\text{ V}$	-1	-	-	mA
I_{OH}	HIGH-level output current	$V_{OH} = 4.6\text{ V}$; $V_{DD} = 5\text{ V}$	-	-	1	mA
I_{LO}	output leakage current	$V_O = V_{DD}$ or V_{SS}	-1	0	+1	μA

[1] For reliable oscillator start-up at power-up: $V_{DD} > V_{DD(\min)} + 0.3\text{ V}$.

[2] Pin CLKOUT is loaded with a 7.5 pF capacitor.

When pin CLKOUT is enabled the current consumption is a function of the load on that pin, the output frequency and the supply voltage. The additional current consumption for a given load can be calculated from the formula $I_{DD} = C_{CLKOUT} \times V_{DD} \times f_{CLKOUT}$

Where:

I_{DD} = supply current

C_{CLKOUT} = capacitance on pin CLKOUT

V_{DD} = supply voltage

f_{CLKOUT} = output frequency on pin CLKOUT

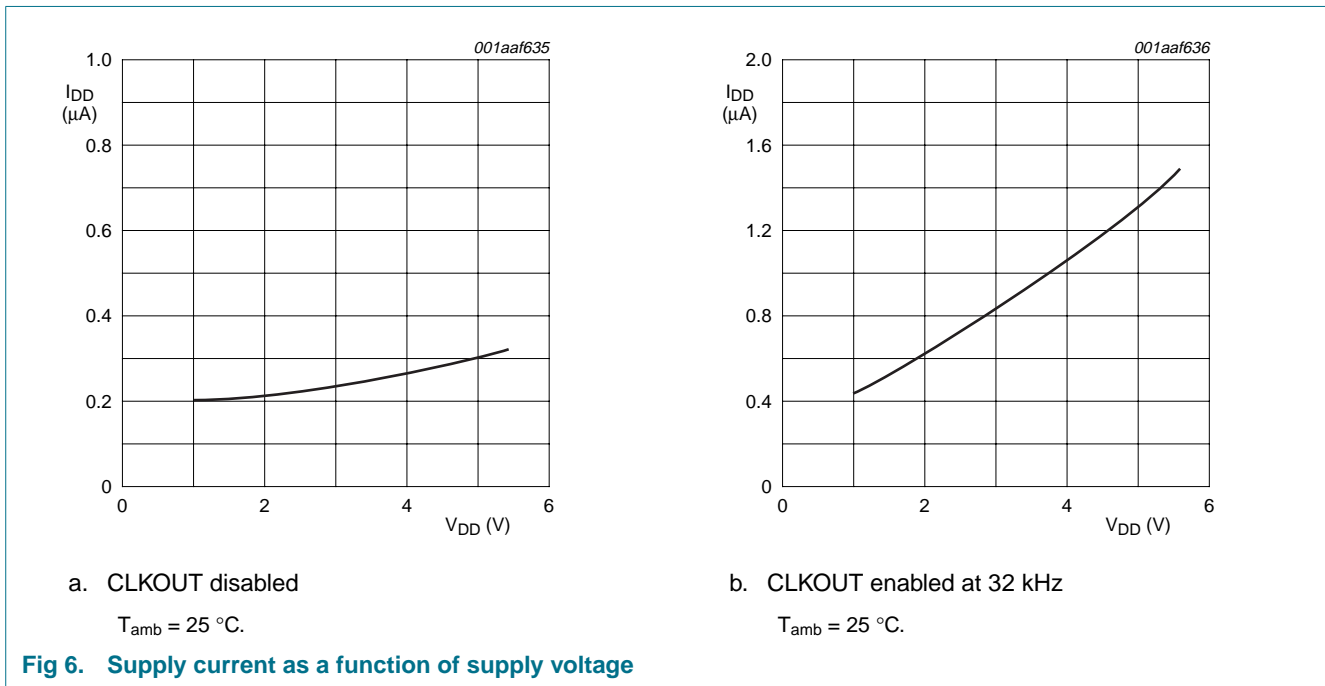
12. Dynamic characteristics

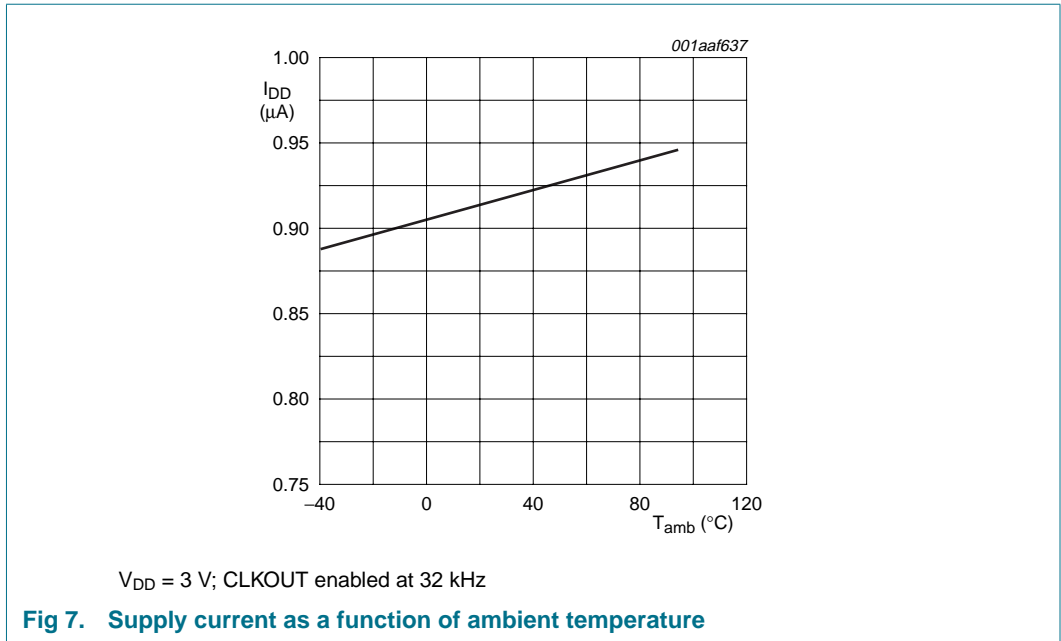
Table 6. Dynamic characteristics

$V_{DD} = 1.5\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; $f_{osc} = 32.768\text{ kHz}$; quartz $R_s = 40\text{ k}\Omega$ and $C_L = 8\text{ pF}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Oscillator						
$C_{L(itg)}$	integrated load capacitance		[1] 6	8	10	pF
$\Delta f_{osc}/f_{osc}$	relative oscillator frequency variation	$\Delta V_{DD} = 200\text{ mV}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$	-	0.2	-	ppm

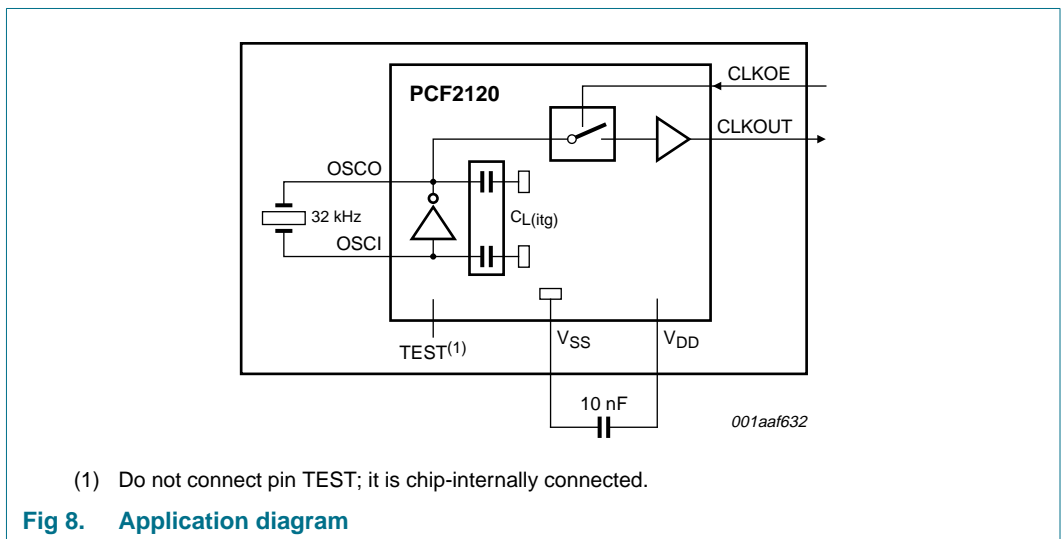
[1] $C_{L(itg)}$ is the combined equivalent integrated oscillator input and output capacitances.





13. Application information

You can mount the PCF2120 oscillator together with the quartz crystal as an accurate and pre-tuned quartz oscillator in one package.



14. Package outline

HVSON10: plastic thermal enhanced very thin small outline package; no leads;
10 terminals; body 3 x 3 x 0.85 mm

SOT650-1

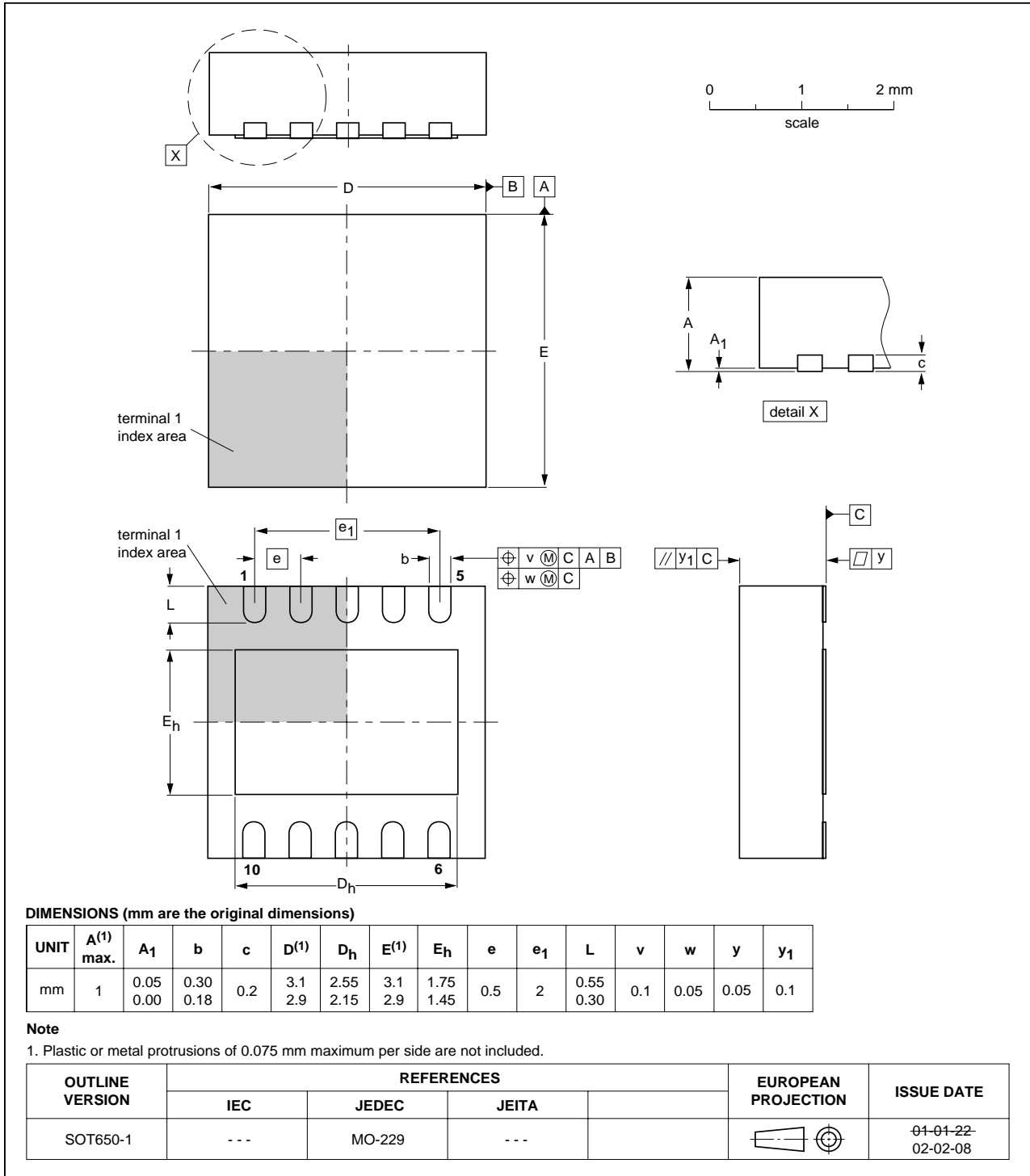


Fig 9. Package outline SOT650-1 (HVSON10)

15. Bare die outline

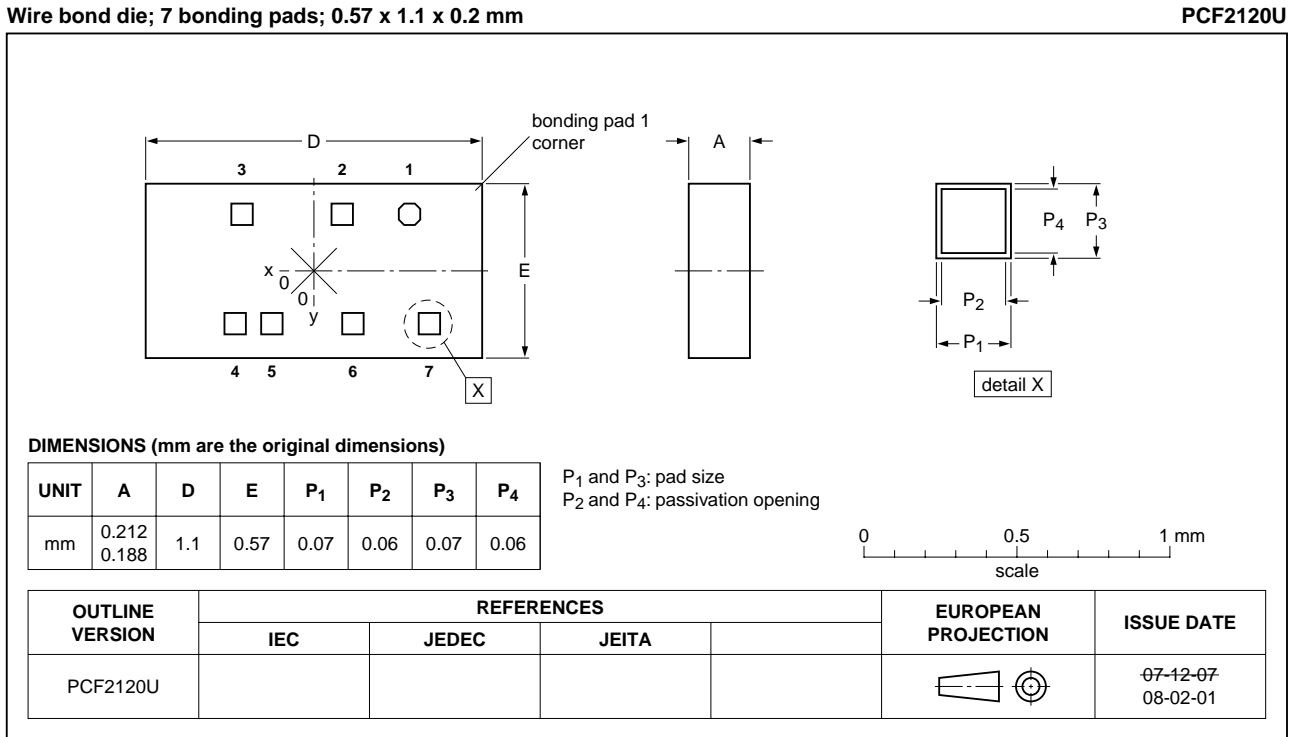


Fig 10. Bare die outline PCF2120U

Table 7. Bonding pad coordinates

Values x and y in μm .

Pad	x	y
1	+313	+187
2	+93	+187
3	-236	+187
4	-259	-172
5	-137	-172
6	+127	-172
7	+380	-172

16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 "Surface mount reflow soldering description".

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 11](#)) than a SnPb process, thus reducing the process window

- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 8](#) and [9](#)

Table 8. SnPb eutectic process (from J-STD-020C)

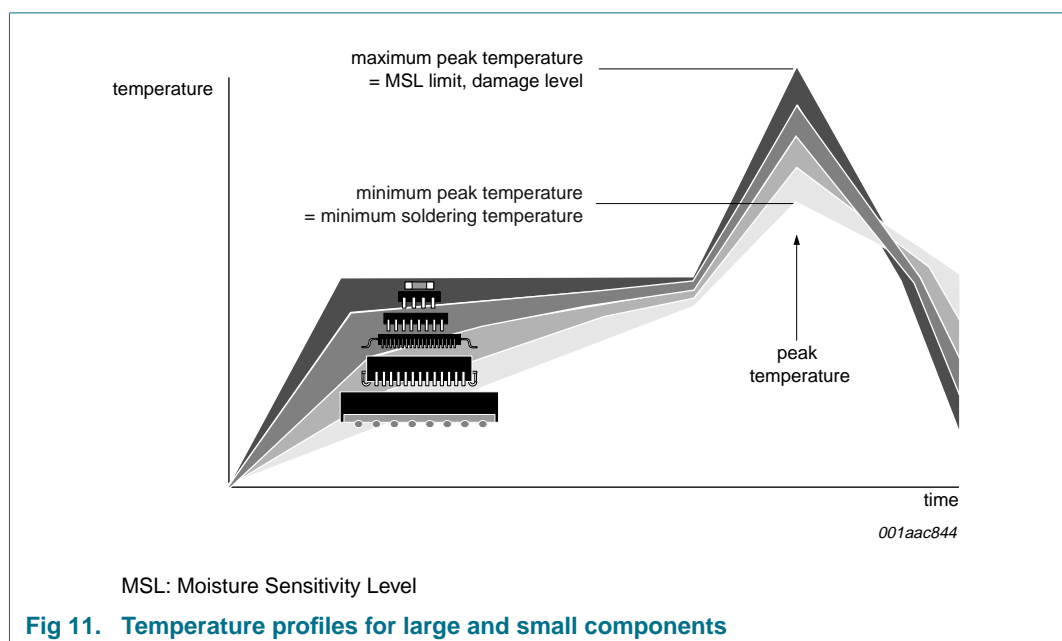
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm ³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 9. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm ³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 11](#).



For further information on temperature profiles, refer to Application Note AN10365
"Surface mount reflow soldering description".

17. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF2120_1	20080205	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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