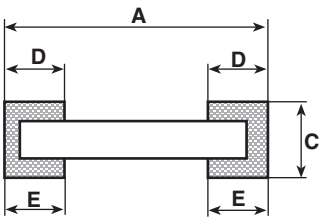
Very High Precision, Very High Stability Thin Chip Resistors

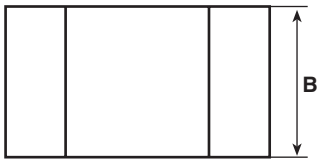
For low noise and precision applications, superior stability, low temperature coefficient of resistance, and low voltage coefficient, VISHAY SFERNICE's precision thin film wrap-around resistors exceed requirements of MIL-PRF-55342G characteristics Y (± 10ppm/°C).

FEATURES

- Load Life Stability at ± 70°C For 2000 hours: 0.15% under Pn
- Low Temperature Coefficient down to ± 10ppm/°C
- Very Low Noise and Voltage Coefficient
- Resistance Range: 50Ω to 3MΩ (depending on size)
- Laser Trimmed Tolerances to ± 0.01%
- TCR in Lot Tracking ≤ 5ppm/°C
- Termination: Thin Film Technology
- Gold Plated or Pre-tinned Terminations over Nickel Barrier

DIMENSIONS in millimeters





CASE SIZE	DIMENSIONS			
	A MAX. TOL. + 0.64 MIN. TOL. - 0.13	B MAX. TOL. +0.26 MIN. TOL. - 0.13	C MAX. TOL. + 0.64 MIN. TOL. - 0.13	D/E MAX. TOL. + 0.13 MIN. TOL. - 0.13
0603	1.52	0.75	0.38	0.38
0805	1.91	1.27	0.38	0.38
1206	3.0	1.60	0.38	0.38
2010	5.08	2.54	0.38	0.60[1]

Note [1]: tolerance ± 0.25

ORDERING INFORMATION

PHR SERIES	0603 CASE STYLE	Y TCR	1003 OHMIC VALUE	P TOLERANCE	B TERMINATION
PHR = Hi Rel chip	0603 0805 1206 2010	Y = ± 10ppm/°C (Digit 1) Z = ± 5ppm/°C (Digit 0) E = ± 25ppm/°C (Digit 2)	The first three digits (2 digits are enough for tolerance G and J) are significant figures and the last digit specifies the number of zero to follow. R designates decimal point 10 R0 = 10Ω 3901 = 3900Ω 1004 = 1MΩ	L = ± 0.01% P = ± 0.02% W = ± 0.05% B = ± 0.10%	B: tinned over nickel barrier (type E4) G: gold over nickel barrier (type E7)

ELECTRICAL SPECIFICATIONS

VISHAY SFERNICE DESIGNATION	PHR 0603	PHR 0805	PHR 1206	PHR 2010
ESA Specification Applied	SCC 4001/023			
Variant Number	01 - 05	02 - 06	03 - 07	04 - 08
Power Rating at + 70°C (Pn)	0.1W	0.125W	0.25W	0.5W
Limiting Element Voltage (UL)	35V	75V	100V	150V
Ohmic Value Range	Min. 50Ω Max. 200kΩ	Min. 50Ω Max. 250kΩ	Min. 50Ω Max. 1MΩ	Min. 50Ω 3MΩ
Insulation Voltage (Ui)	70V	150V	200V	300V
Temperature Coefficient	± 10ppm/°C; ± 25ppm/°C ± 5ppm/°C (22 to 70°C)			
Tolerance	± 0.01% (R > 250Ω), ± 0.02% (R > 100Ω), ± 0.05%, ± 0.1%			
Temperature Range	- 55°C/+ 155°C			
Soldering Temperature (Tsol)	260°C, immersion 10 sec.			

MECHANICAL SPECIFICATIONS

Substrate Alumina

Technology Thin Film

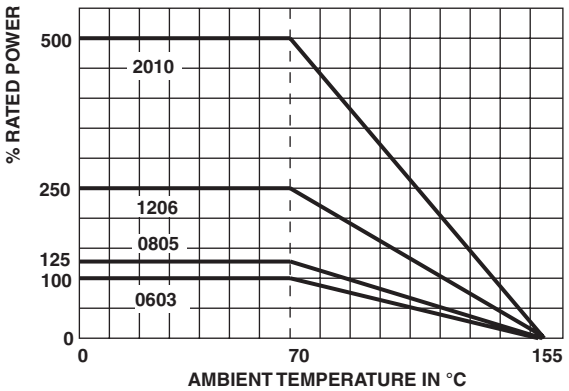
Film **Nickel Chromium** with mineral passivation

Protection Epoxy and Silicon

Terminations **B type**: pre-tinned over nickel barrier for solder reflow

G type: gold over nickel barrier for other applications (not under qualification)

POWER DERATING CURVE



PACKAGING

Two types of packaging are available: waffle-pack and tape and reel.

SIZE	NUMBER OF PIECES PER PACKAGE			TAPE WIDTH
	WAFFLE PACK 2" X 2"	TAPE AND REEL MIN	TAPE AND REEL MAX	
0603	100	250	4000	8 mm
0805				
1206	140			
2010	60			8 mm*

*12 mm on request

EXTENDED FEATURES

You may consult VISHAY SFERNICE for chip sizes, ohmic values and tolerances outside the qualified range.

PERFORMANCE

TEST	CONDITIONS	REQUIREMENTS		TYPICAL
		ESA/SCC 4001/023	MIL-PRF-55342G	
Short Time Overload	$U = \sqrt{6.25 \bullet Pn \bullet Rn/2s}$ U maxi < 2 UL	± 0.05% Rn + 0.05Ω	± 0.10%	± 0.01
Rapid Temperature Change	- 55°C/ + 155°C 5 cycles CEI 66-2-14 Test Na	± 0.05% Rn + 0.05Ω	± 0.1% (For 100 Cycles)	± 0.01% ± 0.015% (For 500 Cycles)
Soldering (Thermal Shock)	260°C/10s CEI 68 - 2 - 20 A Test T6 (met. 1A)	± 0.05% Rn + 0.05Ω	–	± 0.005%
Terminal Strength: Adhesion Bend Strength of End Plated Facing	 CEI 115 - 1 Clause 4.32 CEI 115 - 1 Clause 4.33	± 0.05% Rn + 0.05Ω	–	± 0.01%
Climatic Sequence	CEI 67 - 2 - 1/CEI 68 - 2 - 2 CEI 67 - 2 - 13/CEI 68 - 2- 30	± 0.10% Rn + 0.05Ω	–	± 0.02% Insulation Resistance > 1GΩ
Load Life	2000 Hours Pn at + 70°C 90'/30' Cycle	± 0.15% Rn + 0.05Ω	± 0.5%	± 0.02% Insulation Resistance > 1GΩ
High Temperature Exposure	2000 Hours Pn at + 155°C CEI 68 - 2 - 20A Test B	± 0.15% Rn + 0.05Ω	± 0.10% (Duration 100h)	± 0.05% Insulation Resistance > 1GΩ