

DATA SHEET

TDA1517ATW 8 W BTL or 2 × 4 W SE power amplifier

Product specification
Supersedes data of 2001 Feb 14
File under Integrated Circuits, IC01

2001 Apr 17

8 W BTL or 2 × 4 W SE power amplifier**TDA1517ATW****FEATURES**

- Requires very few external components
- Flexibility in use: mono Bridge-Tied Load (BTL) and stereo Single-Ended (SE); it should be noted that in stereo applications the outputs of both amplifiers are in opposite phase
- High output power
- Low offset voltage at output (important for BTL)
- Fixed gain
- Good ripple rejection
- Mode select switch (operating, mute and standby)
- AC and DC short-circuit safe to ground and V_P
- Electrostatic discharge protection
- Thermal protection
- Reverse polarity safe
- Capable of handling high energy on outputs ($V_P = 0$ V)
- No switch-on/switch-off plop
- Low thermal resistance.

GENERAL DESCRIPTION

The TDA1517ATW is an integrated class-AB output amplifier contained in a plastic heatsink thin shrink small outline package (HTSSOP20). The device is primarily developed for multimedia applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage		6	12	18	V
I_{ORM}	repetitive peak output current		–	–	2.5	A
$I_{q(tot)}$	total quiescent current		–	40	80	mA
I_{stb}	standby current		–	0.1	100	μ A
SE application						
P_o	output power	THD = 10%; $R_L = 4 \Omega$	–	4	–	W
SVRR	supply voltage ripple rejection	$R_S = 0 \Omega$	46	–	–	dB
α_{cs}	channel separation	$R_S = 10 \text{ k}\Omega$	40	55	–	dB
$V_{n(o)}$	noise output voltage	$R_S = 0 \Omega$	–	50	–	μ V
$ Z_i $	input impedance		50	–	–	$\text{k}\Omega$
BTL application						
P_o	output power	THD = 10%; $R_L = 8 \Omega$	–	8	–	W
SVRR	supply voltage ripple rejection	$R_S = 0 \Omega$	50	–	–	dB
$ \Delta V_{OO} $	output offset voltage		–	–	150	mV
$V_{n(o)(offset)}$	noise output offset voltage	$R_S = 0 \Omega$	–	70	–	μ V
$ Z_i $	input impedance		25	–	–	$\text{k}\Omega$

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1517ATW	HTSSOP20	plastic, heatsink thin shrink small outline package; 20 leads; body width 4.4 mm	SOT527-1

8 W BTL or 2 × 4 W SE power amplifier

TDA1517ATW

BLOCK DIAGRAM

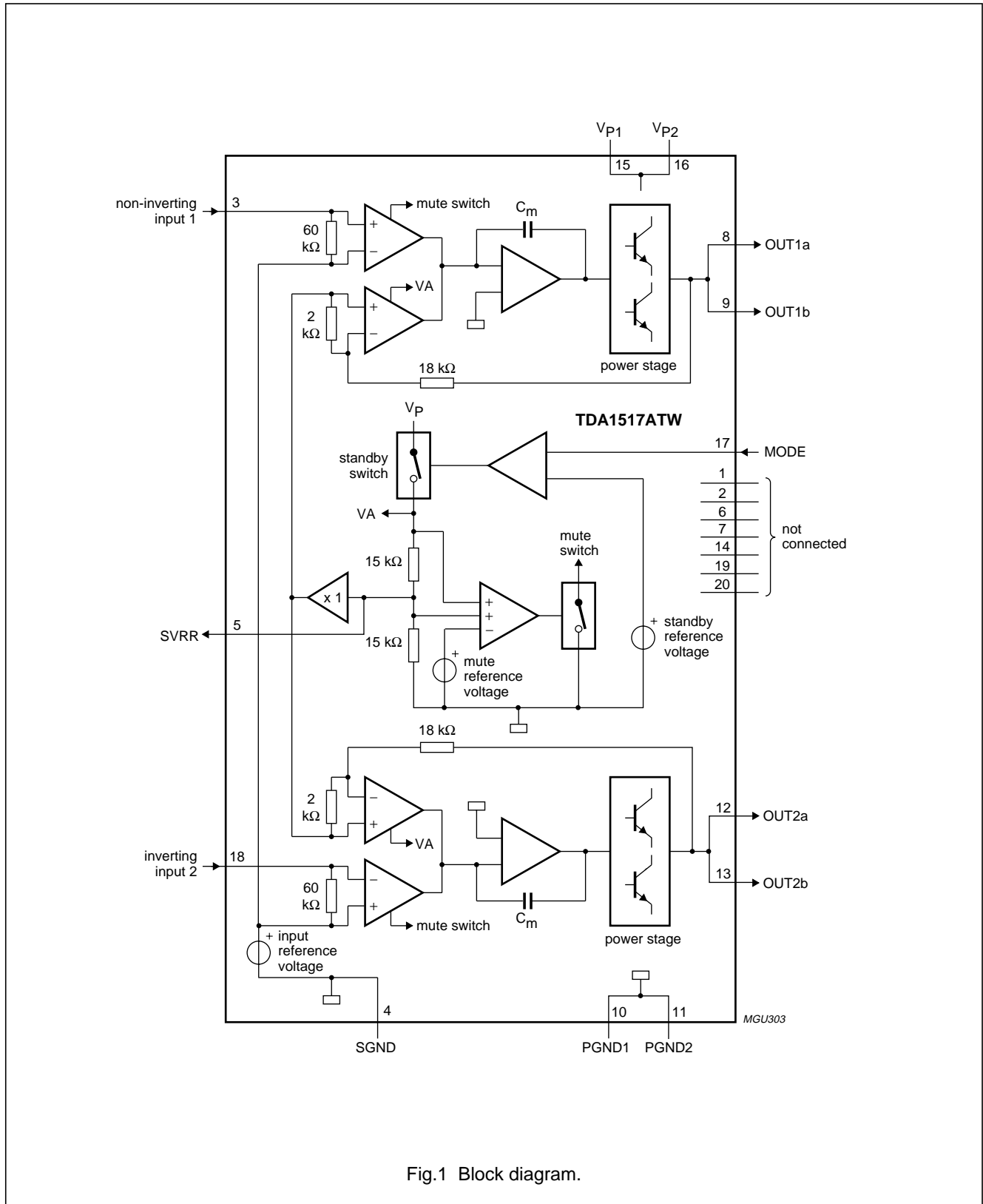


Fig.1 Block diagram.

8 W BTL or 2 × 4 W SE power amplifier

TDA1517ATW

PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
n.c.	2	not connected
IN1+	3	non-inverting input 1
SGND	4	signal ground
SVRR	5	supply voltage ripple rejection
n.c.	6	not connected
n.c.	7	not connected
OUT1a	8	output 1a
OUT1b	9	output 1b
PGND1	10	power ground 1
PGND2	11	power ground 2
OUT2a	12	output 2a
OUT2b	13	output 2b
n.c.	14	not connected
V _{P1}	15	supply voltage 1
V _{P2}	16	supply voltage 2
MODE	17	mode select switch
IN2-	18	inverting input 2
n.c.	19	not connected
n.c.	20	not connected

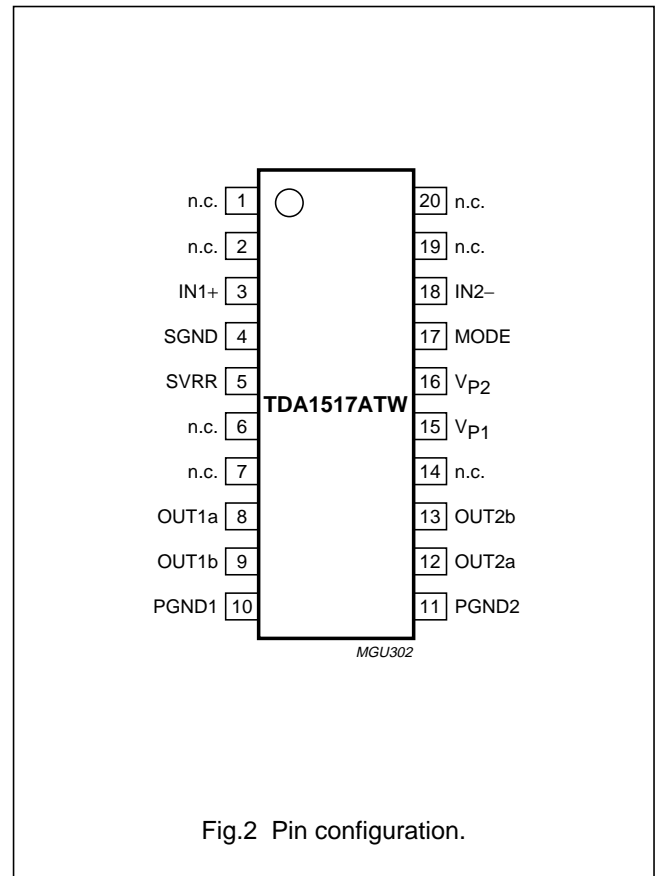


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA1517ATW contains two identical amplifiers with differential input stages. This device can be used for Bridge-Tied Load (BTL) or Single-Ended (SE) applications. The gain of each amplifier is fixed at 20 dB. A special feature of this device is the mode select switch. Since this pin has a very low input current (<40 µA), a low cost supply switch can be used. With this switch the TDA1517ATW can be switched into three modes:

- Standby: low supply current
- Mute: input signal suppressed
- Operating: normal on condition.

8 W BTL or 2 × 4 W SE power amplifier

TDA1517ATW

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT.
V_P	supply voltage		–	18	V
V_{PSC}	AC and DC short-circuit-safe voltage		–	18	V
V_{rp}	reverse polarity voltage		–	6	V
ERG_o	energy handling capability at outputs	$V_P = 0$ V	–	200	mJ
I_{OSM}	non-repetitive peak output current		–	4	A
I_{ORM}	repetitive peak output current		–	2.5	A
P_{tot}	total power dissipation		–	5	W
T_{vj}	virtual junction temperature		–	150	°C
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–40	+85	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
tbf			–	–

DC CHARACTERISTICS $V_P = 12$ V; $T_{amb} = 25$ °C; measured in Fig.3; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage	note 1	6.0	12	18	V
I_q	quiescent current	$R_L = \infty$	–	40	80	mA
Operating condition						
$V_{MODE(oper)}$	mode switch voltage level		8.5	–	V_P	V
$I_{MODE(oper)}$	mode switch current	$V_{MODE} = 12$ V	–	15	40	μA
V_O	DC output voltage		–	5.7	–	V
$ \Delta V_{OO} $	DC output offset voltage		–	–	150	mV
Mute condition						
$V_{MODE(mute)}$	mode switch voltage level		3.3	–	6.4	V
V_O	DC output voltage		–	5.7	–	V
$ \Delta V_{OO} $	DC output offset voltage		–	–	150	mV
Standby condition						
$V_{MODE(stb)}$	mode switch voltage level		0	–	2	V
I_{stb}	standby current		–	0.1	100	μA

Note1. The circuit is DC adjusted at $V_P = 6$ to 18 V and AC operating at $V_P = 8.5$ to 18 V.

8 W BTL or 2 × 4 W SE power amplifier

TDA1517ATW

AC CHARACTERISTICS

$V_P = 12\text{ V}$; $f = 1\text{ kHz}$; $T_{\text{amb}} = 25\text{ °C}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SE application; note 1						
P_o	output power	note 2				
		THD = 1%	2.5	3.3	–	W
		THD = 10%	3	4	–	W
THD	total harmonic distortion	$P_o = 1\text{ W}$	–	0.1	–	%
$f_{ro(L)}$	low frequency roll-off	–1 dB; note 3	–	25	–	Hz
$f_{ro(H)}$	high frequency roll off	–1 dB	20	–	–	kHz
G_V	voltage gain		19	20	21	dB
$ \Delta G_V $	channel balance		–	–	1	dB
SVRR	supply voltage ripple rejection	note 4				
		on	46	–	–	dB
		mute	46	–	–	dB
		standby	80	–	–	dB
$ Z_i $	input impedance		50	60	75	k Ω
$V_{n(o)(rms)}$	noise output voltage (RMS value)	note 5				
		on; $R_S = 0\ \Omega$	–	50	–	μV
		on; $R_S = 10\ \text{k}\Omega$	–	70	100	μV
		mute; note 6	–	50	–	μV
α_{CS}	channel separation	$R_S = 10\ \text{k}\Omega$	40	55	–	dB
$V_{o(mute)}$	output voltage in mute	note 7	–	–	2	mV
BTL application; note 8						
P_o	output power	note 2				
		THD = 1%	5	6.6	–	W
		THD = 10%	6.5	8.0	–	W
THD	total harmonic distortion	$P_o = 1\text{ W}$	–	0.03	–	%
$f_{ro(L)}$	low frequency roll-off	–1 dB; note 3	–	25	–	Hz
$f_{ro(H)}$	high frequency roll off	–1 dB	20	–	–	kHz
G_V	voltage gain		25	26	27	dB
SVRR	supply voltage ripple rejection	note 4				
		on	50	–	–	dB
		mute	50	–	–	dB
		standby	80	–	–	dB
$ Z_i $	input impedance		25	30	38	k Ω
$V_{n(o)(rms)}$	noise output voltage (RMS value)	note 5				
		on; $R_S = 0\ \Omega$	–	70	–	μV
		on; $R_S = 10\ \text{k}\Omega$	–	100	200	μV
		mute; note 6	–	60	–	μV
$V_{o(mute)}$	output voltage in mute	note 7	–	–	2	mV

8 W BTL or 2 × 4 W SE power amplifier

TDA1517ATW

Notes to the characteristics

1. $R_L = 4 \Omega$, measured in Fig.4.
2. Output power is measured directly at the output pins of the IC.
3. Frequency response externally fixed.
4. $V_{ripple} = V_{ripple(max)} = 2 \text{ V (p-p)}$; $R_S = 0 \Omega$.
5. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
6. Noise output voltage independent of R_S .
7. $V_i = V_{i(max)} = 1 \text{ V (RMS)}$.
8. $R_L = 8 \Omega$, measured in Fig.3.

APPLICATION INFORMATION

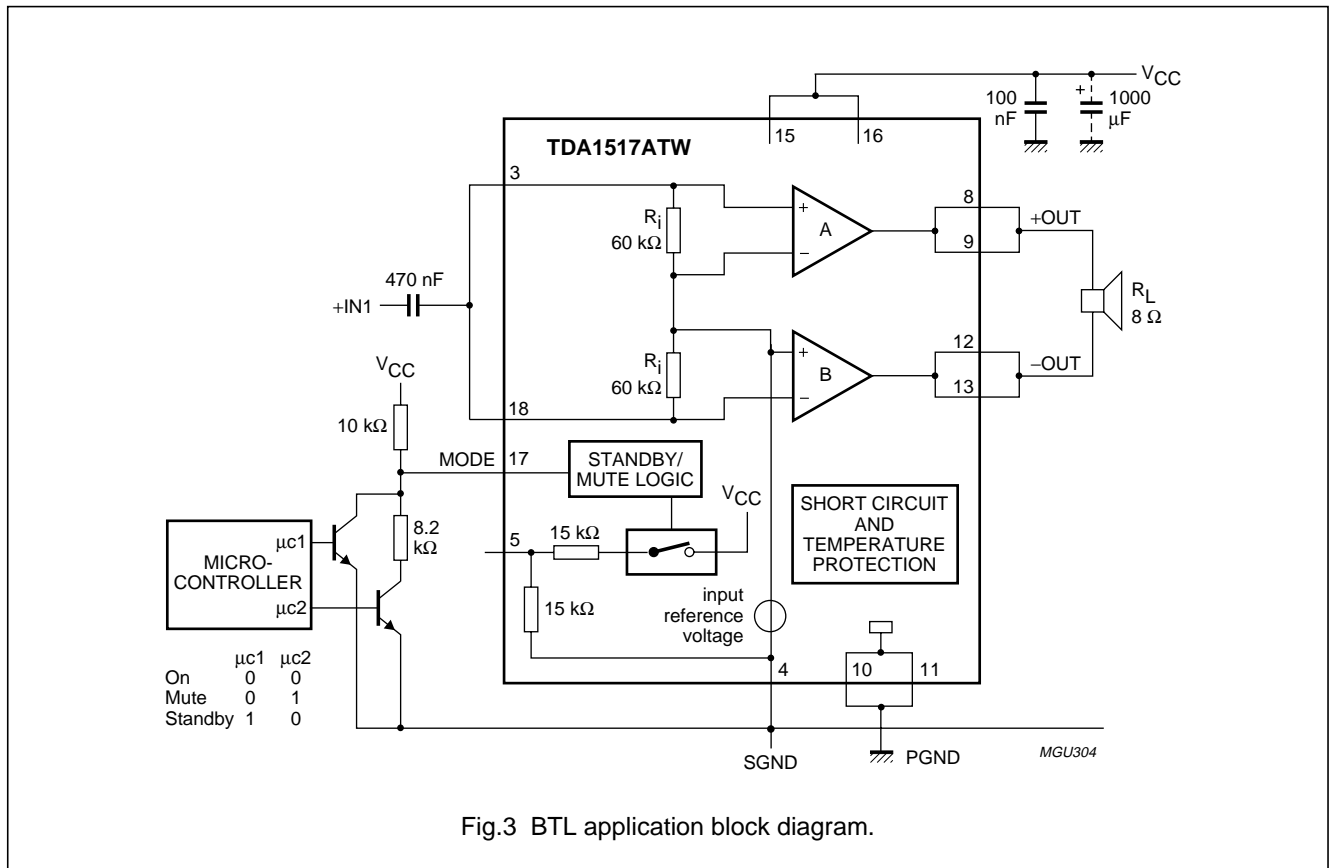


Fig.3 BTL application block diagram.

8 W BTL or 2 × 4 W SE power amplifier

TDA1517ATW

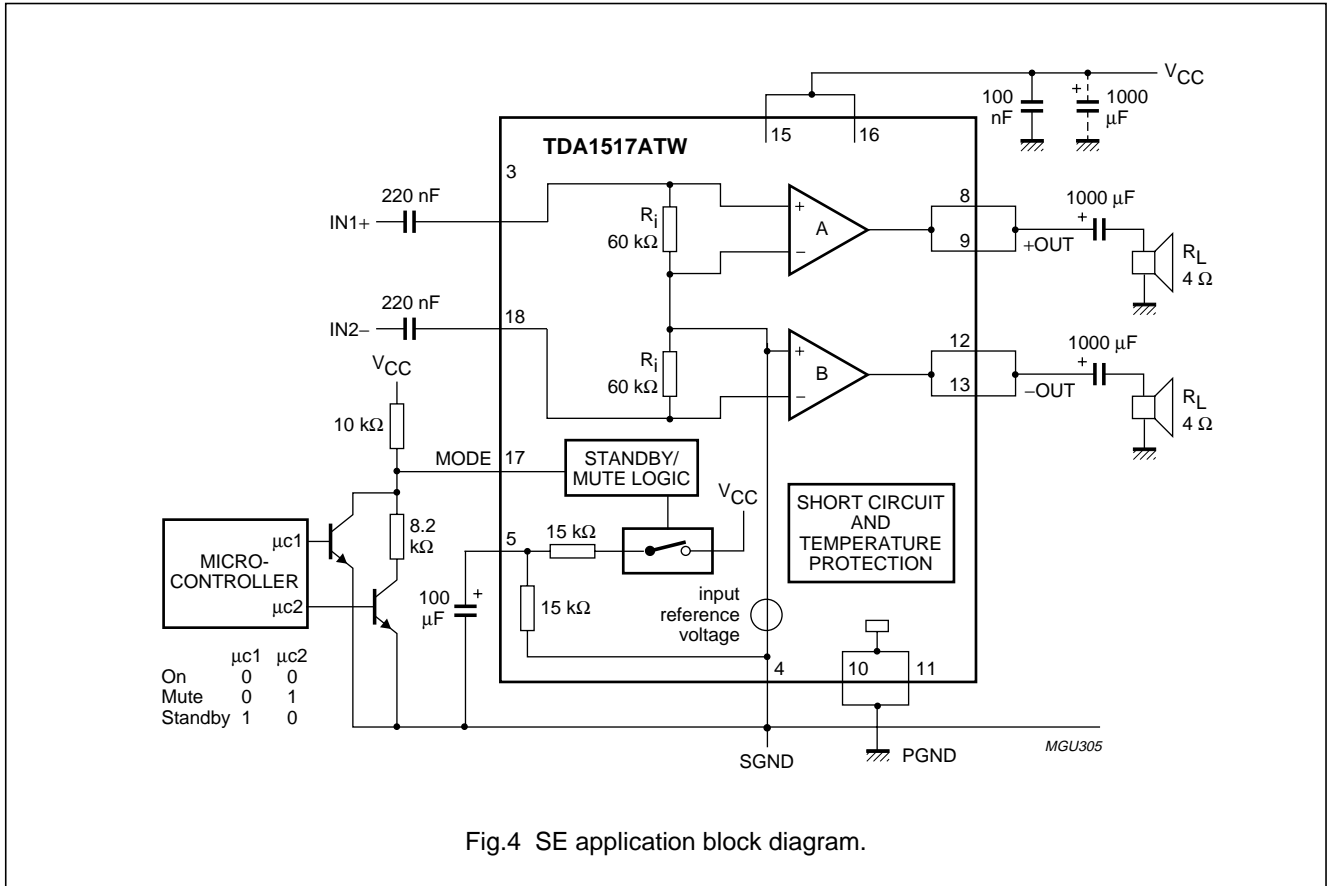


Fig.4 SE application block diagram.

Test conditions

T_{amb} = 25 °C; unless otherwise specified: V_P = 12 V, BTL application, f = 1 kHz, R_L = 8 Ω, fixed gain = 26 dB, audio band-pass: 22 Hz to 22 kHz. In the figures as a function of frequency a band-pass of 10 Hz to 80 kHz was applied.

The BTL application block diagram is shown in Fig.3. The PCB layout [which accommodates both the mono (BTL) and stereo (single-ended) application] is shown in Fig.6.

Printed-Circuit Board (PCB) layout and grounding

For high system performance levels certain grounding techniques are imperative. The input reference grounds have to be tied to their respective source grounds and must have separate traces from the power ground traces; this will separate the large (output) signal currents from interfering with the small AC input signals. The small signal ground traces should be located physically as far as possible from the power ground traces. Supply and output traces should be as wide as possible for delivering maximum output power.

Proper supply bypassing is critical for low noise performance and high power supply rejection. The respective capacitor locations should be as close as possible to the device and grounded to the power ground. Decoupling the power supply also prevents unwanted oscillations. For suppressing higher frequency transients (spikes) on the supply line a capacitor with low ESR (typical 0.1 μF) has to be placed as close as possible to the device. For suppressing lower frequency noise and ripple signals, a large electrolytic capacitor (e.g. 1000 μF or greater) must be placed close to the IC.

In single-ended (stereo) application a bypass capacitor connected to pin SVR reduces the noise and ripple on the midrail voltage. For good THD and noise performance a low ESR capacitor is recommended.

Input configuration

It should be noted that the DC level of the input pins is approximately 2.1 V; a coupling capacitor is therefore necessary.

8 W BTL or 2 × 4 W SE power amplifier

TDA1517ATW

The formula for the cut-off frequency at the input is as

$$\text{follows: } f_{IC} = \frac{1}{2 \times \pi \times R_i C_i}$$

$$\text{thus } f_{IC} = \frac{1}{2 \times \pi \times 30 \times 10^{-3} \times 470 \times 10^{-9}} = 11 \text{ Hz}$$

As can be seen it is not necessary to use high capacitor values for the input; so the delay during switch-on, which is necessary for charging the input capacitors, can be minimized. This results in a good low frequency response and good switch-on behaviour.

In stereo applications (single-ended) coupling capacitors on both input and output are necessary. It should be noted that the outputs of both amplifiers are in opposite phase.

Built-in protection circuits

The IC contains two types of protection circuits:

- Short-circuits the outputs to ground, the supply to ground and across the load: short-circuit is detected and controlled by a SOAR protection circuit
- Thermal shut-down protection: the junction temperature is measured by a temperature sensor. Thermal foldback is activated at a junction temperature of >150 °C.

Output power

The output power as a function of supply voltage has been measured on the output pins and at THD = 10%. The maximum output power is limited by the maximum allowable power dissipation and the maximum available output current, 2.5 A repetitive peak current.

Supply voltage ripple rejection

The SVRR has been measured without an electrolytic capacitor on pin 5 and at a bandwidth of 10 Hz to 80 kHz. The curves for operating and mute condition (respectively) were measured with $R_{\text{source}} = 0 \Omega$. Only in single-ended applications is an electrolytic capacitor (e.g. 100 μF) on pin 5 necessary to improve the SVRR behaviour.

Headroom

A typical music CD requires at least 12 dB (is factor 15.85) dynamic headroom (compared with the average power output) for passing the loudest portions without distortion. The following calculation can be made for this application at $V_P = 12 \text{ V}$ and $R_L = 8 \Omega$: P_o at THD = 0.1% is approximately 5 W (see Fig.7).

Average listening level without any distortion yields:

$$P_{\text{ALL}} = \frac{P_{\text{tot}}}{\text{factor}} = \frac{5}{15.85} = 315 \text{ mW}$$

The power dissipation can be derived from Fig.11 for 0 dB and 12 dB headroom.

Table 1 Power rating

RATING	HEADROOM	POWER DISSIPATION
$P_o = 5 \text{ W}$ (THD = 0.1%)	0 dB	3.5 W
	12 dB	2.0 W

Thus for the average listening level (music power) a power dissipation of 2.0 W can be used for the thermal PCB calculation; see Section "Thermal behaviour (PCB design considerations)".

Mode pin

For the 3 functional modes: standby, mute and operate, the MODE pin can be driven by a 3-state logic output stage, e.g. a microcontroller with some extra components for DC-level shifting; see Fig.10 for the respective DC levels.

- Standby mode is activated by a low DC level between 0 and 2 V. The power consumption of the IC will be reduced to <0.12 mW.
- Mute mode is activated by a DC level between 3.3 and 6.4 V. The outputs of the amplifier will be muted (no audio output); however the amplifier is DC biased and the DC level of the output pins stays at half the supply voltage. The input coupling capacitors are charged when in mute mode to avoid pop-noise.
- The IC will be in the operating condition when the voltage at pin MODE is between 8.5 V and V_{CC} .

Switch-on/switch-off

To avoid audible plops during switch-on and switch-off of the supply voltage, the MODE pin has to be set in standby condition (V_{CC} level) before the voltage is applied (switch-on) or removed (switch-off). The input and SVRR capacitors are smoothly charged during mute mode.

The turn-on and turn-off time can be influenced by an RC-circuit connected to the MODE pin. Switching the device or the MODE pin rapidly on and off may cause 'click and pop' noise. This can be prevented by proper timing on the MODE pin. Further improvement in the BTL application can be obtained by connecting an electrolytic capacitor (e.g. 100 μF) between the SVRR pin and signal ground.

8 W BTL or 2 × 4 W SE power amplifier

TDA1517ATW

Thermal behaviour (PCB design considerations)

The typical thermal resistance [$R_{th(j-a)}$] of the IC in the HTSSOP20 package is 37 K/W if the IC is soldered on a printed-circuit board with double sided 35 μm copper with a minimum area of approximately 30 cm^2 . The actual usable thermal resistance depends strongly on the mounting method of the device on the printed-circuit board, the soldering method and the area and thickness of the copper on the printed-circuit board.

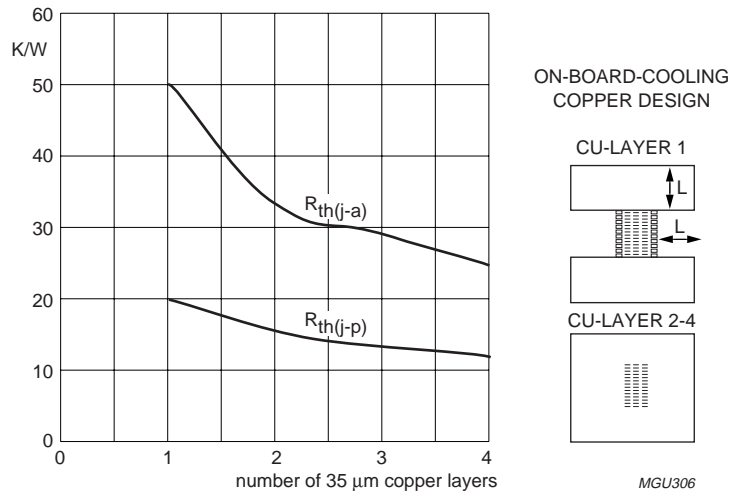
The bottom 'heat-spreader' of the IC has to be soldered efficiently on the 'thermal land' of the copper area of the printed-circuit board using the re-flow solder technique.

A number of thermal vias in the 'thermal land' provide a thermal path to the opposite copper site of the printed-circuit board. The size of the surface layers should be as large as needed to dissipate the heat.

The thermal vias (0.3 mm \varnothing) in the 'thermal land' should not use web construction techniques, because those will have high thermal resistance; continuous connection completely around the via-hole is recommended.

For a maximum ambient temperature of 60 $^{\circ}\text{C}$ the following calculation can be made: for the application at $V_P = 12\text{ V}$ and $R_L = 8\ \Omega$ the (ALL-) music power dissipation approximately 2.0 W;
 $T_{j(max)} = T_{amb} + P \times R_{th(j-a)} = 60\ ^{\circ}\text{C} + 2.0 \times 37 = 134\ ^{\circ}\text{C}$.

Note: the above calculation holds for application at 'average listening level' music output signals. Applying (or testing) with sine wave signals will produce approximately twice the music power dissipation; at worst case condition this can activate the maximum temperature protection.



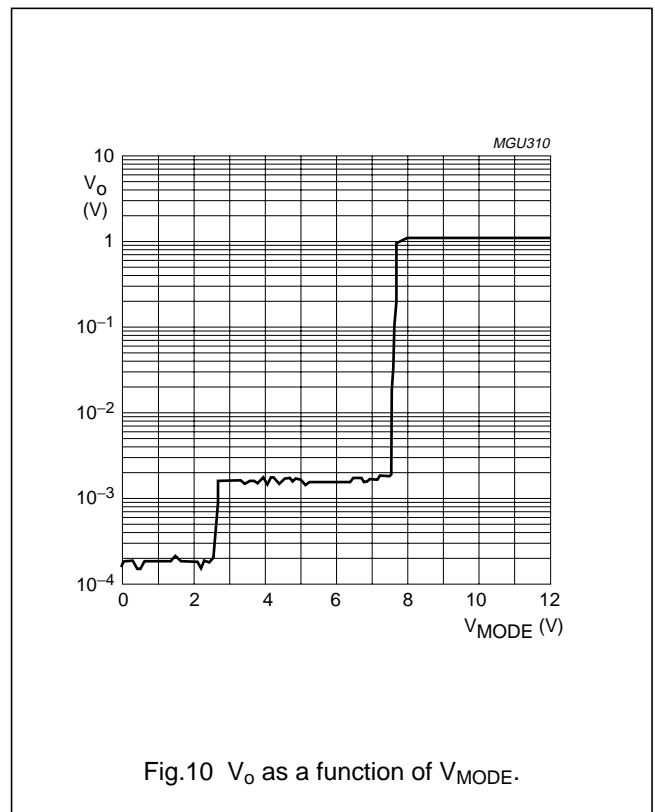
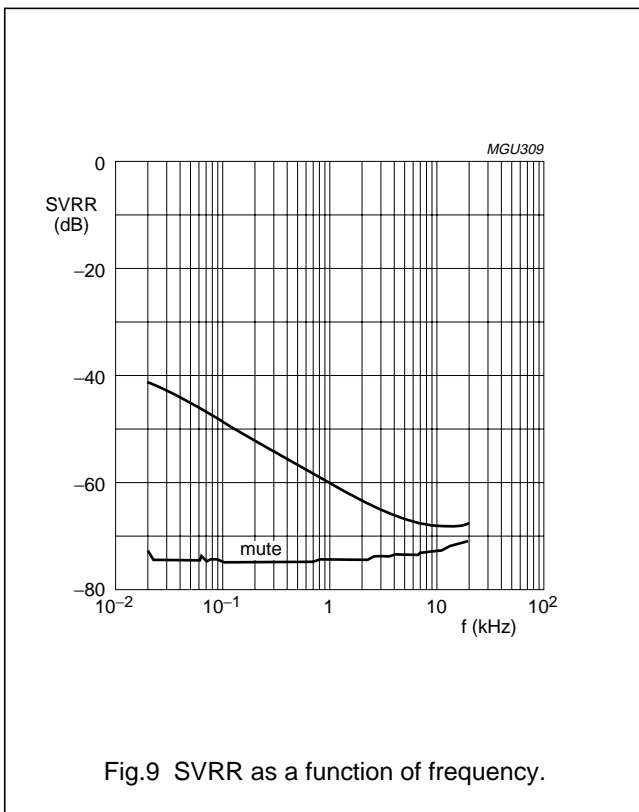
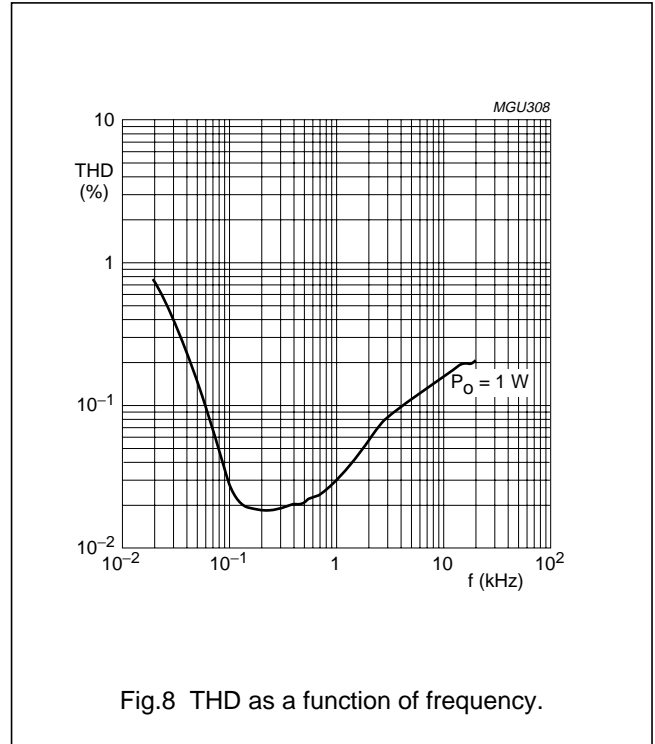
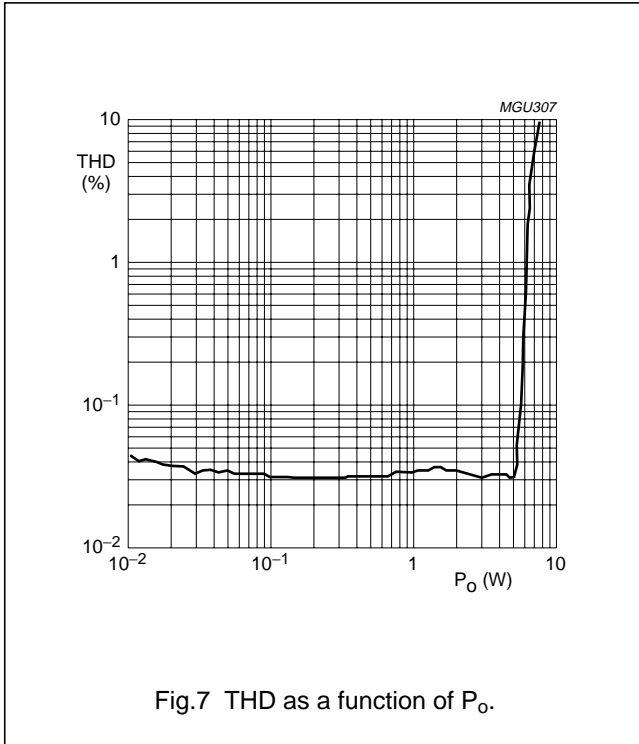
$R_{th(j-p)}$ curve is given for practical calculation purpose.
 L = 30 mm plus vias

Fig.5 Thermal resistance of the HTSSOP20 mounted on printed-circuit board.

8 W BTL or 2 × 4 W SE power amplifier

TDA1517ATW

Typical performance characteristics for BTL application at $V_P = 12\text{ V}$ and $R_L = 8\ \Omega$



8 W BTL or 2 × 4 W SE power amplifier

TDA1517ATW

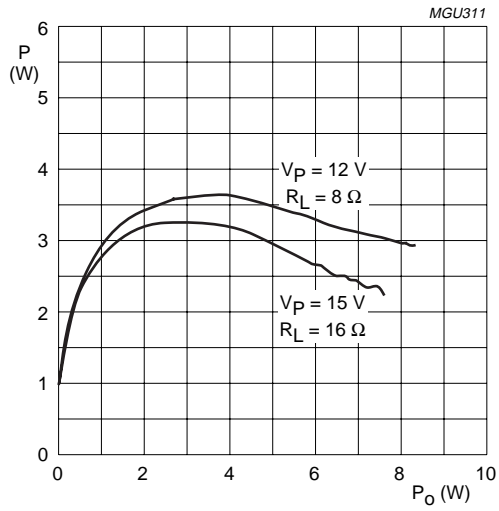


Fig.11 Power dissipation as a function of P_o .

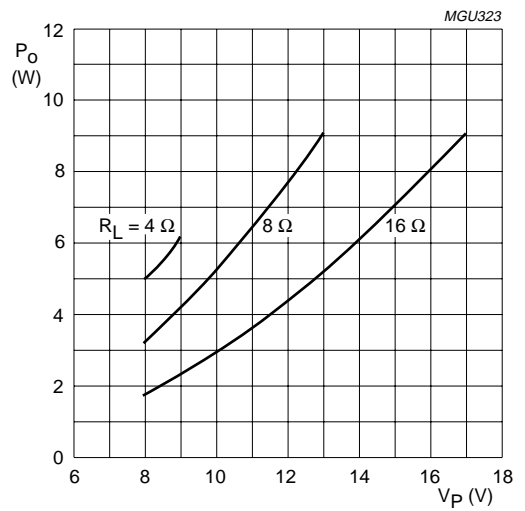


Fig.12 P_o as a function of V_p .

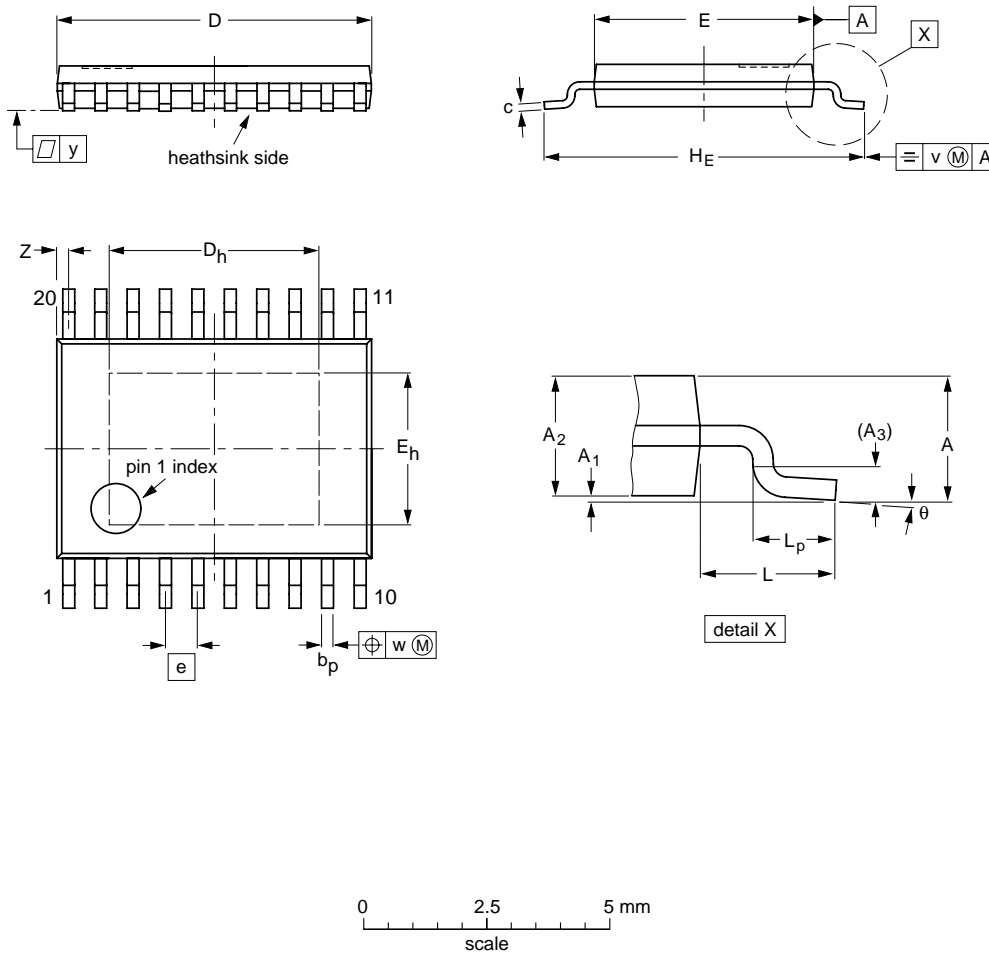
8 W BTL or 2 × 4 W SE power amplifier

TDA1517ATW

PACKAGE OUTLINE

HTSSOP20: plastic, heatsink thin shrink small outline package; 20 leads; body width 4.4 mm

SOT527-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	D _h	E ⁽²⁾	E _h	e	H _E	L	L _p	v	w	y	z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.20 0.09	6.6 6.4	4.3 4.1	4.5 4.3	3.1 2.9	0.65	6.6 6.2	1.0	0.75 0.50	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT527-1						99-11-12- 00-07-12

8 W BTL or 2 × 4 W SE power amplifier

TDA1517ATW

SOLDERING**Introduction to soldering surface mount packages**

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our “*Data Handbook IC26; Integrated Circuit Packages*” (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferably be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
 - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
 - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

8 W BTL or 2 × 4 W SE power amplifier

TDA1517ATW

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW ⁽¹⁾
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable ⁽²⁾	suitable
PLCC ⁽³⁾ , SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended ⁽³⁾⁽⁴⁾	suitable
SSOP, TSSOP, VSO	not recommended ⁽⁵⁾	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

8 W BTL or 2 × 4 W SE power amplifier

TDA1517ATW

DATA SHEET STATUS

DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

8 W BTL or 2 × 4 W SE power amplifier

TDA1517ATW

NOTES

8 W BTL or 2 × 4 W SE power amplifier

TDA1517ATW

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 7 - 9 Rue du Mont Valérien, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4728 6600, Fax. +33 1 4728 6638

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: Philips Hungary Ltd., H-1119 Budapest, Fehervari ut 84/A,
Tel: +36 1 382 1700, Fax: +36 1 382 1800

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 5F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2451, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
60/14 MOO 11, Bangna Trad Road KM. 3, Bagna, BANGKOK 10260,
Tel. +66 2 361 7910, Fax. +66 2 398 3447

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 3341 299, Fax.+381 11 3342 553

For all other countries apply to: Philips Semiconductors,
Marketing Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN,
The Netherlands, Fax. +31 40 27 24825

Internet: <http://www.semiconductors.philips.com>

© Philips Electronics N.V. 2001

SCA 72

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Printed in The Netherlands

753503/02/pp20

Date of release: 2001 Apr 17

Document order number: 9397 750 08264

Let's make things better.

Philips
Semiconductors



PHILIPS