PRELIMINARY

CYL008M162FFB

128-Mbit (8-Mbit x 16) Low-Power MoBL4™ SDRAM

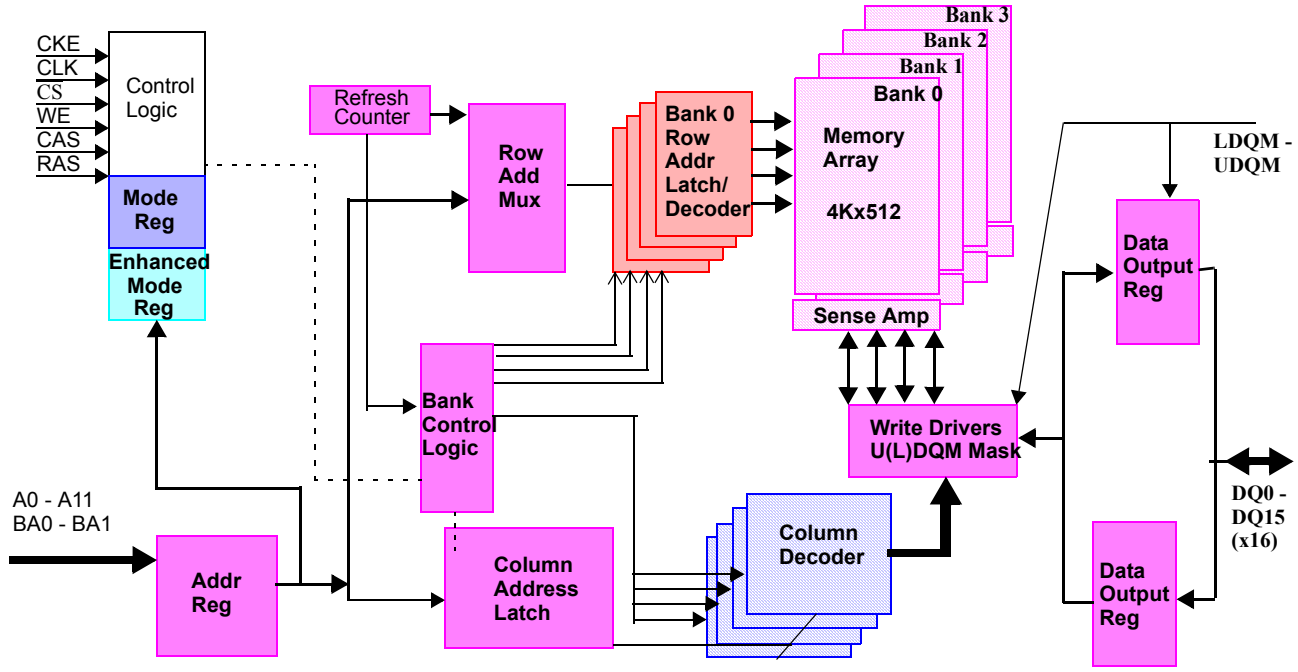
Features

- **Functionality**
  - **— Internal 4 Bank Operation**
  - **— Standard SDRAM Functionality**
  - **— Programmable burst lengths: 1, 2, 4, 8, or full page**
  - **— Compatible with JEDEC Low Power SDRAM Standard**
- **Low Power Features**
  - **— Low voltage power supply: 1.8V**
  - **— Temperature Compensated Self Refresh (TCSR)**
  - **— Partial Array Self Refresh power-saving mode**
  - **— Deep Sleep Mode**
  - **— Self Refresh Mode; standard and low power**
- **Temperature: –40°C to +85°C**
- **8 mm x 8 mm x 1.0 mm 54-ball 0.8 mm FBGA Package**

Functional Description[1]

The CYL008M162FFB is a high-performance CMOS Dynamic RAM (DRAM) organized as 8M x 16.This device features advanced circuit design to provide ultra-low active current and extremely low standby current. This is ideal for providing More Battery Life™ in portable applications such as wireless handsets. The device is compatible with the JEDEC standard LP-SDRAM specifications.

Logic Block Diagram



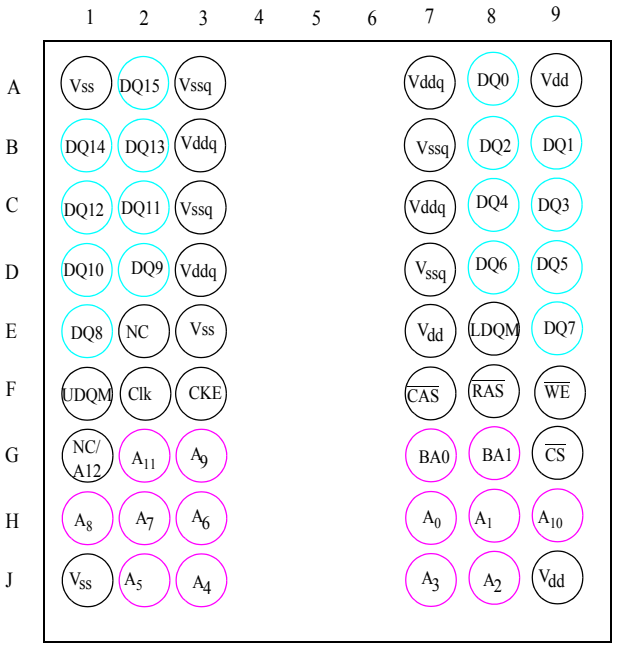
Selection Guide

Device	Voltage		Frequency	Access Time	t_{RCD}	t_{RP}
	Core	I/O		CL=2		
CYL008M162FFBU-1ABAI	1.7 - 1.95V	1.7 - Vdd	100Mhz	8ns	20ns	20ns

Note:
1. For best-practice recommendations, please refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com.

Pin Configuration

54 ball FBGA(8mm x 8mm x 1.0mm)



Pin Description

Name	Type	Description
CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	Clock Enable: CKE activates(HIGH) and deactivates(LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF Refresh operation(all banks idle), ACTIVE POWER-DOWN(row active in any bank) or CLOCK SUSPEND operation(burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
CS	Input	Chip Select: $\overline{CS}$ enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
$\overline{CAS}$, $\overline{RAS}$, $\overline{WE}$	Input	Command Inputs: $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
L(U)DQM	Input	Input/Output Mask: L(U)DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when during a READ cycle. LDQM corresponds to DQ0 – DQ7, UDQM corresponds to DQ8–DQ15. L(U)DQM are considered same state when referenced as U(L)DQM.
BA0, BA1	input	Bank Address Input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. These pins also provide the op-code during a LOAD MODE REGISTER command

Name	Type	Description
A0 - A11	Input	Address Inputs: A0–A11 are sampled during the ACTIVE command (row- address A0–A11) and READ/WRITE command (column-address A0–A8; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (A10 LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
DQ[0:15]	I/O	Data Input/Output: Data bus
NC	-	No Connect: These pins are not connected to the die
V_{ddq}	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
V_{ssq}	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
V_{dd}	Supply	Power Supply: Voltage dependant on option.
V_{ss}	Supply	Ground.

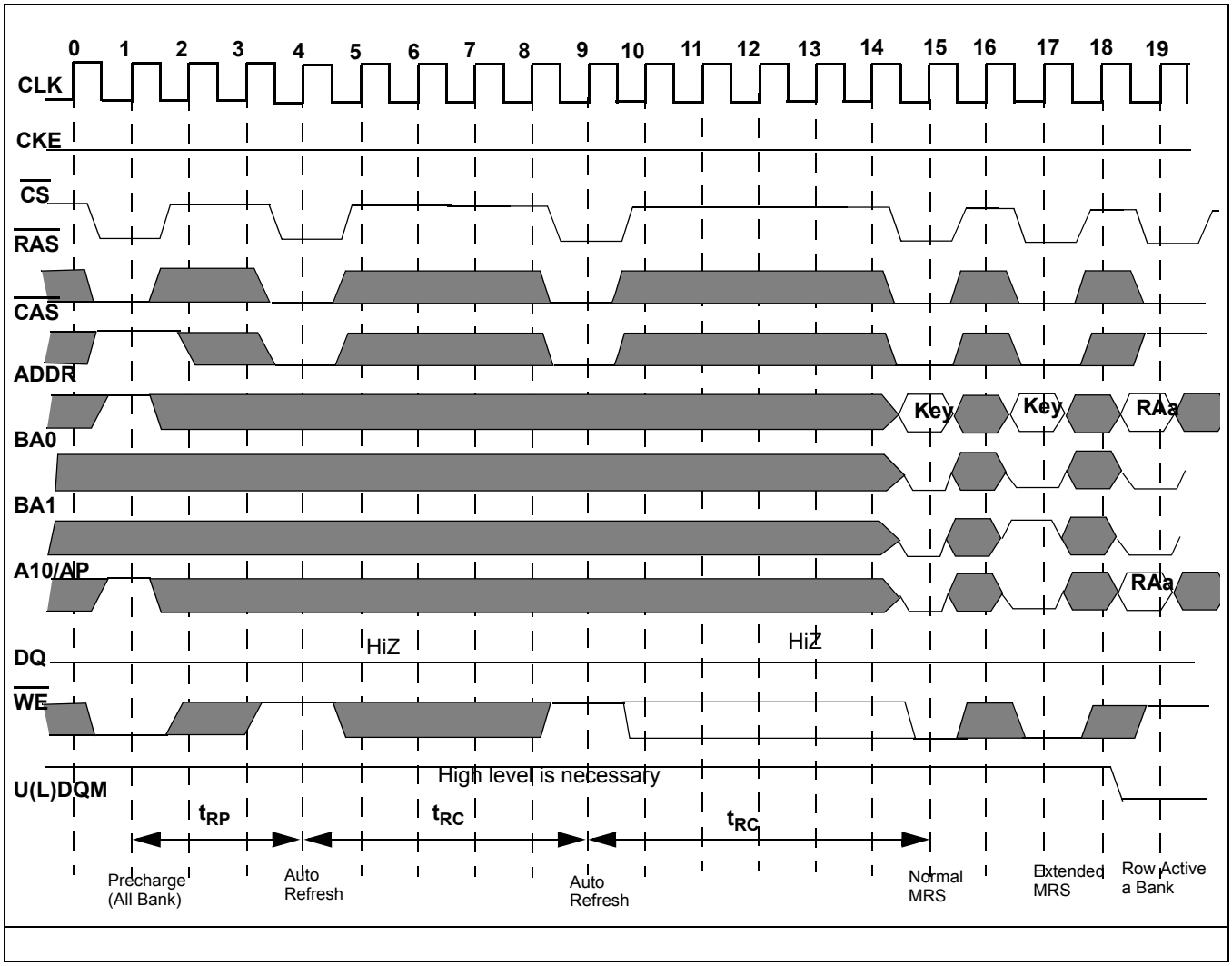
FUNCTIONAL DESCRIPTION

The Cypress 128Mb SDRAM is a quad-bank DRAM that operates at 1.8V and includes a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 33,554,432-bit banks is organized as 4,096 rows by 512 columns by 16 bits. Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0- A11 select the row). The address bits (A0-A8) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.The SDRAM must be initialized prior to normal operation. The following sections provide detailed information regarding device initialization, register definition,command descriptions and device operation.

Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to V_{DD} and V_{DDQ} (simultaneously) and the clock is stable (meets the clock specifications in the AC characteristics), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. The COMMAND INHIBIT or NOP should be applied atleast once during the 100µs delay. After the 100µs delay, a PRECHARGE command should be applied. All banks must then be precharged, thereby placing the device in the all banks idle state. Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.Refer Figure 1.

Figure 1. Initialize and Load Mode Register[2, 3, 4, 5]



Register Definition

There are two mode registers which contain settings to achieve low power consumption. The two registers : Mode Register (MR) and Extended Mode Register (EMR) are discussed below.

Mode Register(MR)

The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in Table 1.The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.Mode Register bits M0-M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4-M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the width burst mode , M10,M11,M12 and M13 should be set to zero.The mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

Notes:
2. The two AUTO REFRESH commands at Cycle 4 and Cycle 8 may be applied before either LOAD MODE REGISTER (LMR) command.
3. PRE = PRECHARGE command, LMR = LOAD MODE REGISTER command, AR = AUTO REFRESH command, ACT = ACTIVE command, RA = Row Address, BA = Bank Address
4. The Load Mode Register for both MR/EMR and 2 Auto Refresh commands can be in any order; However, all must occur prior to an Active command.
5. Apply Power and start clock, attempt to maintain CKE = “H”, DQM = “H“ 4 other pins are NOP condition at the Inputs.

Burst Length

Read and write accesses to the SDRAM are burst oriented.The burst length is programmable, as shown in Table 7.The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1,2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths. Reserved states should not be used, as unknown operation or incompatibility with future versions may result.When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected.All accesses for that burst take place within this block,meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A8 when the burst length is set to two; by A2-A8 when the burst length is set to four; and by A3-A8 when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

Burst Type

The burst type can be set to either Sequential or Interleaved by using the M3 bit in the Mode register.The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 7.

Table 1. Mode Register

M13- A1	M12- BA0	M11- A11	M10- A10	M9-A9	M8-A8	M7-A7	M6-A6	M5-A5	M4-A4	M3-A3	M2-A2	M1-A1	M0-A0
Reserved(Set to '0')				WB	Op Mode		CAS Latency			BT	Burst Length		

Table 2. MR - Burst Length Settings[6, 7, 8, 9, 10, 11]

M2 M1 M0	Burst Length	
	M3=0	M3=1
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full Page	Reserved

Table 3. MR - Burst Type Setting

M3	Burst Type
0	Sequential
1	Interleaved

Table 4. MR - CAS Latency Setting

M6 M5 M4	CAS Latency
0 0 0	Reserved
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	Reserved
1 0 1	Reserved
1 1 0	Reserved
1 1 1	Reserved

Table 5. MR - Width Burst Mode Setting

M9	Width Burst Mode
0	Prog. Burst Length
1	Single Mode Access

Table 6. MR - Operation Mode Setting

M8	M7	M6-M0	Operating Mode
0	0	Defined	Standard Operation
-	-	-	All other states reserved

Note:
6. For a burst length of two, A1-A7 select the block-of-two burst; A0 selects the starting column within the block.
7. For a burst length of four, A2-A7 select the block-of-four burst; A0-A1 select the starting column within the block.
8. For a burst length of eight, A3-A7 select the block-of-eight burst; A0-A2 select the starting column within the block.
9. For a full-page burst, the full row is selected and A0-A7 select the starting column.
10. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
11. For a burst length of one, A0-A7 select the unique column to be accessed,and mode register bit M3 is ignored.

Table 7. Burst Length Definition

Burst Length	Starting Column Address	Order of Accesses within a Burst	
		Type= Sequential	Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page(y)	n=A0-A11(location 0-y)	Bn,Bn+1,Bn+2....Bn,...	Not supported

Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to one, two, or three clocks. If a READ command is registered at clock edge ***r***, and the latency is ***q*** clocks, the data will be available by clock edge ***r + q***. The DQs will start driving as a result of the clock edge one cycle earlier **(*r + q*- 1)**, and provided that

the relevant access times are met, the data will be valid by clock edge ***r + q***. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in Figure 2. Table 8. indicates the operating frequencies at which each CAS latency setting can be used. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

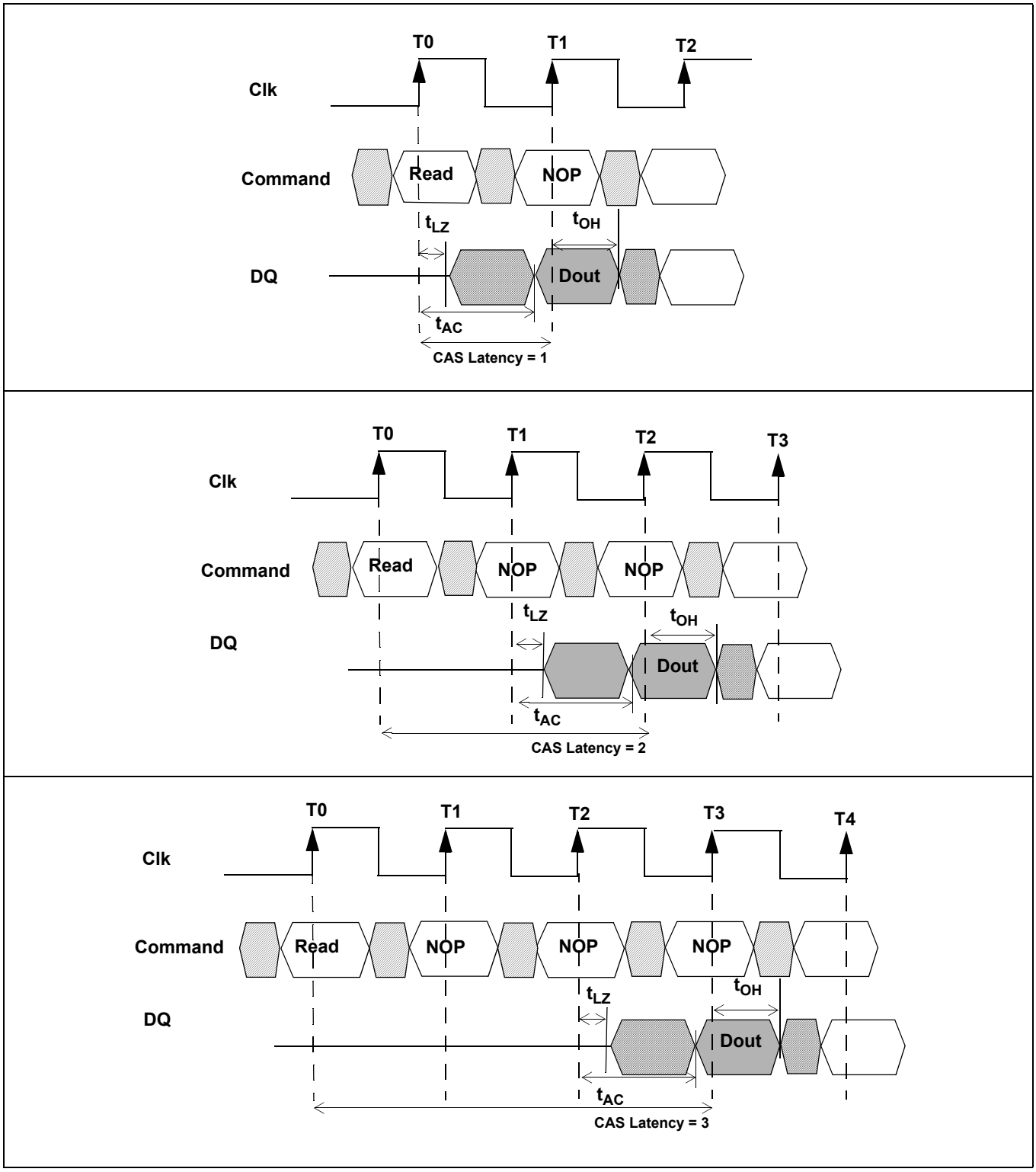


Figure 2. CAS Latency

Table 8. CAS Latency

Speed Bin	Allowable Operating Frequency(Mhz)		
	CAS Latency =1	CAS Latency =2	CAS Latency =3
100Mhz	<=40	<=100	Not Supported

EXTENDED MODE REGISTER (EMR)

The Extended Mode Register controls additional functions such as the Temperature Compensated Self Refresh (TCSR) Control, and Partial Array Self Refresh (PASR).The Extended Mode Register is programmed via the Mode Register Set command (BA1=1,BA0=0) and retains the stored information until it is programmed again or the device loses power. The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time before before initiating any subsequent operation. Violating either of these requirements results in unspecified operation.

TEMPERATURE COMPENSATED SELF REFRESH

Every cell in the DRAM requires refreshing due to the capacitor losing its charge over time. The refresh rate is dependent on temperature. At higher temperatures a capacitor loses charge quicker than at lower temperatures, requiring the cells to be refreshed more often.Temperature Compensated Self Refresh (TCSR) allows the controller to program the Refresh interval during SELF REFRESH mode, according to the case temperature of the device. This allows great power savings during SELF REFRESH during most operating temperature ranges. Only during extreme temperatures would the controller have to select a TCSR level that will guarantee data during SELF REFRESH. Historically, during Self Refresh, the refresh rate has been set to accomodate the worst case, or highest temperature range expected. Thus, during ambient temperatures, the power consumed during refresh was unnecessarily high, because the refresh rate was set to accommodate the higher temperatures. Setting EM4 and EM3, allow the DRAM to accomodate more specific temperature regions during SELF REFRESH. There are four temperature settings, which will vary the SELF REFRESH current according to the selected temperature. This selectable refresh rate will save power when the DRAM is operating at normal temperatures. Cypress 128Mb SDRAMs will also have a Auto Temperature Self Refresh which will automatically adjust the refresh rate based on the temperature without any register update needed.

PARTIAL ARRAY SELF REFRESH

The Partial Array Self Refresh (PASR) feature allows the controller to select the amount of memory that will be refreshed during SELF REFRESH. The refresh options are all banks (banks 0, 1, 2, and 3); two banks(banks 0 and 1); and one bank (bank 0). WRITE and READ commands occur to any bank selected during standard operation, but only the selected banks in PASR will be refreshed during SELF REFRESH. The data in banks 2 and 3 will be lost when the two bank option is used. Similarly the data will be lost in banks 1, 2, and 3 when the one bank option is used.

SLEW RATE CONTROL

The Slew rate feature allows one to reduce the drive strength of the I/O's on the device during low frequency operation. This allows systems to reduce the noise associated with the I/O's switching.

Table 9. Extended Mode Register

EM13-BA1	EM12-BA0	EM11-A11	EM10-A10	EM9-A9	EM8-A8	EM7-A7	EM6-A6	M5-A5	EM4-A4	EM3-A3	EM2-A2	EM1-A1	EM0- A0
1	0	All must be set to '0'				Bank Up/Down	Slew Rate		TCSR		PCSR		

Table 10.EMRS - Partial Array Self Refresh Selection[12]

EM7- A7	EM2 - A2	EM1 - A1	EM0 - A0	Self Refresh Coverage
X	0	0	0	Four Banks
0	0	0	1	Two Banks(Bank0,1)
0	0	1	0	One Bank(Bank0)
1	0	0	1	Two Banks(Bank2,3)
1	0	1	0	One Bank(Bank2)
X	0	1	1	RFU
X	1	0	0	RFU
X	1	0	1	RFU
X	1	1	0	RFU
X	1	1	1	RFU

Note:
12. RFU: Reserved for Future Use

Table 11.EMRS - Case Temperature

EM4 - A4	EM3 - A3	Maximum Case Temperature
1	1	85°C
0	0	70°C
0	1	45°C
1	0	15°C

Table 12.EMRS - Slew Rate Control

EM6 - A6	EM5 - A5	Slew Rate
0	0	100%
0	1	75%
1	0	50%
1	1	30%

Table 13.Commands[13, 14, 15, 16, 17, 18, 19, 20]

Name(Function)	CS	RAS	CAS	WE	U(L)DQM	ADDR	DQ
COMMAND INHIBIT(NOP)	H	X	X	X	X	X	X
NO OPERATION(NOP)	L	H	H	H	X	X	X
ACTIVE(Select bank and activate row)	L	L	H	H	X	Bank/ Row	X
READ(Select bank and column, and start READ burst)[20]	L	H	L	H	L/H	Bank/ Col	X
WRITE(Select bank and column, and start WRITE burst)[20]	L	H	L	L	L/H	Bank/ Col	Valid
BURST TERMINATE	L	H	H	L	X	X	Active
PRECHARGE(Deactivate row in bank or banks)	L	L	H	L	X	Code	X
AUTO REFRESH or SELF REFRESH(Enter Self Refresh Mode)	L	L	L	H	X	X	X
LOAD MODE REGISTER	L	L	L	L	X	Opcode	X
Write Enable/Output Enable	-	-	-	-	L	-	Active
Write Inhibit/OUtput High-Z	-	-	-	-	H		High Z

Note:
13. CKE is HIGH for all commands shown except SELF REFRESH.
14. A0-A10 define the op-code written to the mode register.
15. A0-A11 provide row address, and BA0, BA1 determine which bank is made active.
16. A0-A8 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which bank is being read from or written to.
17. A10 LOW: BA0, BA1 determine the bank being precharged. A10 HIGH: All banks precharged and BA0, BA1 are “Don’t Care.”
18. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
19. Internal refresh counter controls row addressing; all inputs and I/Os are “Don’t Care” except for CKE.
20. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay). LDQM controls DQ0-7, UDQM controls DQ8-15, DQM2 controls DQ16-23, and DQM3 controls DQ24-31.

Cycle to Cycle Commands

Table 14.CKE[21, 23, 24]

CKE_{n-1}	CKE_n	Current State	$Command_n$	$Action_n$
L	L	Power Down	X	Maintain Power Down
		Self Refresh	X	Maintain Self Refresh
		Clock Suspend	X	Maintain Clock Suspend
L	H	Power Down[25]	Command Inhibit or NOP	Exit Power Down
		Self Refresh[26]	Command Inhibit or NOP	Exit Self Refresh
		Clock Suspend[27]	X	Exit Clock Suspend
H	L	All Banks Idle	Command Inhibit or NOP	Power Down Entry
		All Banks Idle	Auto Refresh	Self Refresh Entry
		Reading or Writing	Valid	Clock Suspend Entry
H	H		See Table 15.	

Notes:
21. CKE_n is the logic state of CKE at clock edge n; CKE_{n-1} was the state of CKE at the previous clock edge.
22. Current State is the state of the SDRAM immediatly prior to the clock edge n.
23. $Command_n$ is the command registered at clock edge n , and $Action_n$ is a result of Command $_n$.
24. All states and sequences not shown are illegal or reserved.
25. Exiting power down at clock edge n will put the device in all the banks idle state in time for clock edge n+1(provided the t_{CKS} is met)
26. Exiting self refresh at clock edge n will put the device in all the banks idle state once t_{XSR} is met. Command Inhibit or NOP commands should be issued on any clock edges occuring during the t_{XSR} period. A minimum of two NOP commands must be provided during the t_{XSR} period.
27. After exiting clock suspend at clock edge n, the device will resume operation and recognize the next command at clock edge n+1.

Table 15.Curent State Bank n, Command to Bank n[28, 29, 30, 31, 32, 33]

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command(Action)
Any	H	X	X	X	COMMAND INHIBIT (NOP/Continue previous operation)
	L	H	H	H	NO OPERATION (NOP/Continue previous operation)
Idle	L	L	H	H	ACTIVE (Select and activate row)
	L	L	L	H	AUTO REFRESH[34]
	L	L	L	L	LOAD MODE REGISTER[34]
	L	L	H	L	PRECHARGE[38]
Row Active	L	H	L	H	READ (Select column and start READ burst)[37]
	L	H	L	L	WRITE (Select column and start WRITE burst)[37]
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)[35]
Read(Auto Precharge Disabled)	L	H	L	H	READ (Select column and start new READ burst)[37]
	L	H	L	L	WRITE (Select column and start WRITE burst)[37]
	L	L	H	L	PRECHARGE (Truncate READ burst, start PRECHARGE)[35]
	L	H	H	L	BURST TERMINATE[36]
Write (Auto Precharge Disabled)	L	H	L	H	READ (Select column and start READ burst)[37]
	L	H	L	L	WRITE (Select column and start new WRITE burst)[37]
	L	L	H	L	PRECHARGE (Truncate WRITE burst, start PRECHARGE)[35]
	L	H	H	L	BURST TERMINATE[36]

Notes:

28. This table applies when CKEn-1 was HIGH and CKEn is HIGH (see Table 14.) and after t_{XSR} has been met (if the previous state was self refresh).
29. This table is bank-specific, except where noted; i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state. Exceptions are covered in the notes below.
30. Current state definitions: Idle: The bank has been precharged, and t_{RP} has been met.Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress. Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated. Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated.
31. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and Table 15. and according to Table 16.. Precharging: Starts with registration of a PRECHARGE command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state. Row Activating: Starts with registration of an ACTIVE command and ends when tRCD is met. Once t_{RCD} is met, the bank will be in the row active state. Read w/Auto Precharge Enabled: Starts with registration of a READ command with auto precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state. Write w/Auto Precharge Enabled: Starts with registration of a WRITE command with auto precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.
32. The following states must not be interrupted by any executable command; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states. Refreshing: Starts with registration of an AUTO REFRESH command and ends when t_{RC} is met. Once t_{RC} is met, the SDRAM will be in the all banks idle state. Accessing Mode Register: Starts with registration of a LOAD MODE REGISTER command and ends when t_{MRD} has been met. Once t_{MRD} is met, the SDRAM will be in the all banks idle state. Precharging All: Starts with registration of a PRECHARGE ALL command and ends when tRP is met. Once t_{RP} is met, all banks will be in the idle state.
33. All states and sequences not shown are illegal or reserved.
34. Not bank-specific; requires that all banks are idle.
35. May or may not be bank-specific; if all banks are to be precharged, all must be in a valid state for precharging.
36. Not bank-specific; BURST TERMINATE affects the most recent READ or WRITE burst, regardless of bank.
37. READs or WRITEs listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
38. Does not affect the state of the bank and acts as a NOP to that bank.

Table 16.Current State Bank n,Command to Bank m[39, 40, 41, 42, 43, 44]

Current State	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Command(Action)
Any	H	X	X	X	COMMAND INHIBIT (NOP/Continue previous operation)
	L	H	H	H	NO OPERATION (NOP/Continue previous operation)
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE (Select and activate row)
	L	H	L	H	READ (Select column and start READ burst)[45]
	L	H	L	L	WRITE (Select column and start WRITE burst)[45]
	L	L	H	L	PRECHARGE

Table 16.Current State Bank n,Command to Bank m[39, 40, 41, 42, 43, 44]

Read(Auto Precharge Disabled)	L	L	H	H	ACTIVE (Select and activate row)
	L	H	L	H	READ (Select column and start new READ burst)[45, 48]
	L	H	L	L	WRITE (Select column and start WRITE burst)[45, 51, 49]
	L	L	H	L	PRECHARGE[47]
Write(Auto PRecharge Disabled)	L	L	H	H	ACTIVE (Select and activate row)
	L	H	L	H	READ (Select column and start READ burst)[45, 46, 50]
	L	H	L	L	WRITE (Select column and start new WRITE burst)[45, 51]
	L	L	H	L	PRECHARGE[47]
Read (With Auto Precharge)	L	L	H	L	ACTIVE (Select and activate row)
	L	H	L	H	READ (Select column and start new READ burst)[45, 46, 52]
	L	H	L	L	WRITE (Select column and start WRITE burst)[45, 46, 54]
	L	L	H	L	PRECHARGE[47]
Write(With Auto Precharge)	L	L	H	H	ACTIVE (Select and activate row)
	L	H	L	H	READ (Select column and start READ burst)[45, 46, 53]
	L	H	L	L	WRITE (Select column and start new WRITE burst)[45, 46, 55]
	L	L	H	L	PRECHARGE[47]

Note:
39. This table applies when CKEn-1 was HIGH and CKEn is HIGH and after t_{XSR} has been met (if the previous state was self refresh).
40. This table describes alternate bank operation, except where noted; i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m* (assuming that bank *m* is in such a state that the given command is allowable). Exceptions are covered in the notes below.
41. Current state definitions: Idle: The bank has been precharged, and t_{RP} has been met. Row Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress. Read: A READ burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated. Write: A WRITE burst has been initiated, with auto precharge disabled, and has not yet terminated or been terminated. Read w/Auto Precharge Enabled: Starts with registration of a READ command with auto precharge enabled, and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state. Write w/Auto Precharge Enabled: Starts with registration of a WRITE command with auto precharge enabled, and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.
42. AUTO REFRESH, SELF REFRESH and LOAD MODE REGISTER commands may only be issued when all banks are idle.
43. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
44. All states and sequences not shown are illegal or reserved.
45. READs or WRITEs to bank *m* listed in the Command (Action) column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
46. CONCURRENT AUTO PRECHARGE: Bank *n* will initiate the auto precharge command when its burst has been interrupted by bank *m*'s burst.
47. Burst in bank *n* continues as initiated.
48. For a READ without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CAS latency later (Figure 34.).
49. For a READ without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered (Figure 35.). U(L)DQM should be used one clock prior to the WRITE command to prevent bus contention.
50. For a WRITE without auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered (Figure 36.), with the data-out appearing CAS latency later. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
51. For a WRITE without auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the WRITE on bank *n* when registered (Figure 37.). The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m*.
52. For a READ with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the READ on bank *n*, CAS latency later. The PRECHARGE to bank *n* will begin when the READ to bank *m* is registered (Figure 34.)
53. For a READ with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the READ on bank *n* when registered. U(L)DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank *n* will begin when the WRITE to bank *m* is registered (Figure 35.).
54. For a WRITE with auto precharge interrupted by a READ (with or without auto precharge), the READ to bank *m* will interrupt the WRITE on bank *n* when registered, with the data-out appearing CAS latency later. The PRECHARGE to bank *n* will begin after t_{WR} is met, where t_{WR} begins when the READ to bank *m* is registered. The last valid WRITE to bank *n* will be data-in registered one clock prior to the READ to bank *m* (Figure 36.).
55. For a WRITE with auto precharge interrupted by a WRITE (with or without auto precharge), the WRITE to bank *m* will interrupt the WRITE on bank *n* when registered. The PRECHARGE to bank *n* will begin after t_{WR} is met, where t_{WR} begins when the WRITE to bank *m* is registered. The last valid WRITE to bank *n* will be data registered one clock prior to the WRITE to bank *m* (Figure 37.).

Command Operation

Extended Mode register set command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0 = Low, BA1 = High)

The LPSDRAM has an extended mode register that defines low power functions. In this command, A0 through A11 are the data input pins.After power on, the extended mode register set command must be executed to fix low power functions.The extended mode register can be set only when all banks are in idle state.During tRSC following this command, the LPSDRAM can not accept any other commands.

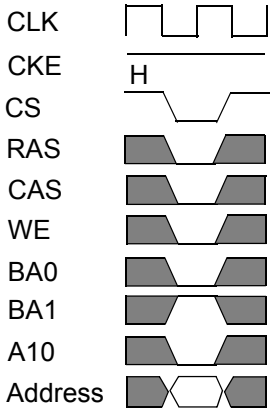


Figure 3. EMRS Set Command

Mode register set command (LOAD MODE REGISTER COMMAND) (CS, RAS, CAS, WE, BA0, BA1=Low)

The LPSDRAM has a mode register that defines how the device operates. In this command, A0 through A11 are the data input pins.

After power on, the mode register set command must be executed to initialize the device. The mode register can be set only when the banks are in the idle state. During t_{RSC} following this command, the LPSDRAM cannot accept any other commands.

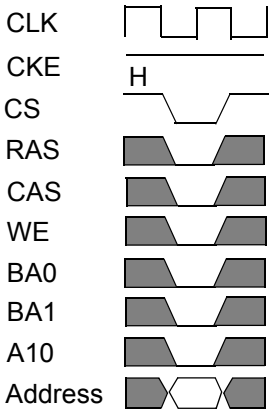


Figure 4. MR Set Command

Activate Command ($\overline{CS}$, $\overline{RAS}$=Low, $\overline{CAS}$, $\overline{WE}$=HIgh)

The LPSDRAM has four banks, each with 4,096 rows. This command activates the bank selected by BA0 and BA1 and a row address selected by A0 through A11. This row remains active for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

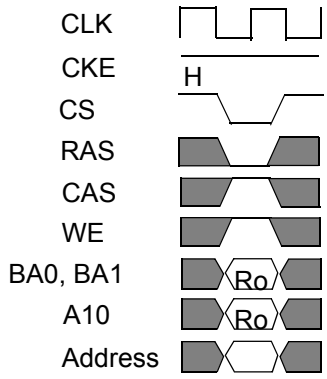


Figure 5. Activate Command

Precharge command ($\overline{CS}$, $\overline{RAS}$, $\overline{WE}$, BA0, BA1=Low, $\overline{CAS}$ = High)

The PRECHARGE command is used to deactivate the active row in a particular bank or the active row in all banks. The bank(s) will be available for a subsequent row access a specified time (t_{RP}) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. Otherwise BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. This command corresponds to a conventional DRAM’s $\overline{RAS}$ rising.

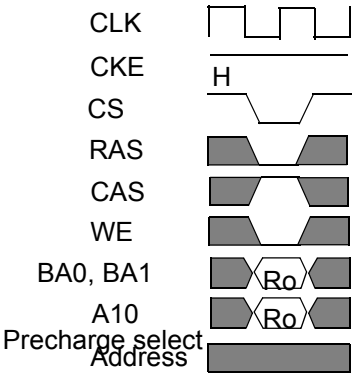


Figure 6. Precharge Command

Write command ($\overline{CS}$, $\overline{CAS}$, $\overline{WE}$=Low, $\overline{RAS}$=High)

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A7 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst. If auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the U(L)DQM input logic level appearing coincident with the data. If a given U(L)DQM signal is registered LOW, the corresponding data will be written to memory; if the U(L)DQM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

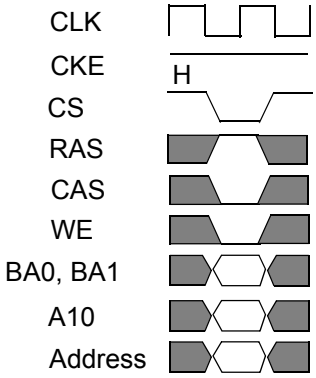


Figure 7. Write Command

Read command ($\overline{CS}$, $\overline{CAS}$=Low, $\overline{RAS}$, $\overline{WE}$=High)

READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0-A8 selects the starting column location. The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst. If auto precharge is not selected, the row will remain open for subsequent accesses. Read data appears on the DQs subject to the logic level on the U(L)DQM inputs two clocks earlier. If a given U(L)DQM signal was registered HIGH, the corresponding DQs will be High-Z two clocks later; if the U(L)DQM signal was registered LOW, the DQs will provide valid data.

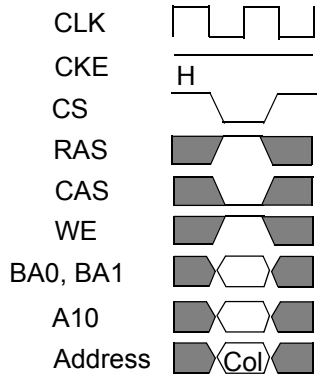


Figure 8. Read Command

Auto refresh command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$=Low, $\overline{WE}$, CKE=High)

AUTO REFRESH is used during normal operation of the SDRAM. This command is nonpersistent, so it must be issued each time a refresh is required. All active banks must be PRECHARGED prior to issuing an AUTO REFRESH command. The AUTO REFRESH command should not be issued until the minimum t_{RP} has been met after the PRECHARGE command. The addressing is generated by the internal refresh controller. The address bits thus are a “Don’t Care” during an AUTO REFRESH command. The Cypress 128Mb SDRAM requires 4,096 AUTO REFRESH cycles every 64ms (t_{REF}), regardless of width option. Providing a distributed AUTO REFRESH command every 15.625µs will meet the refresh requirement and ensure that each row is refreshed. Alternatively, 4,096 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (t_{RFC}), once every 64ms

Before executing Auto refresh, all banks must be precharged. After this cycle, all banks will be in the idle (precharged) state and ready for a row activate command. During tRC1 period (from refresh command to refresh or activate command), the LPSDRAM cannot accpet any other command.

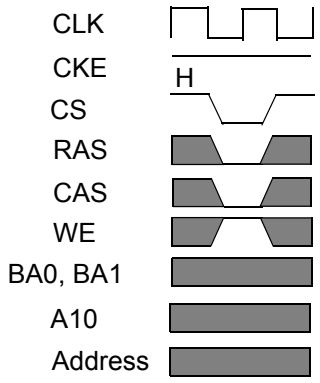


Figure 9. Auto Refresh Command

Self refresh entry command (CS, RAS, CAS, CKE=Low, WE=High)

The SELF REFRESH command can be used to retain data in the SDRAM(without external clocking), even if the rest of the system is powered down. The SELF REFRESH command is initiated like an AUTO REFRESH command except CKE is disabled (LOW). Once the SELF REFRESH command is registered, all the inputs to the SDRAM become “Don’t Care” with the exception of CKE, which must remain LOW.Once self refresh mode is engaged, the SDRAM provides its own internal clocking, causing it to perform its own AUTO REFRESH cycles. The SDRAM must remain in self refresh mode for a minimum period equal to t_{RAS} and may remain in self refresh mode for an indefinite period beyond that.The procedure for exiting self refresh requires a sequence of commands. First, CLK must be stable (meet the clock specifications in the AC characteristics) prior to CKE going back HIGH. Once CKE is HIGH, the SDRAM must have NOP commands issued (a minimum of two clocks) for t_{XSR} because time is required for the completion of any internal refresh in progress. Upon exiting the self refresh mode, AUTO REFRESH commands must be issued every 15.625µs or less as both SELF REFRESH and AUTO REFRESH utilize the row refresh counter.

After the command execution, self refresh operation continues while CKE remains low. When CKE goes high, the LPSDRAM exits the self refresh mode. During self refresh mode, refresh interval and refresh operation are performed internally, so there is no need for external control. Before executing self refresh, all banks must be precharged.

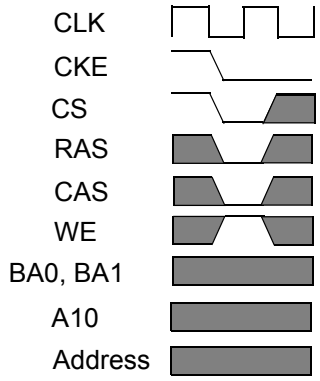


Figure 10. Self Refresh Entry Command

Power down entry command (CS, CKE=Low, RAS, CAS, WE=High)

After the command execution, power down mode continues while CKE remains low. When CKE goes high, the LPSDRAM exits the power down mode. Before executing power down, all banks must be precharged.

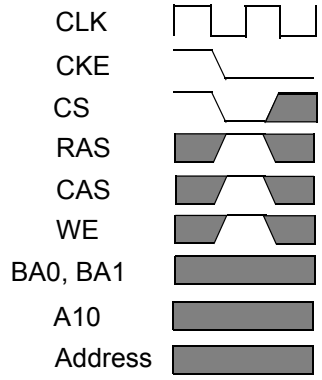


Figure 11. Power Down Entry Command

Deep power down entry command (CS, CKE, WE=Low, RAS, CAS=High)

After the command execution, deep power down mode continues while CKE remains low. WHen CKE goes high, the LPSDRAM exits the deep power down mode. Before executing deep power down, all banks must be precharged.

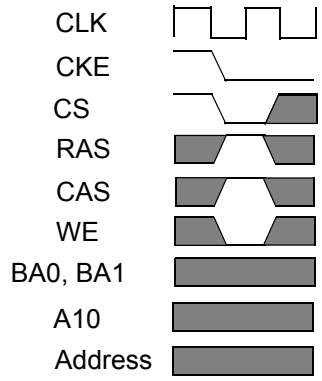


Figure 12. Deep Power Down Entry Command

Burst stop command(Burst Terminate) (CS=WE=Low, RAS, CAS=High)

This command can stop the current burst operation.The BURST TERMINATE command is used to truncate either fixed-length or full-page bursts. The most recently registered READ or WRITE command prior to the BURST TERMINATE command will be truncated.

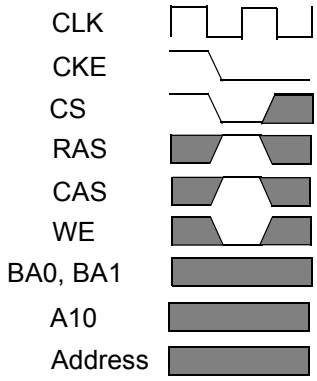


Figure 13. Burst Stop Command

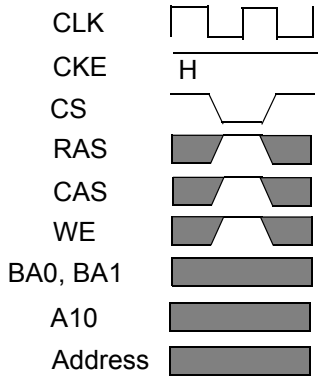


Figure 14. No Operation

No operation (Command Inhibit) ($\overline{CS}$=Low, $\overline{RAS}$, $\overline{CAS}$, WE=High)

The NO OPERATION (NOP) command is used to perform a NOP to an SDRAM which is selected ($\overline{CS}$ is LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.This command is not an execution command. No operations begin or terminate by this command.

AUTO PRECHARGE

AUTO PRECHARGE is accomplished by using A10 to enable auto precharge in conjunction with a specific READ or WRITE command. AUTO PRECHARGE thus performs the same PRECHARGE command , without requiring an explicit command. A PRECHARGE of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. AUTO PRECHARGE does not apply in the full page mode burst. Auto precharge is nonpersistent in that it is either enabled or disabled for each individual READ or WRITE command.

Auto precharge ensures that the precharge is initiated at the earliest valid stage within a burst. The user must not issue another command to the same bank until the precharge time (t_{RP}) is completed.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–40°C to +85°C

Supply Voltage to Ground Potential ..... –0.4V to 4.6V

DC Voltage Applied to Outputs in High-Z State[56, 57, 58].....–0.4V to 3.3V

DC Input Voltage[56, 57, 58].....–0.4V to 3.3V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current .....> 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{DD}	V_{DDQ}
CYL008M162FFBU	Industrial	–40°C to +85°C	1.7V to 1.95V	1.7V to V_{DD}

DC Electrical Characteristics and Operating Conditions

Parameter / Condition	Symbol	Min	Max	Units
Supply Voltage	Vdd(1.8V)	1.7	1.95	V
I/O Supply Voltage	Vddq(1.8V)	1.7	Vdd	V
Input High Voltage : Logic 1 All Inputs[61]	Vih	0.8*Vddq	Vddq+0.3	V
Input Low Voltage : Logic 0 All Inputs[61]	Vil	-0.3	0.3	V
Data Output High Voltage : Ioh = -0.1mA	Voh	0.9*Vddq		V
Data Output Low Voltage : Iol = 0.1mA	Vol		0.2	V
Input Leakage Current: Any Input 0V = V_{IN} = V_{DD} (All other pins not under test = 0V)	Iil	-5	5	µA
Output Leakage Current: DQs are disabled; 0V = V_{OUT} = V_{DD}q	Ioz	-5	5	µA

Table 17.AC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS[59, 63]

Parameter / Condition	Symbol	Min	Max	Units
Input High Voltage: Logic 1; All Inputs	Vih	1.4		V
Input Low Voltage: Logic 0 ; All Inputs	Vil		0.4	V

Table 18.Idd Specifications and Conditions[59, 61, 64, 65]

Description	Parameter	Description	Max	Units
Operating Current (One bank Active)	Idd1	Operating Current: Active Mode; Burst =2 ; Read or Write ; tRC=tRC(min); CAS Latency =3[64, 65, 67]	60	mA
Precharge Standby Current in Power down mode	Idd2p	Standby Current : Power Down Mode : CKE=LOW; All banks Idle	250	µA
Precharge Standby Current in non Power down mode	Idd2n	Standby Current : Power Down Mode : CKE=HIGH; All banks Idle	10	mA

Notes:

56. $V_{IH(MAX)}$ = V_{CC} + 0.5V for pulse durations less than 20ns.
57. $V_{IL(MIN)}$ = -0.5V for pulse durations less than 20ns
58. Overshoot and undershoot specifications are characterized and are not 100% tested.
59. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. (VDD and VDDQ must be powered up simultaneously. VSS and VSSQ must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the tREF refresh requirement is exceeded.
60. All states and sequences not shown are illegal or reserved.
61. In addition to meeting the transition rate specification, the clock and CKE must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
62. t_{HZ} defines the time at which the output achieves the open circuit condition; it is not a reference to VOH or VOL. The last valid data element will meet t_{OH} before going High-Z.
63. AC timing and IDD tests have VIL and VIH, with timing referenced to VIH/2 = crossover point. If the input transition time is longer than t_T (MAX), then the timing is referenced at VIL (MAX) and VIH (MIN) and no longer at the VIH/2 crossover point.
64. IDD specifications are tested after the device is properly initialized.
65. IDD is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
66. The IDD current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
67. Address transitions average one transition every two clocks.

Table 18.Idd Specifications and Conditions[59, 61, 64, 65]

Active Standby Current in Power down mode	Idd3p	Standby Current:Active Mode; $\overline{CS}$=HIGH; CKE=LOW;All banks active after tRCD met; No access in progress[66, 68, 69]	2	mA
Active Standby Current in non Power down mode (One Bank Active)	Idd3n	Standby Current:Active Mode; $\overline{CS}$=HIGH; CKE=HIGH;All banks active after tRCD met; No access in progress[67, 69]	20	mA
Operating Current (Burst Mode)	Idd4	Operating Current : Burst Mode: Continous Burst ; Read or Write : All banks Active; Vdd = 1.8V CAS Latency =3[66, 67, 68, 69]	50	mA
Refresh Current	Idd5	Auto Refresh Current : t_{RC}=$t_{RC(min)}$) CAS Latency=3;CKE,$\overline{CS}$=HIGH[68, 69]	120	mA
Self-Refresh Current	Idd6(Vdd = 1.8V)	Self Refresh Current: CKE <= 0.2V, 4 Banks	150	µA
		Self Refresh Current: CKE <= 0.2V, 2 Banks	115	µA
		Self Refresh Current: CKE <= 0.2V, 1 Bank	95	µA
Deep Power Down Current	Idd7	Deep power down	10	µA

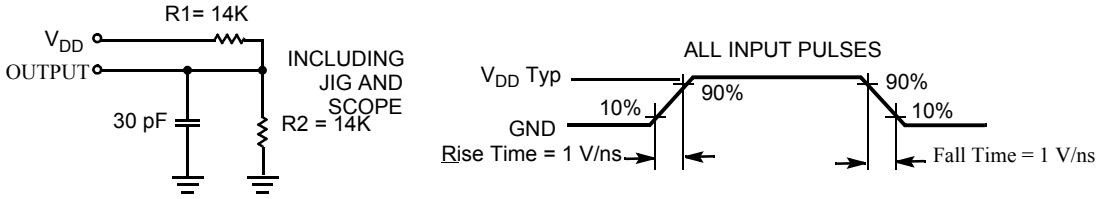
Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, $V_{DD(typ)}$	4	pF
C_{OUT}	Output Capacitance		6	pF

Thermal Resistance[70]

Parameter	Description	Test Conditions	FBGA	Unit
θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	TBD	°C/W
θ_{JC}	Thermal Resistance (Junction to Case)		TBD	°C/W

AC Test Loads and Waveforms



Notes:
68. Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid VIH or VIL levels.
69. CKE is HIGH during refresh command period t_{RFC} (MIN) else CKE is LOW. The IDD6 limit is actually a nominal value and does not result in a fail value
70. Tested initially and after design or process changes that may affect these parameters.

AC Characteristics

AC CHARACTERISTICS		Symbol	100MHz		Units
Parameter			Min	Max	
Clock Specifications					
Clock Frequency		t_{CLK}		100	Mhz
Clock Period[71]		t_{CLKS}	10		ns
Clock High Time		t_{CKH}	3		ns
Clock Low Time		t_{CKL}	3		ns
Synchronous timing Specifications					
Input Setup Time to Clock		t_{CSS}	2.0		ns
Input Hold time to Clock		t_{CSH}	1.0		ns
Clock Access Time[38]	CL=3	$t_{AC}(3)$			ns
	CL=2	$t_{AC}(2)$		8	ns
	CL=1	$t_{AC}(1)$		22	ns
Output hold time from Clock		t_{COH}	2.5		ns
Data High Impedance Time[62]	CL=3	$t_{HZ}(3)$			ns
	CL=2	$t_{HZ}(2)$		8	ns
	CL=1	$t_{HZ}(1)$		20	ns
Active to Precharge Command		t_{RAS}	60	120000	ns
Active to Active Command Period		t_{RC}	80		ns
Active to Read or Write Delay		t_{RCD}	20		ns
Refresh Period(4096 rows)		t_{REF}		64	ms
Auto Refresh Period		t_{RFC}	70		ns
Precharge Command Period		t_{RP}	20		ns
Active Banka to Active Bankb Command		t_{RRD}	20		ns
Transition Time[72]		t_T	0.5	1.2	ns
Write Recovery Time[73]		t_{WR}	2		t_{CK}
Write Recovery Time[74]		t_{WR}	2		t_{CK}
Exit Self Refresh to Active Command[75]		t_{XSR}	80		ns
READ/WRITE command to READ/WRITE command[76]		t_{CCD}	1		t_{CK}
CKE to clock disable or power-down entry mode[77]		t_{CKED}	1		t_{CK}
CKE to clock enable or power-down exit setup mode[77]		t_{PED}	1		t_{CK}
U(L)DQM to input data delay[76]		t_{DQD}	0		t_{CK}
U(L)DQM to data mask during WRITEs[76]		t_{DQM}	0		t_{CK}
U(L)DQM to data high-impedance during READs[76]		t_{DQZ}	2		t_{CK}
WRITE command to input data delay[76]		t_{DWD}	0		t_{CK}

Note:

71. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including t_{WR}, and PRECHARGE commands). CKE may be used to reduce the data rate.
72. AC characteristics assume t_T = 1ns.
73. Auto precharge mode only. The precharge timing budget (t_{RP}) begins at 10ns for -100Mhz after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode.
74. Precharge mode only.
75. CLK must be toggled a minimum of two times during this period.
76. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
77. Timing actually specified by t_{CKS}; clock(s) specified as a reference only at minimum cycle rate.
78. Timing actually specified by t_{WR} plus t_{RP}; clock(s) specified as a reference only at minimum cycle rate.
79. Timing actually specified by t_{WR}.
80. JEDEC and PC100 specify three clocks.

AC Characteristics

Data-in to ACTIVE command[78]		t_{DAL}	5		t_{CK}
Data-in to PRECHARGE command[79]		t_{DPL}	2		t_{CK}
Last data-in to burst STOP command[76]		t_{BDL}	1		t_{CK}
Last data-in to new READ/WRITE command[76]		t_{CDL}	1		t_{CK}
Last data-in to PRECHARGE command[79]		t_{RDL}	2		t_{CK}
LOAD MODE REGISTER command to ACTIVE or REFRESH command[80]		t_{MRD}	2		t_{CK}
Data-out to high-impedance from PRECHARGE command[76]	CL=3	$t_{ROH}(3)$			t_{CK}
	CL=2	$t_{ROH}(2)$	2		t_{CK}
	CL=1	$t_{ROH}(1)$	1		t_{CK}

Device Operation

BANK/ROW ACTIVATION

Before any READ or WRITE commands can be issued to a bank within the SDRAM, a row in that bank must be “opened”(activated). This is accomplished via the ACTIVE command,which selects both the bank and the row to be activated. A READ or WRITE command may then be issued to that row, subject to the t_{RCD} specification. t_{RCD} (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a t_{RCD} specification of 20ns with a 100 MHz clock (10ns period) results in 2.5 clocks. A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been “closed” (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by t_{RC}. A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by t_{RRD}.

READ Operation

READ bursts are initiated with a READ command, as shown in Figure 15. The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. For the generic READ commands used in the following illustrations, auto precharge is disabled. During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid by the next positive clock edge. Figure 2. shows general timing for each possible CAS latency setting.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A fullpage burst will continue until terminated. (The burst will wrap around at the end of the page). A continuous flow of data can be maintained by having addtional Read Burst or single Read Command. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst that is being truncated. The new READ command should be issued ***x*** cycles before the clock

edge at which the last desired data element is valid, where ***x*** equals the CAS latency minus one.

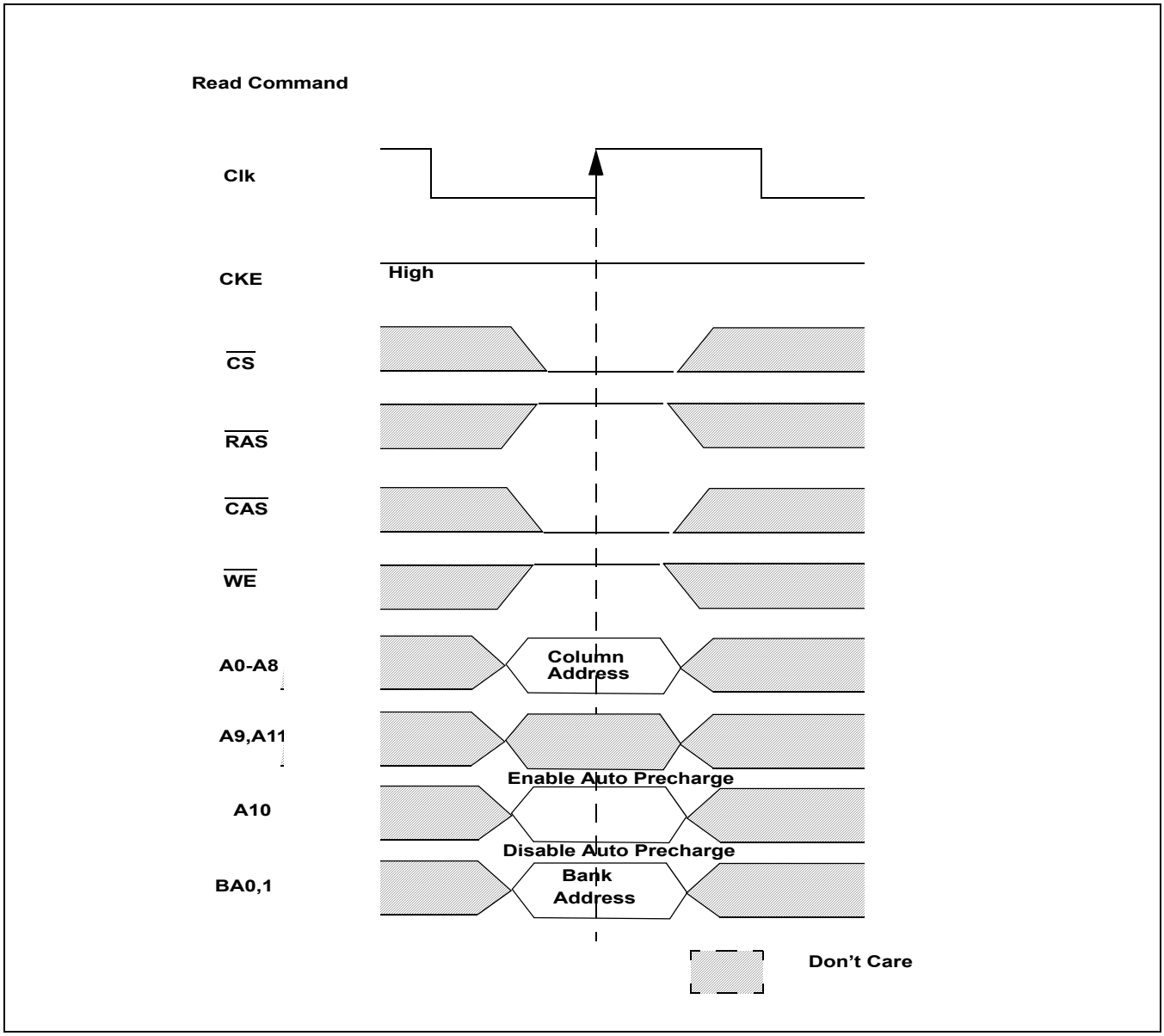


Figure 15. Read Command

This is shown in Figure 16.for CAS latencies of one, two and three; data element *n* + 3 is either the last of a burst of four or the last desired of a longer burst. Full-speed random read accesses can be performed to the same bank, as shown in Figure 17., or each subsequent READ may be performed to a different bank.

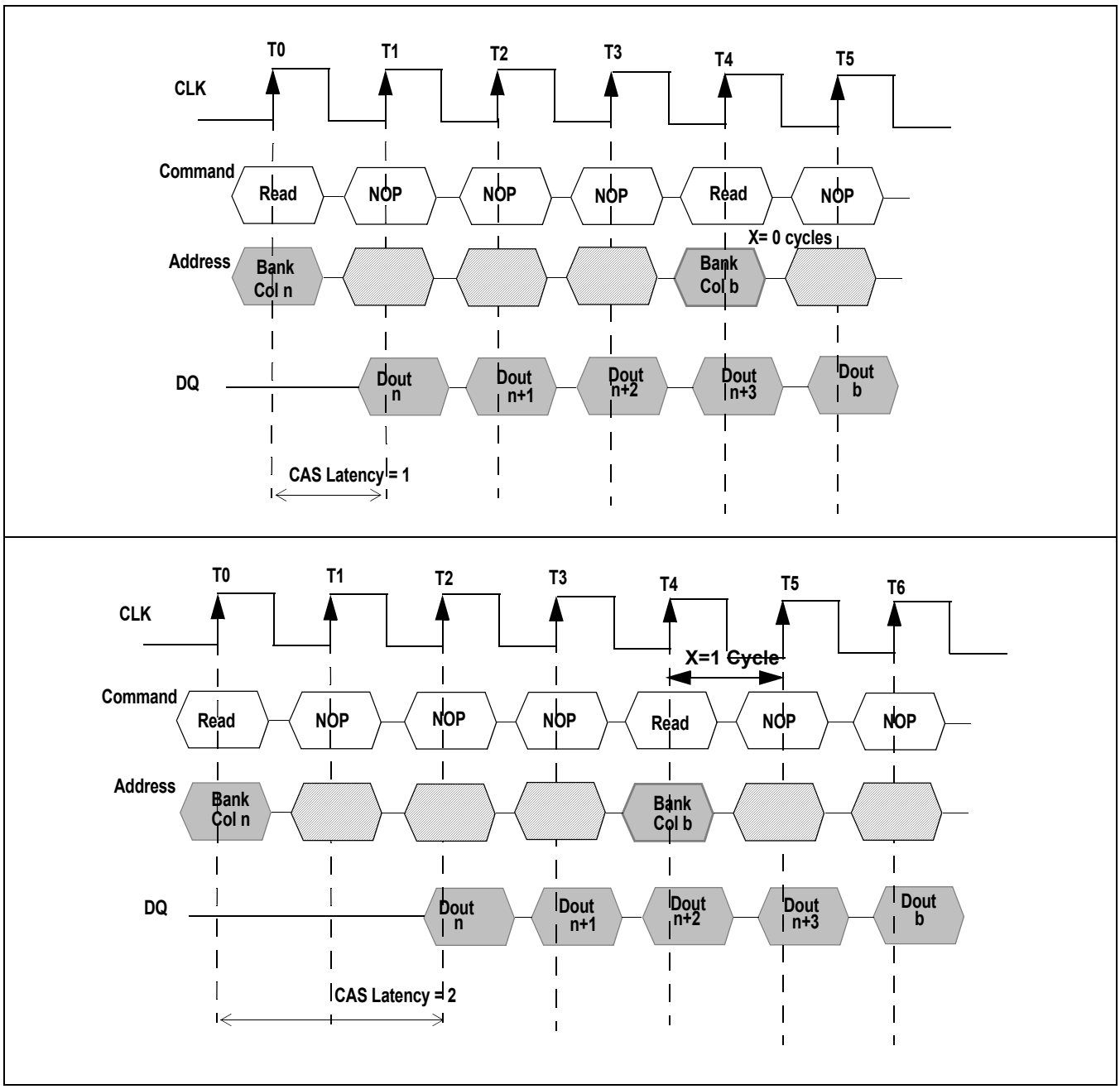


Figure 16. Consecutive Burst Reads -Transition from Burst of 4 Read to a Single read for CAS latency 1,2,3

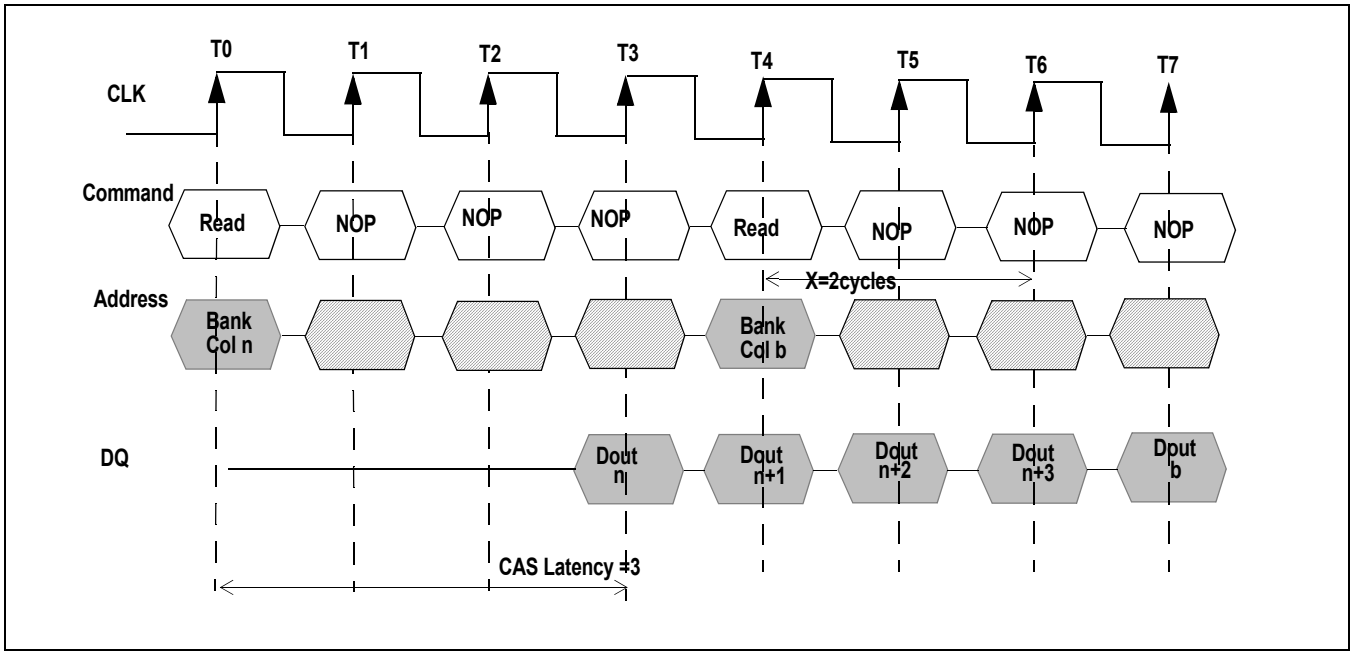


Figure 16. Consecutive Burst Reads -Transition from Burst of 4 Read to a Single read for CAS latency 1,2,3

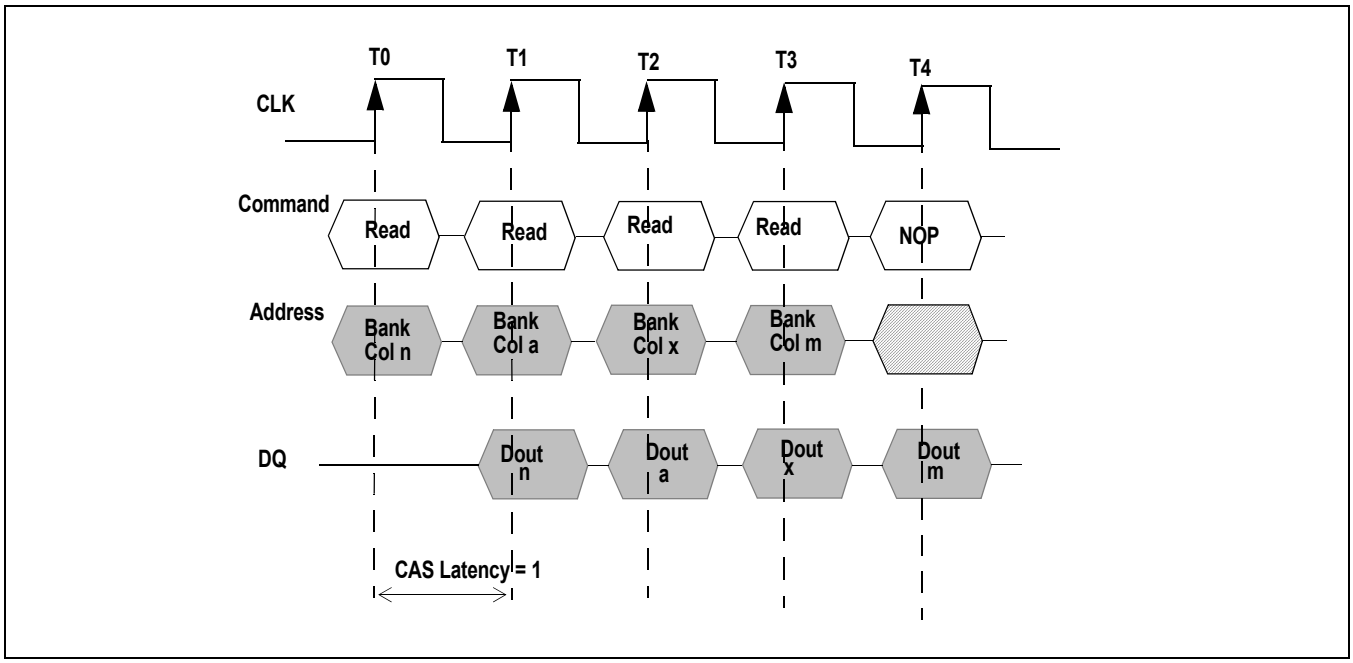


Figure 17. Random Read Accesses for CAS LAtency =1,2,3

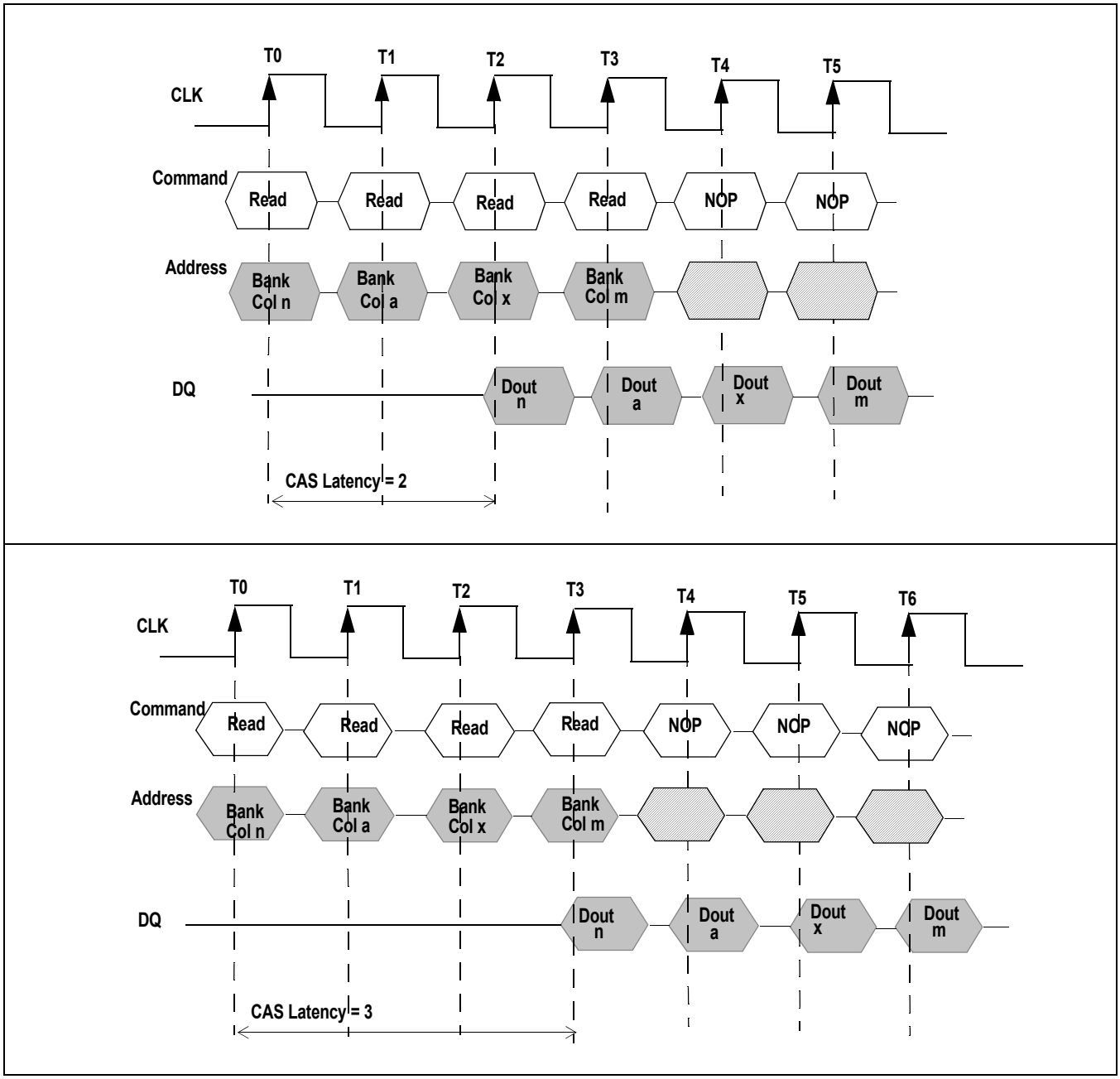


Figure 17. Random Read Accesses for CAS LAtency =1,2,3

A Read Burst can be terminated by a subsequent Write command, and data from a fixed length READ burst may be immediately followed by data from a WRITE command (subject to bus turnaround limitations). The WRITE burst may be initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided. In a given system design, there may be a possibility that the device driving the input data will go Low-Z before the SDRAM DQs go High-Z. In this case, at least a single-cycle delay should occur between the last read data and the WRITE command. The U(L)DQM input is used to avoid I/O contention, as shown in Figure 18. and Figure 19.. The U(L)DQM signal must be asserted (HIGH) at least two clocks prior to the WRITE command (U(L)DQM latency is two clocks for output buffers) to suppress data-out from the READ. Once the WRITE command is registered, the DQs will go High-Z (or remain High-Z), regardless of the state of the U(L)DQM signal, provided the U(L)DQM was active on the clock just prior to the WRITE command that truncated the READ command. The U(L)DQM signal must be de-asserted prior to the WRITE command (U(L)DQM latency is zero clocks for input buffers) to ensure that the written data is not masked. Figure 18.shows the case where the clock frequency allows for bus contention to be avoided without adding a NOP cycle, and Figure 19.shows the case where the additional NOP is needed.

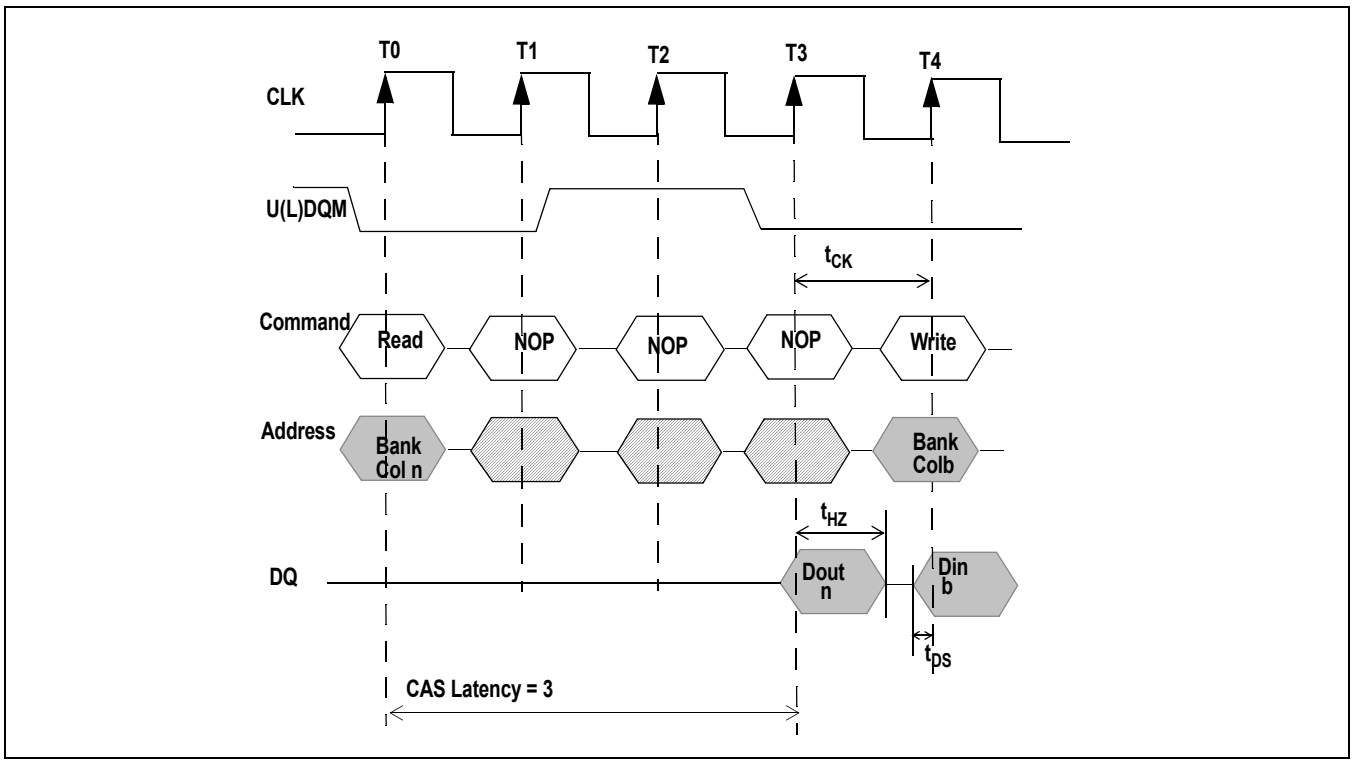


Figure 18. Read to Write

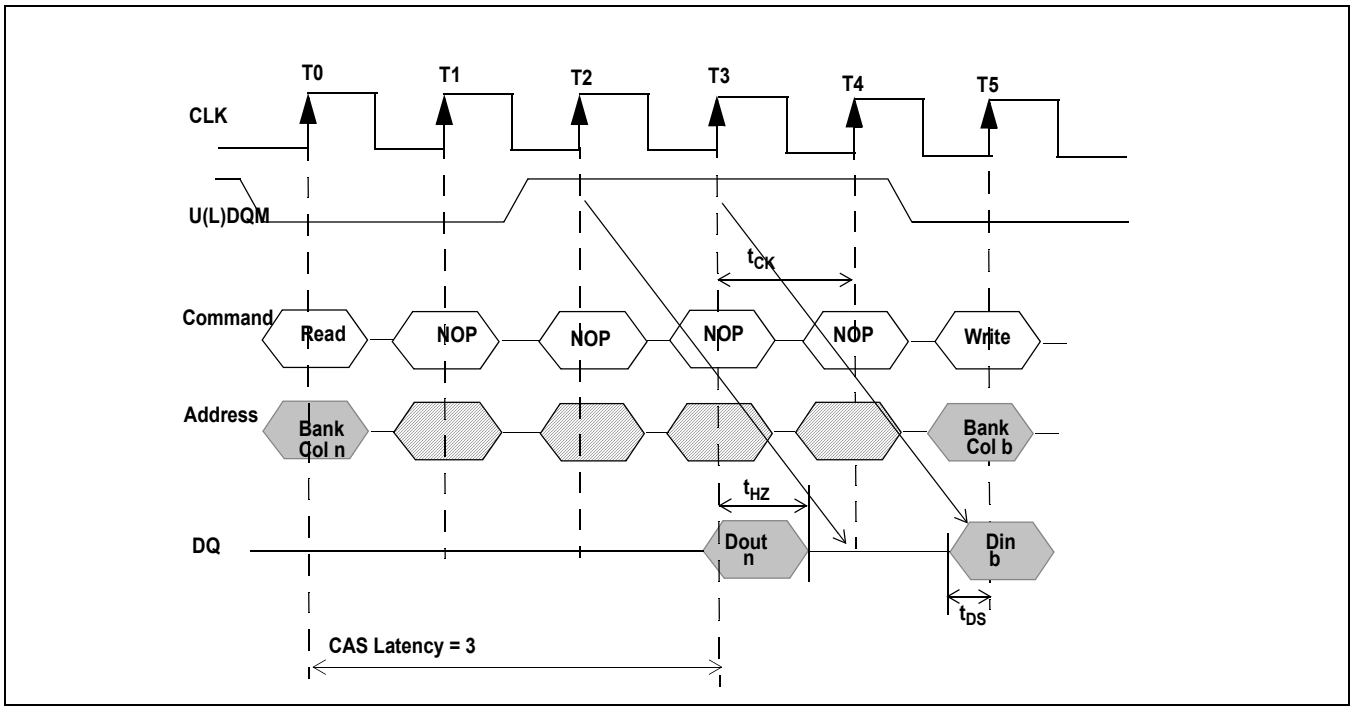


Figure 19. Read to Write with extra clock cycle

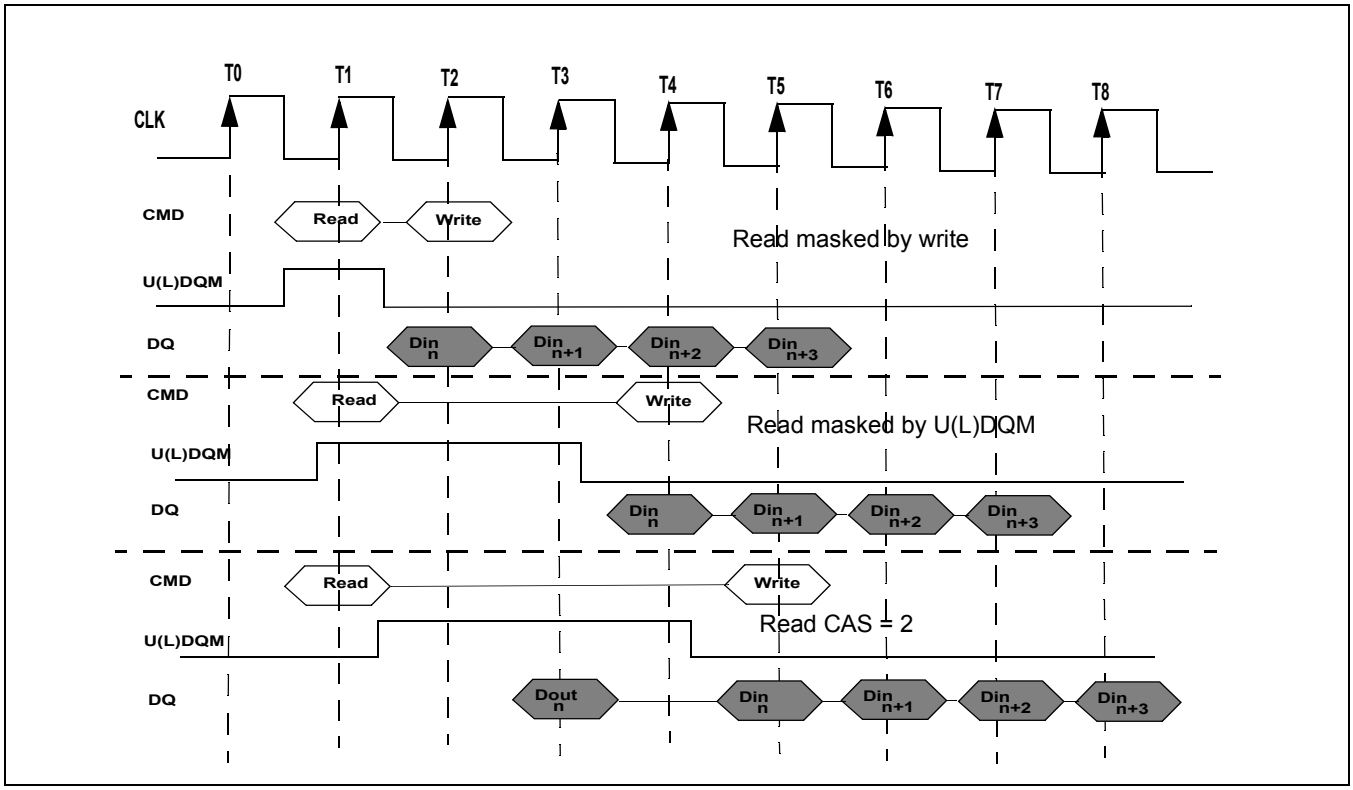


Figure 20. Read Interrupted by Write and U(L)DQM ; CAS Latency =2

A fixed-length READ burst or a full-page burst may be followed by, or truncated with, a PRECHARGE command to the same bank . The PRECHARGE command should be issued ***x*** cycles before the clock edge at which the last desired data element is valid, where ***x*** equals the CAS latency minus one. This is shown in Figure 21. for each possible CAS latency; data element *n* + 3 is either the last of a burst of four or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until t_{RP} is met. Note that part of the row precharge time is hidden during the access of the last data element(s). The BURST TERMINATE command should be issued ***x*** cycles before the clock edge at which the last desired data element is valid, where ***x*** equals the CAS latency minus one. This is shown in Figure 22. for each possible CAS latency; data element *n* + 3 is the last desired data element of a longer burst.

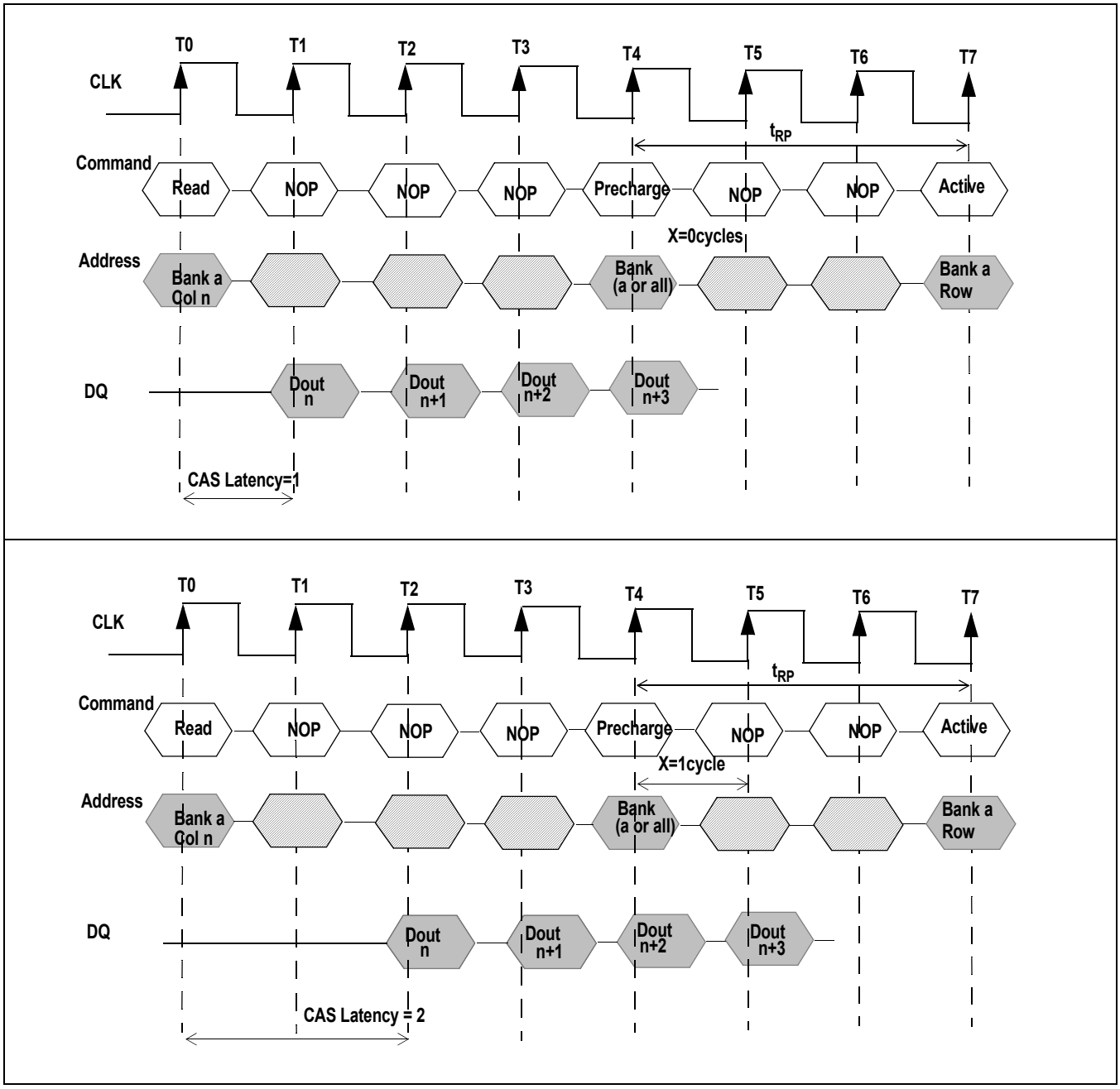


Figure 21. Read to Precharge

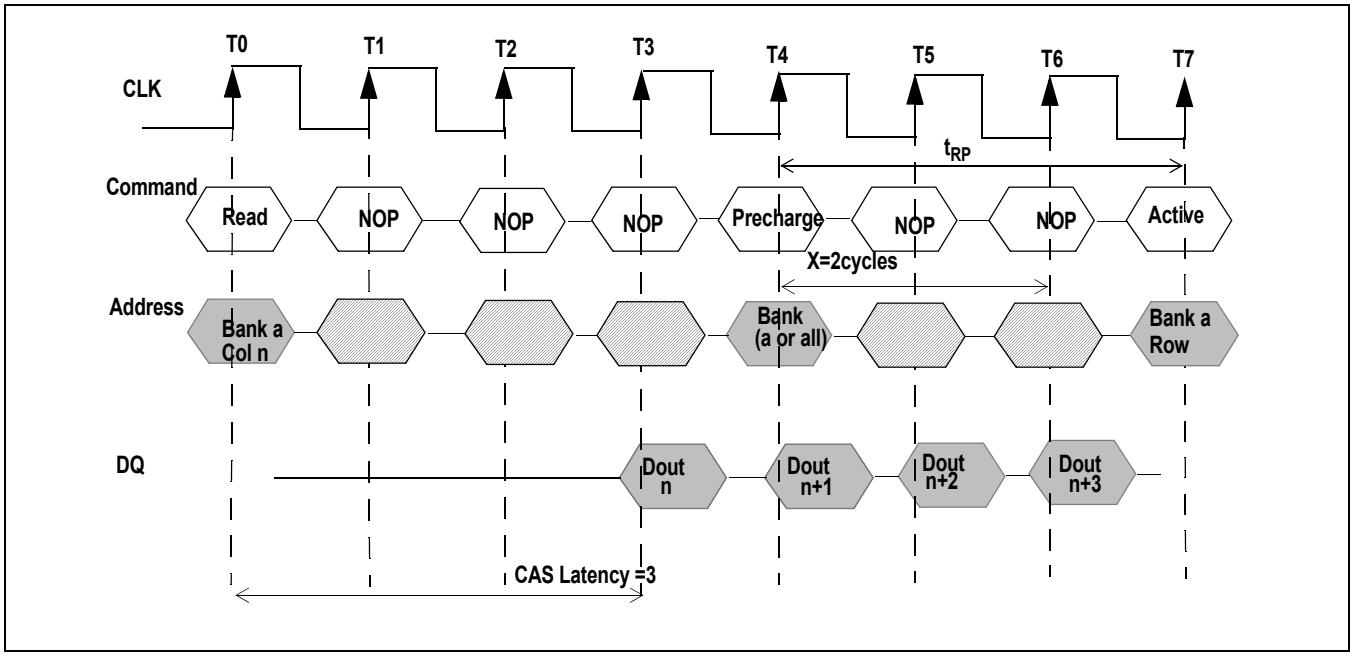


Figure 21. Read to Precharge

Write Operation

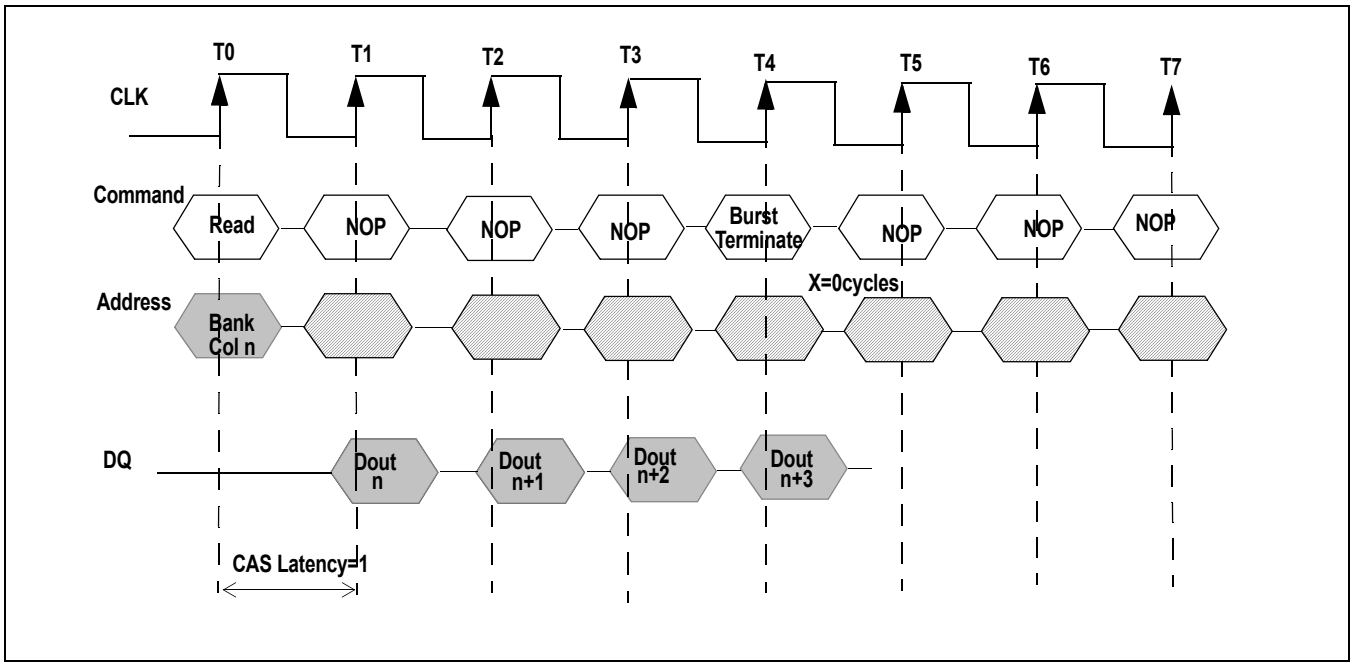


Figure 22. Terminating a Read Burst

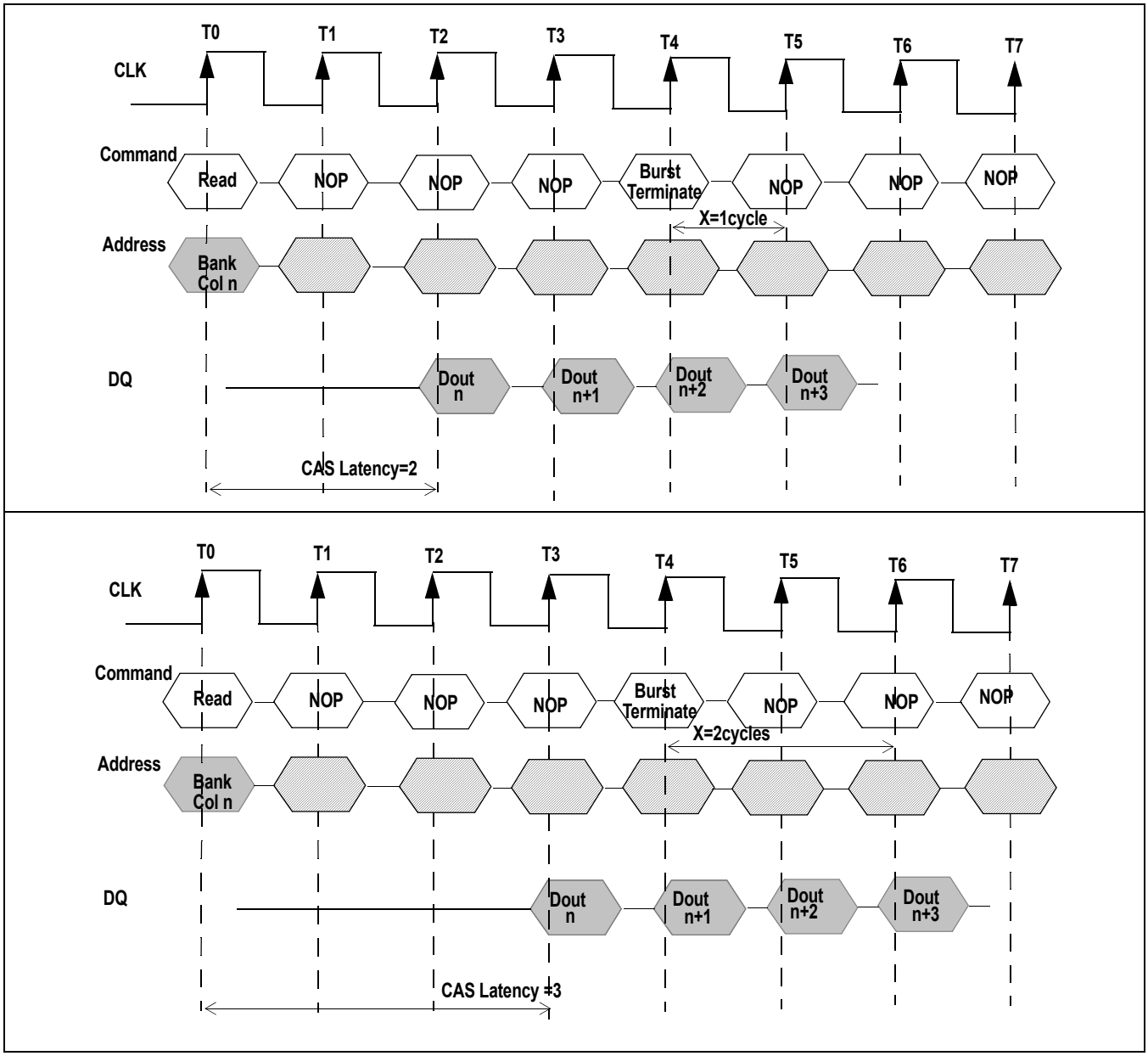


Figure 22. Terminating a Read Burst

WRITE bursts are initiated with a WRITE command,as shown in Figure 23. The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. During WRITE bursts, the first valid data-in element will be registered coincident with the WRITE command. Subsequent data elements will be registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored (see Figure 24.). A fullpage burst will continue until terminated. (wrap around at the end of the page) An example is shown in Figure 25. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst. A WRITE command can be initiated on any clock cycle following a previous WRITE command. Full-speed random write accesses within a page can be performed to the same bank, as shown in Figure 26. or each subsequent WRITE may be performed to a different bank.

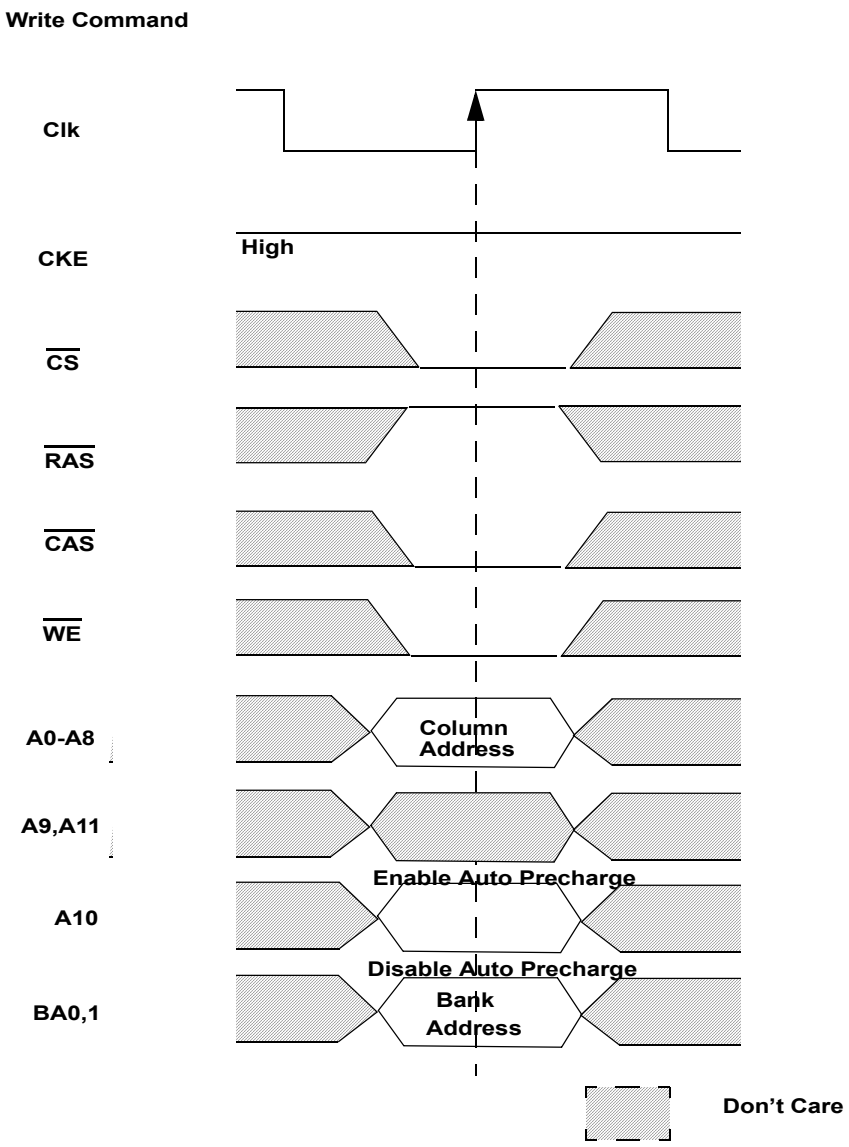


Figure 23. Write Command

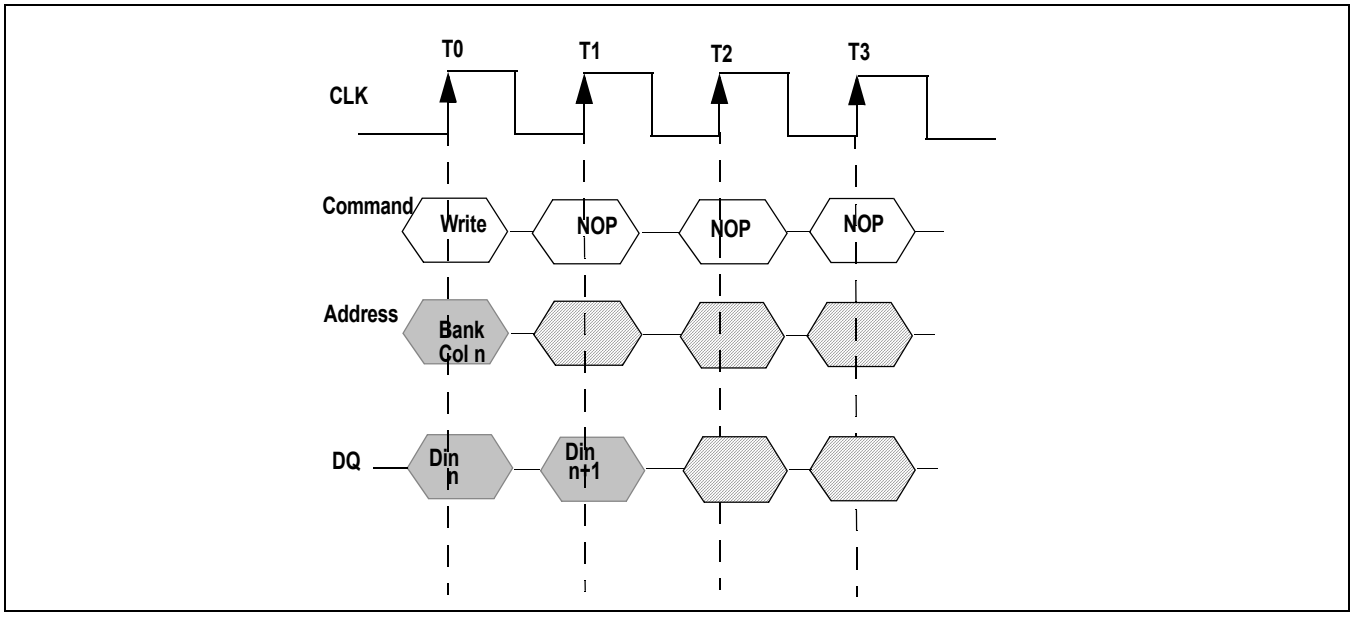


Figure 24. Write Burst - Burst length of 2

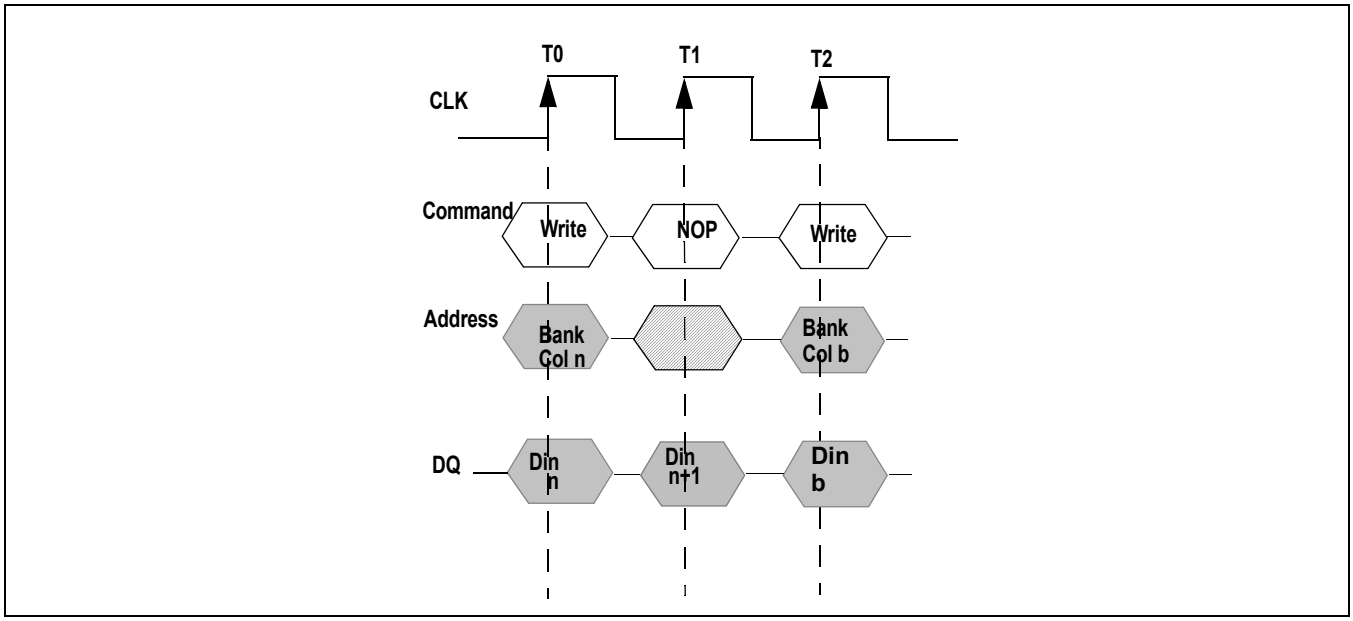


Figure 25. Write to Write - Transition from a burst of 2 to a single write

Data for a fixed-length WRITE burst a full-page WRITE bursmay be followed by, or truncated with, a PRECHARGE command to the same bank.The PRECHARGE command should be issued t_{WR} after the clock edge at which the last desired input data element is registered. The auto precharge mode requires a t_{WR} of atleast one clock plus time, regardless of frequency. In addition, when truncating a WRITE burst, the U(L)DQM signal must be used to mask input data for the clock edge prior to, and the clock edge coincident with, the PRECHARGE command. An example is shown in Figure 28. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until

t_{RP} is met. An example is shown in Figure 27.. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst.

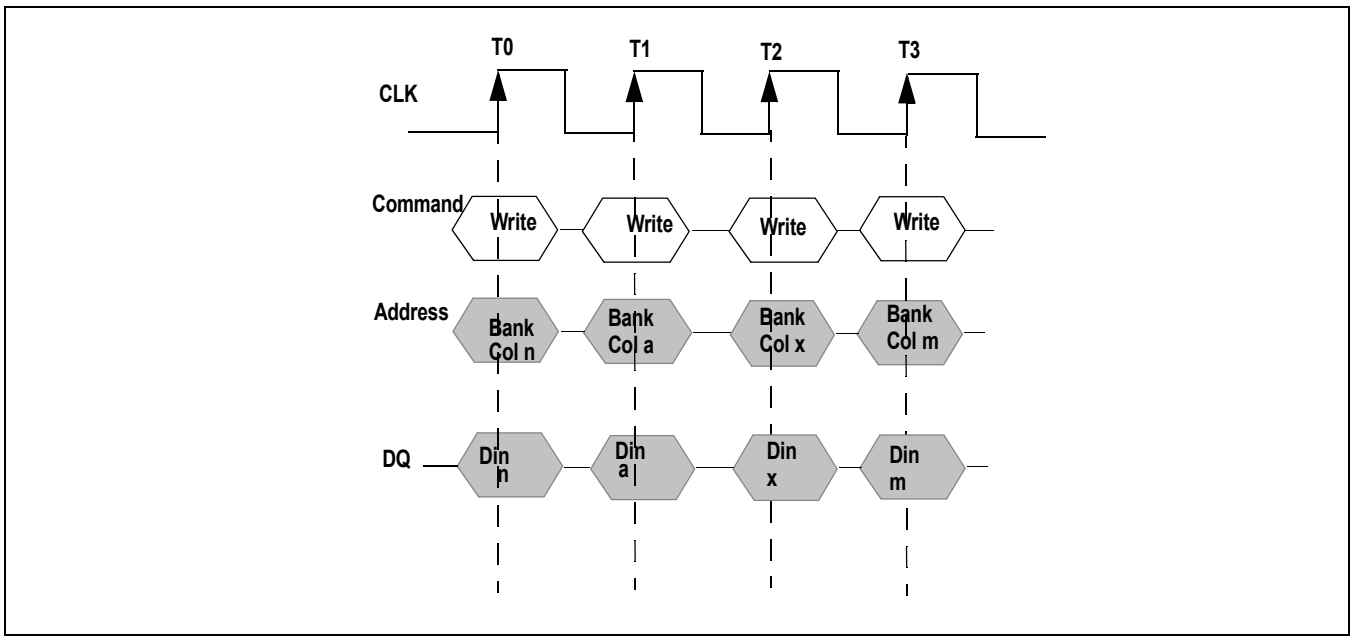


Figure 26. Random Write Cycles

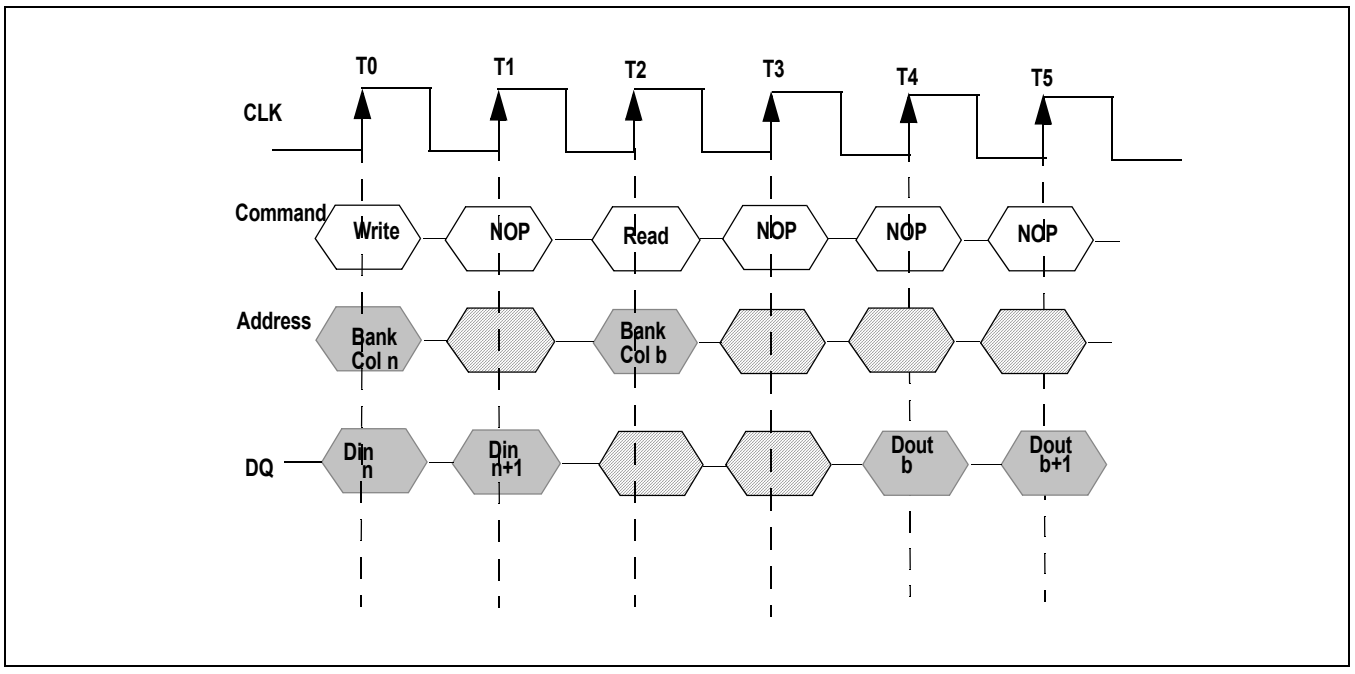


Figure 27. Write to Read Burst of 2 Write and Read(CAS Latency =2)

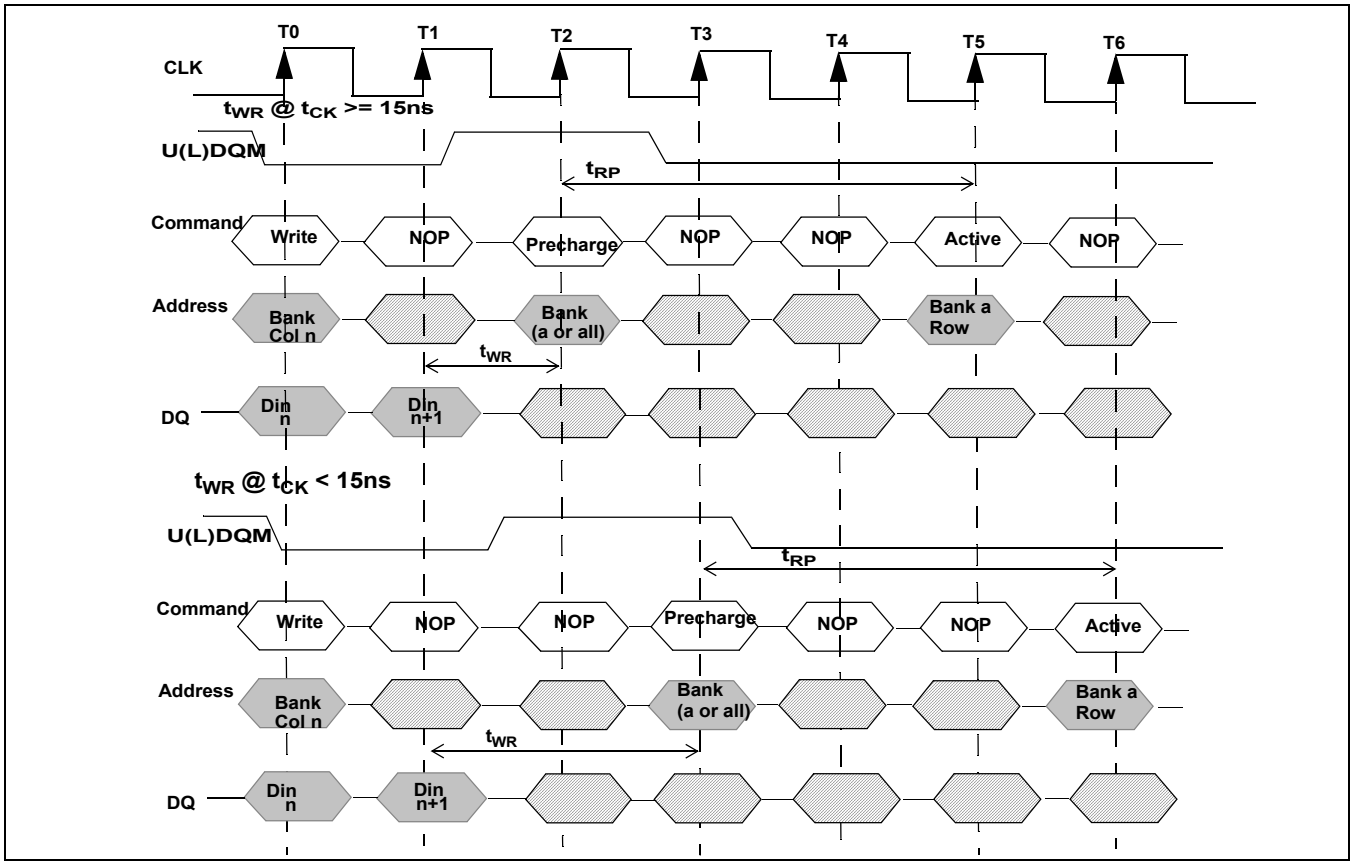


Figure 28. Write to Precharge

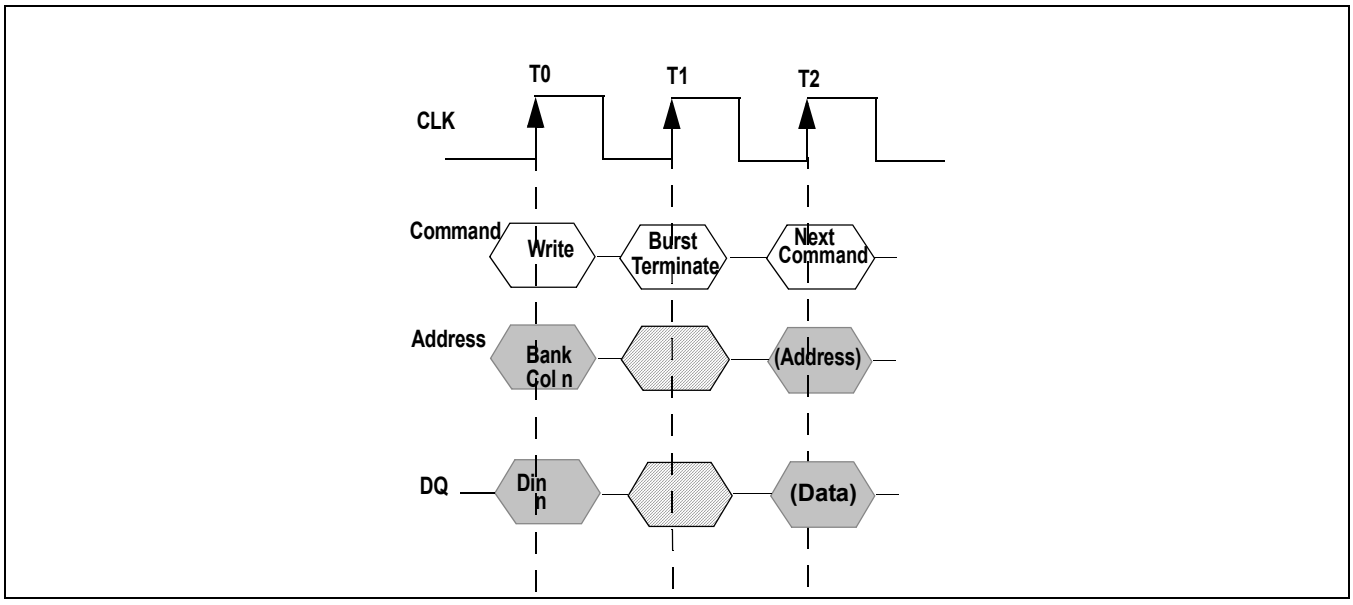


Figure 29. Terminating a Write Burst

Fixed-length or full-page WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied coincident with the BURST TERMINATE command will be ignored. The last data written (provided that U(L)DQM is LOW at that time) will be the input data applied one clock previous to the BURST TERMINATE command. This is shown in Figure 29., where data *n* is the last desired data element of a longer burst.

PRECHARGE

The PRECHARGE command (see Figure 30.) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (t_{RP}) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as “Don’t Care.” Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

POWER-DOWN

Power-down occurs if CKE is registered LOW coincident with a NOP or COMMAND INHIBIT when no accesses are in progress. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby. The device may not remain in the power-down state longer than the refresh period (64ms) since no refresh operations are performed in this mode. The power-down state is exited by registering a NOP or COMMAND INHIBIT and CKE HIGH at the desiredclock edge (meeting t_{CKS}). See Figure 31.

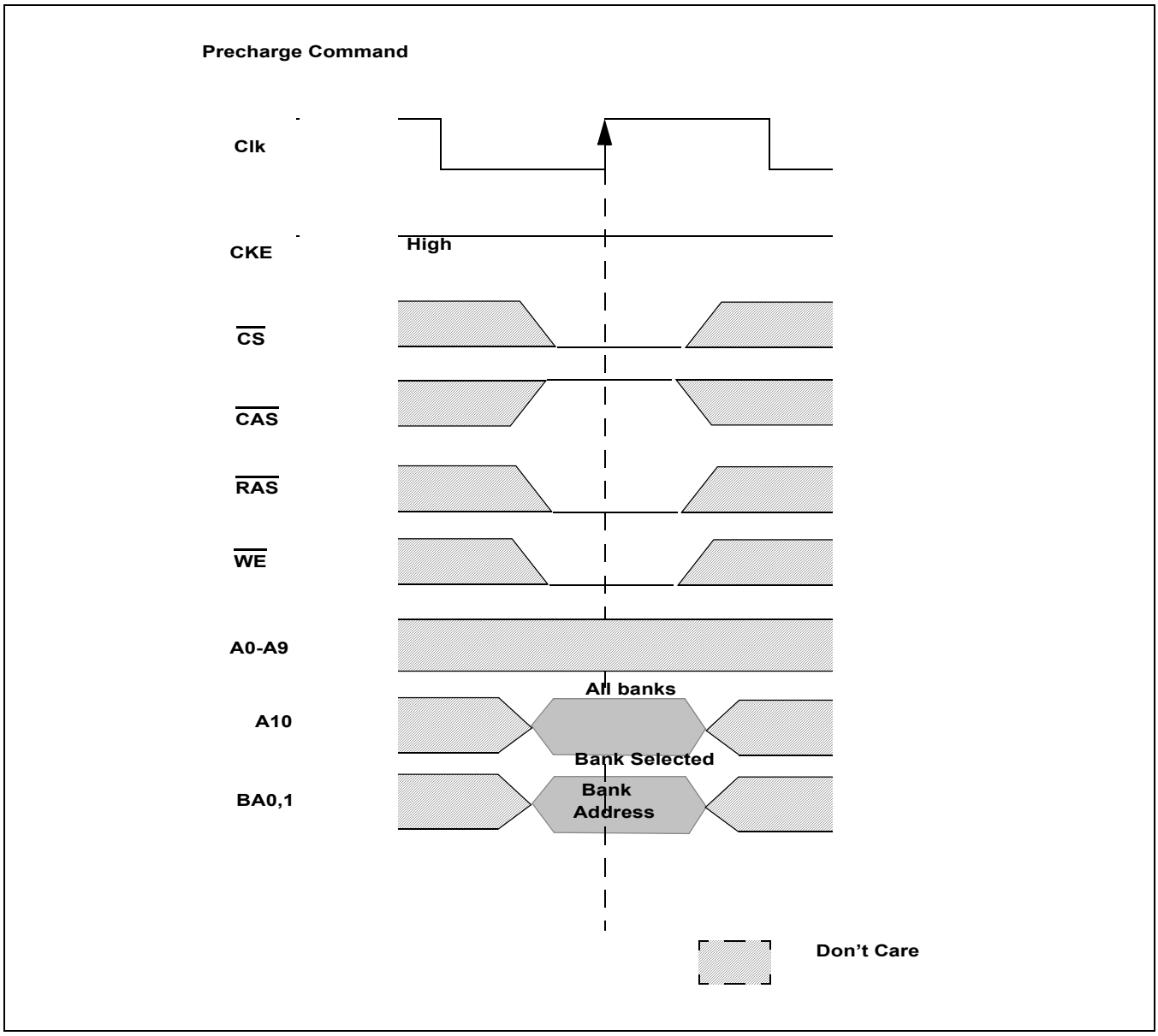


Figure 30. Precharge Command

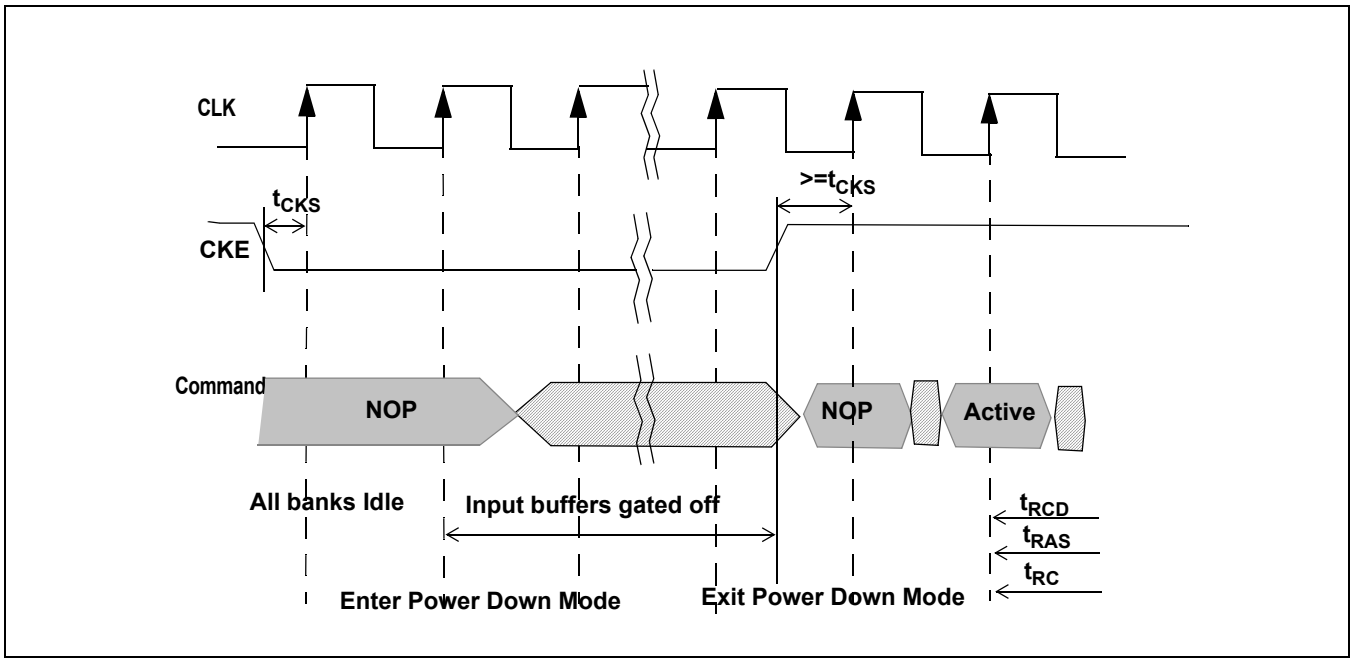


Figure 31. Power Down

CLOCK SUSPEND

The clock suspend mode occurs when a column access/ burst is in progress and CKE is registered LOW. In the clock suspend mode, the internal clock is deactivated, “freezing” the synchronous logic. For each positive clock edge on which CKE is sampled LOW, the next internal positive clock edge is suspended. Any command or data present on the input pins at the time of a suspended internal clock edge is ignored; any

data present on the DQ pins remains driven; and burst-counters are not incremented, as long as the clock is suspended. (See examples in Figure 32. and Figure 33.) Clock suspend mode is exited by registering CKE HIGH; the internal clock and related operation will resume on the subsequent positive clock edge.

BURST READ/SINGLE WRITE

In this mode, all WRITE commands result in the access of a single column location (burst of one), regardless of the programmed burst length. The burst read/single write mode is entered by programming the write burst mode bit (M9) in the

mode register to a logic 1. READ commands access columns according to the programmed burst length and sequence.

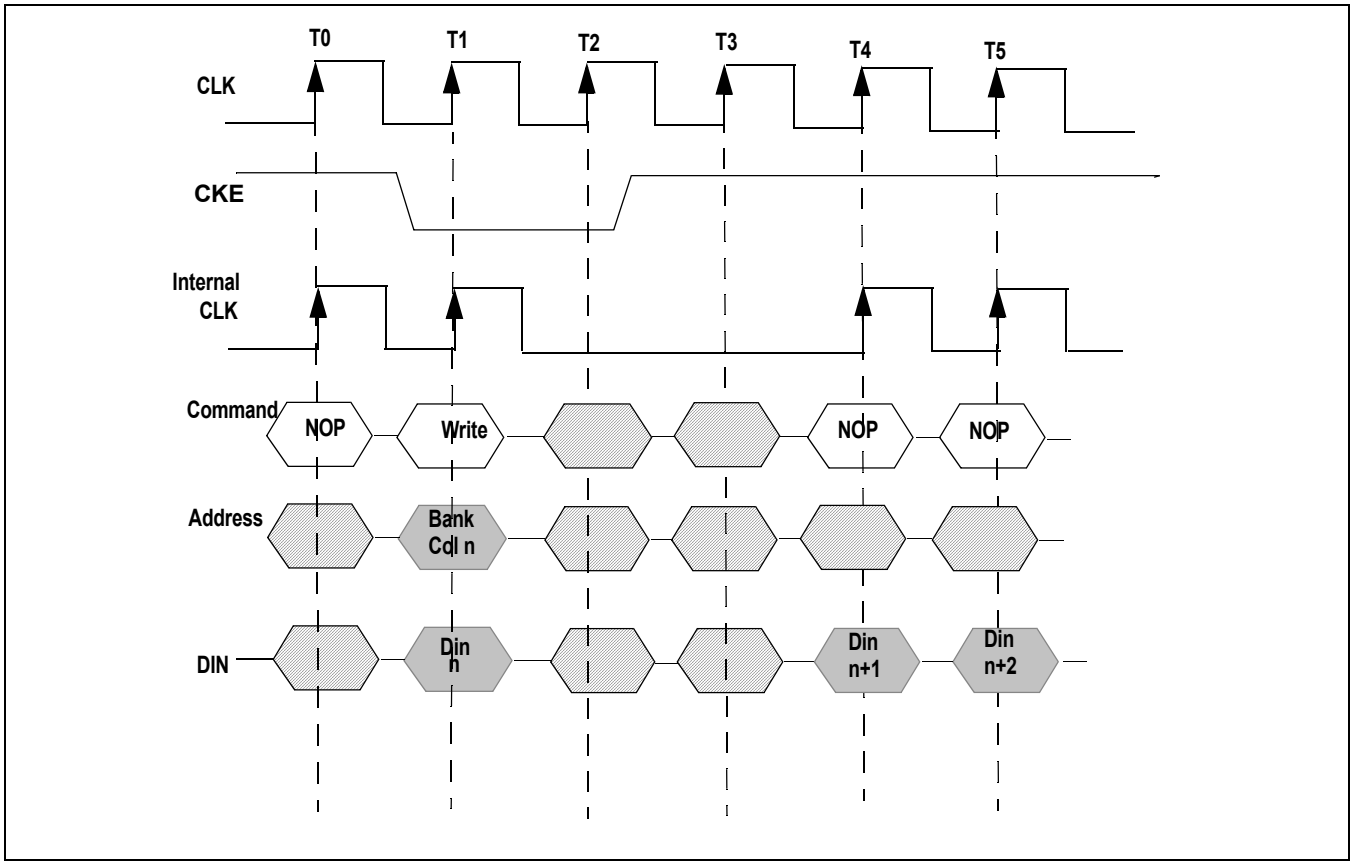


Figure 32. Clock Suspend During Write Burst

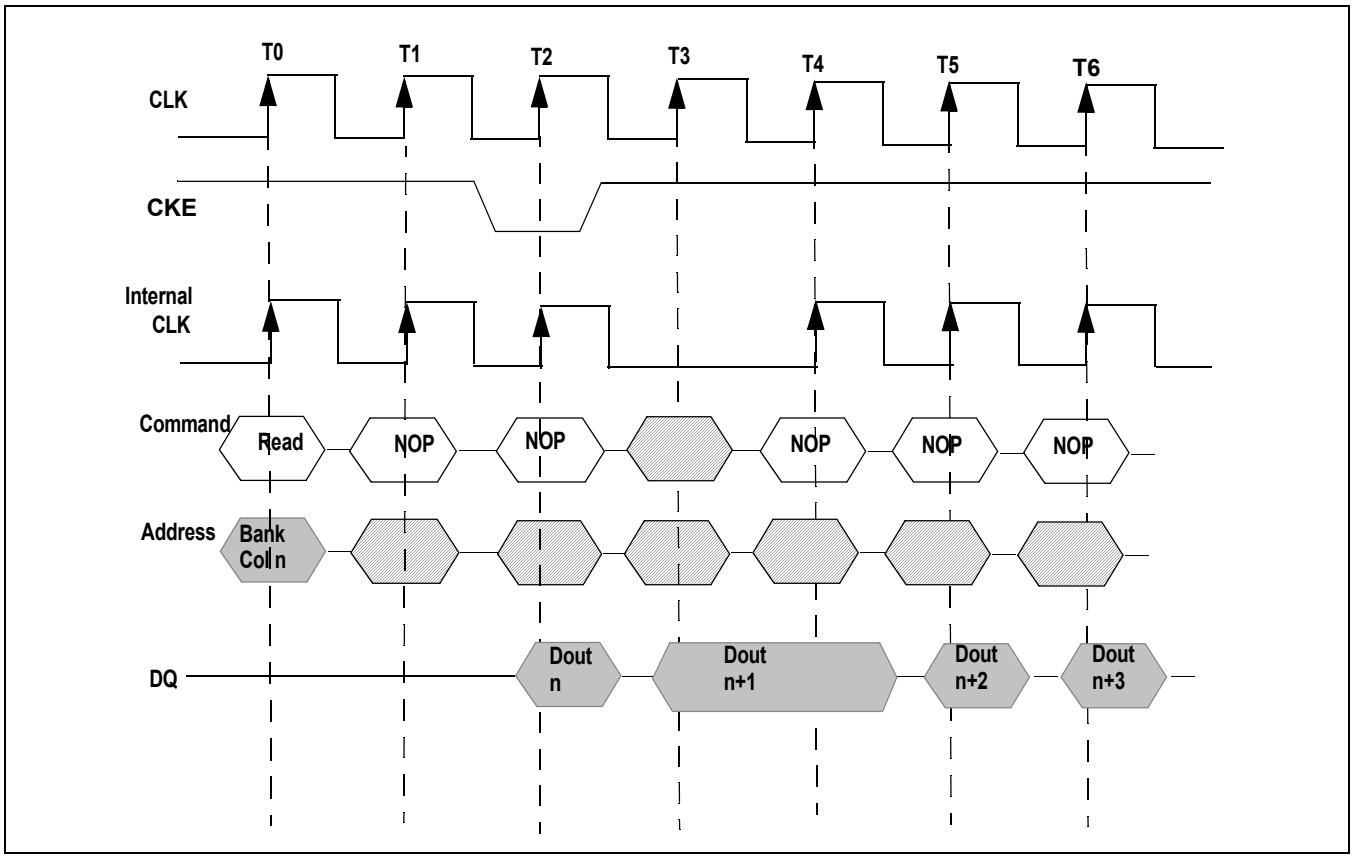


Figure 33. Clock Suspend During Read Burst - Burst of 4 (CAS latency =2)

Concurrent Auto Precharge

If an access command with Auto Precharge is being exeeuted ; an access command (either a Read or Write) is not allowed by SDRAM's. If this feature is allowed then the SDRAM supports Concurrent Auto Precharge. Cypress SDRAMs support Concurrent Auto Precharge.

Four cases where Concurrent Auto Precharge occurs are defined below.

Read With Auto Precharge

1. Interrupted by a Read(with or without auto precharge): A read to bank m will interrupt a Read on bank n,CAS latency later. The precharge to bank n will begin when the Read to bank m is registered. (Figure 34.)

2. Interrupted by a Write(with or without auto precharge): A Write to bank m will interrupt a Read on bank n when registered. U(L)DQM should be used two clocks prior to the Write command to prevent bus contention. The Precharge to bank n will begin when the write to bank m is registered. (Figure 35.)

Write with Auto Precharge

3. Interrupted by a Read(with or without auto precharge): A Read to bank m will interrupt a Write on bank n when registered , with the data-out appearing CAS latency later. The Precharge to bank n will begin after t_{WR} is met, where t_{WR} begins when the Read to bank m is registered. The last valid Write to bank n will be data-in registered one clock prior to the Read to bank m.(Figure 36.)

4. Interrupted by a Write (with or without auto Precharge): A Write to bank m will interrupt a Write on bank n when registered. The Precharge to bank n will begin after t_{WR} is met ,where t_{WR} begins when the Write to bank m is registered. The latest valid data Write to bank n will be data registered one clock prior to a Write to bank m.(Figure 37.)

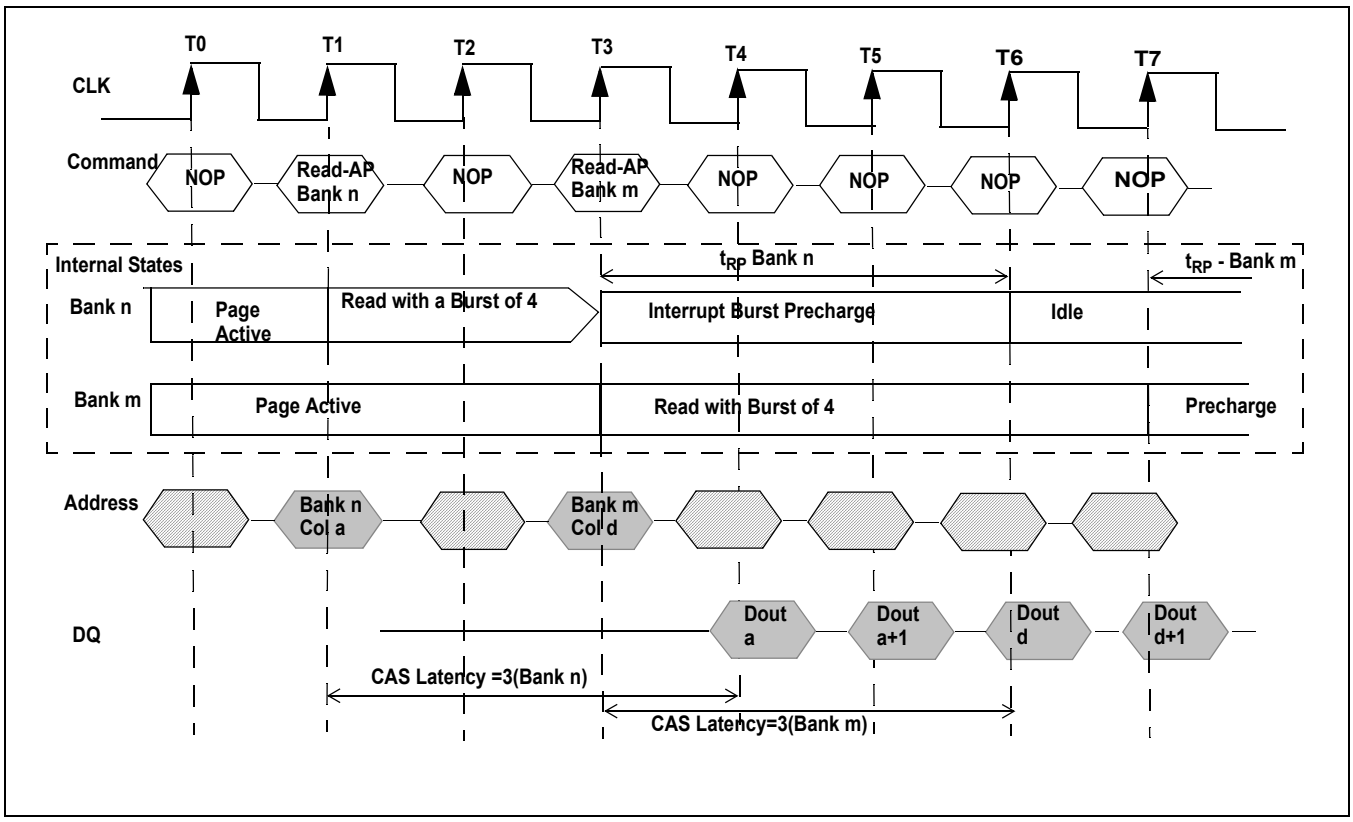


Figure 34. Read with Auto Precharge Interrupted by a Read(CAS Latency =3)

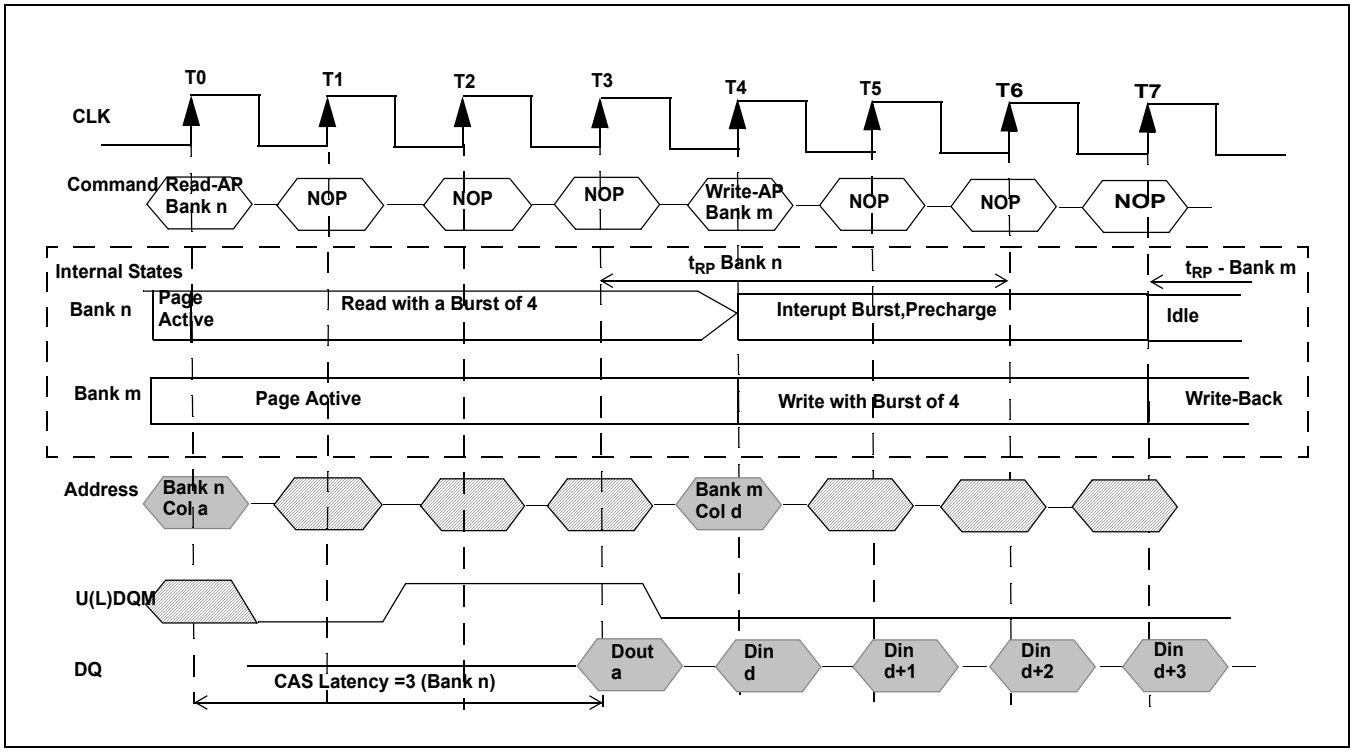


Figure 35. Read With Auto Precharge Interrupted by a Write(Read CAS Latency =3)

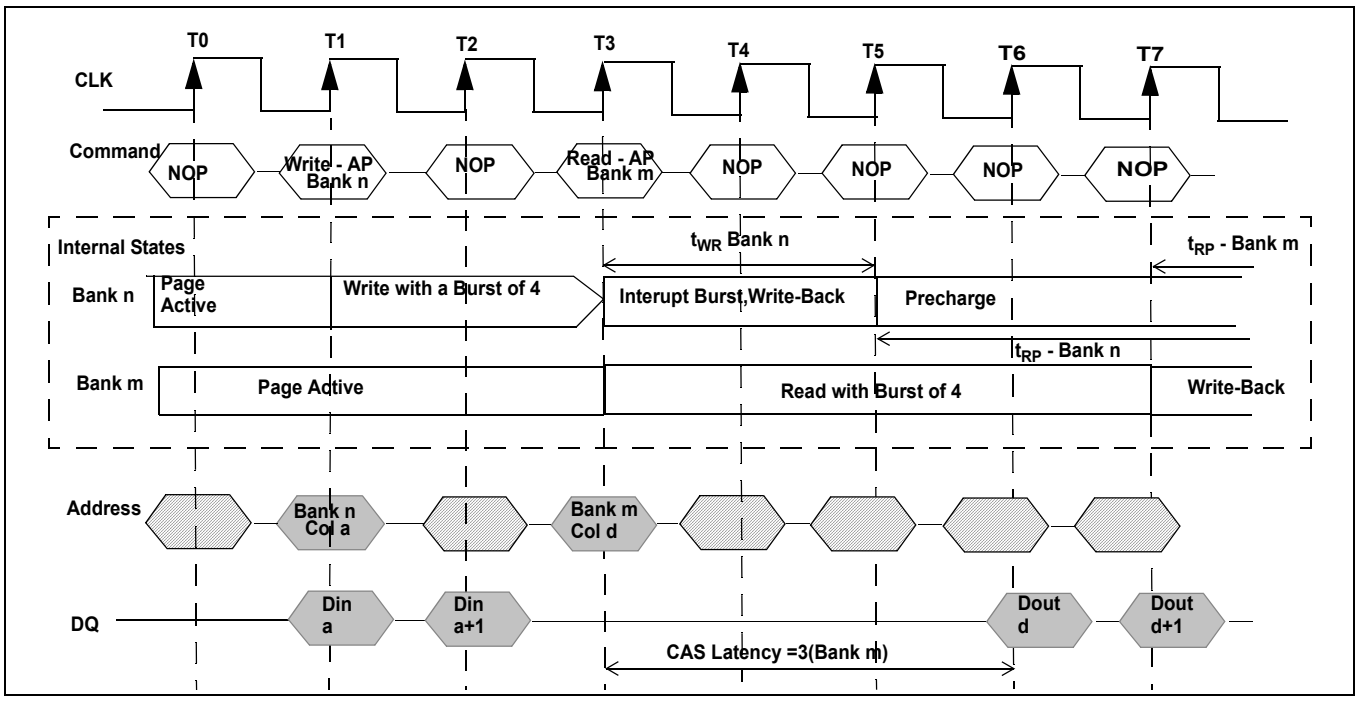


Figure 36. Write with Auto Precharge Interrupted by a Read(CAS Latency =3)

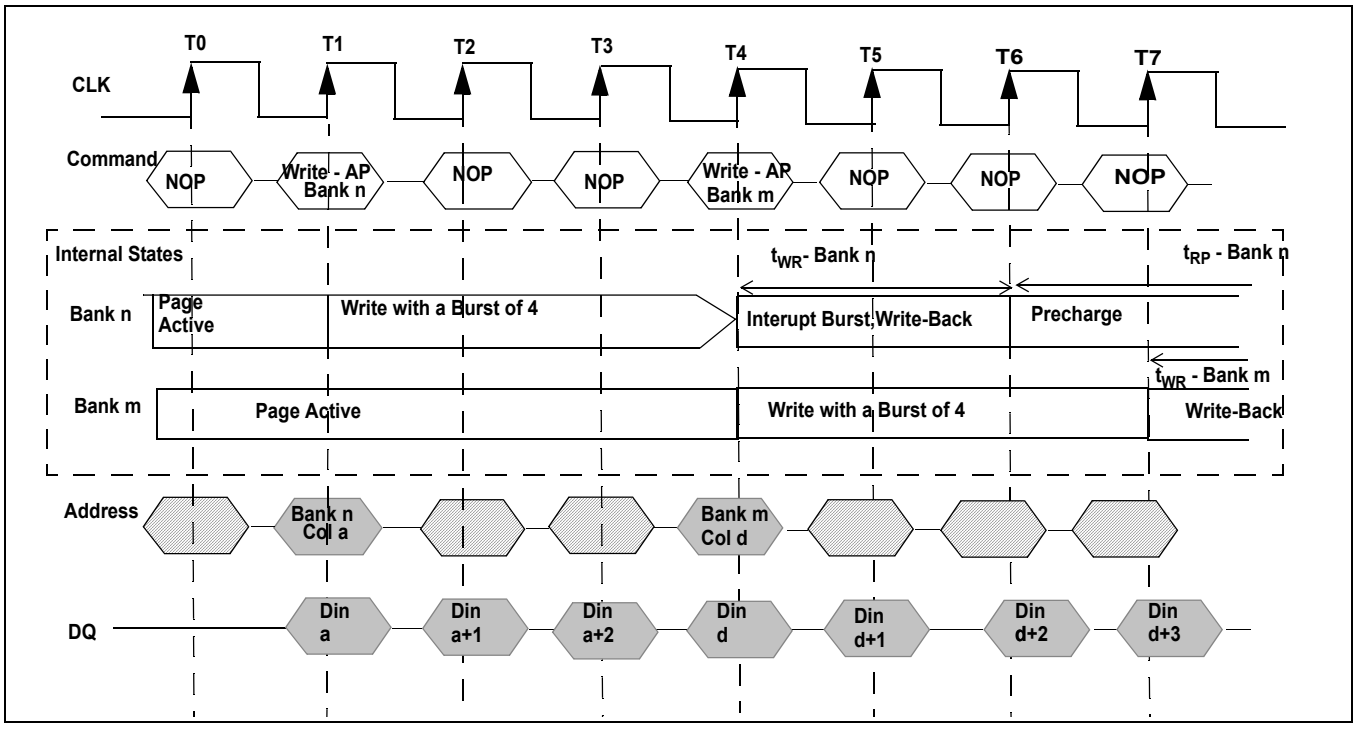
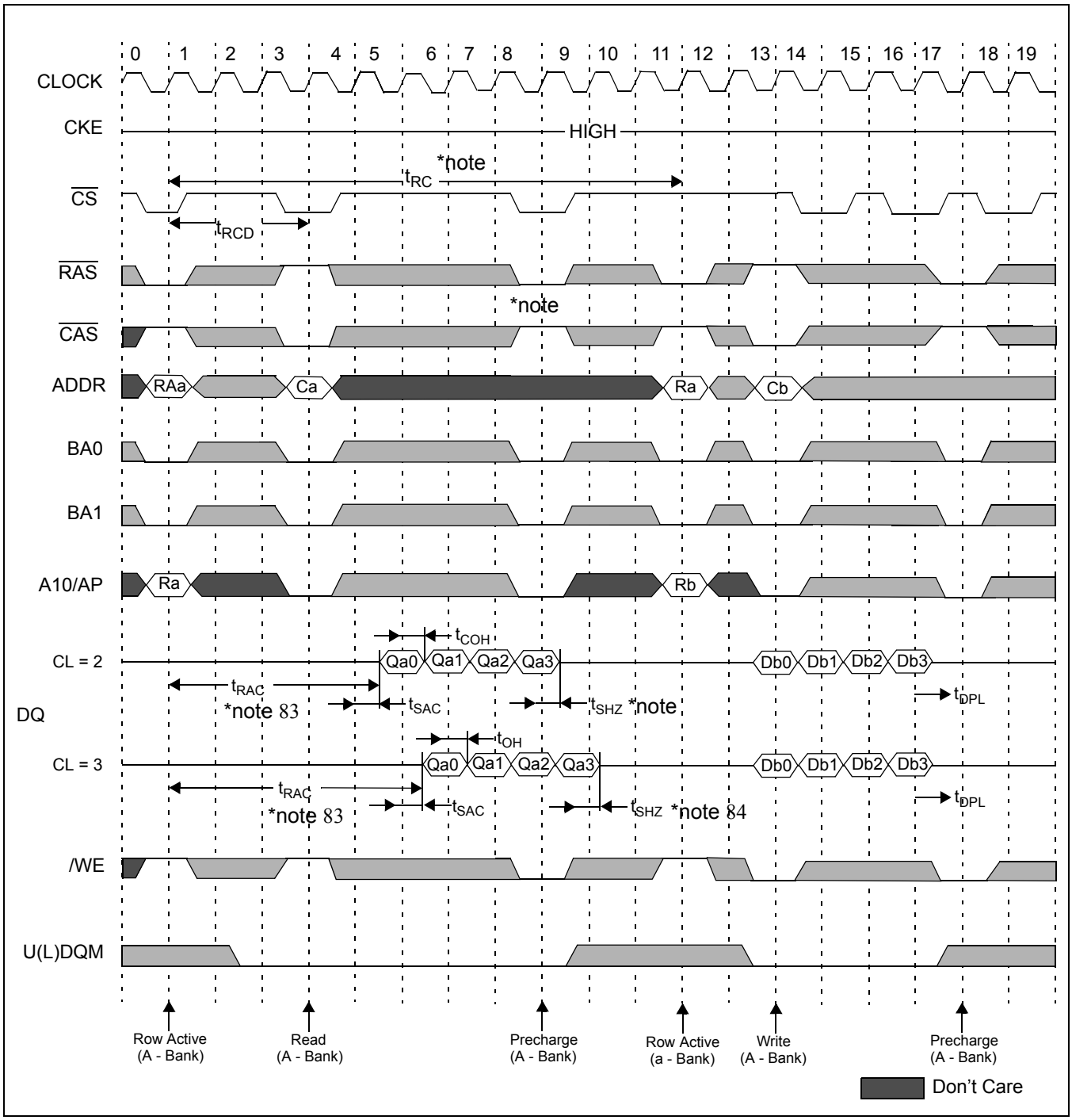


Figure 37. Write with Auto Precharge Interrupted by a Write

Read/Write Operation.



Note:

81. Minimum row cycle times is required to complete internal DRAM operation.
82. Row precharge can interrupt burst on any cycle.[CAS Latency -1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(t_{SHZ}) after the clock.
83. Access time from Row active command. tcc *(t_{RCD} + CAS latency - 1) + t_{SAC}
84. Out put will be Hi-Z after the end of burst. (1,2,3,8 & Full page bit burst)

Figure 38. Read & Write Cycle at Same Bank @Burst Length=4, tDPL=1CLK (100mhz)

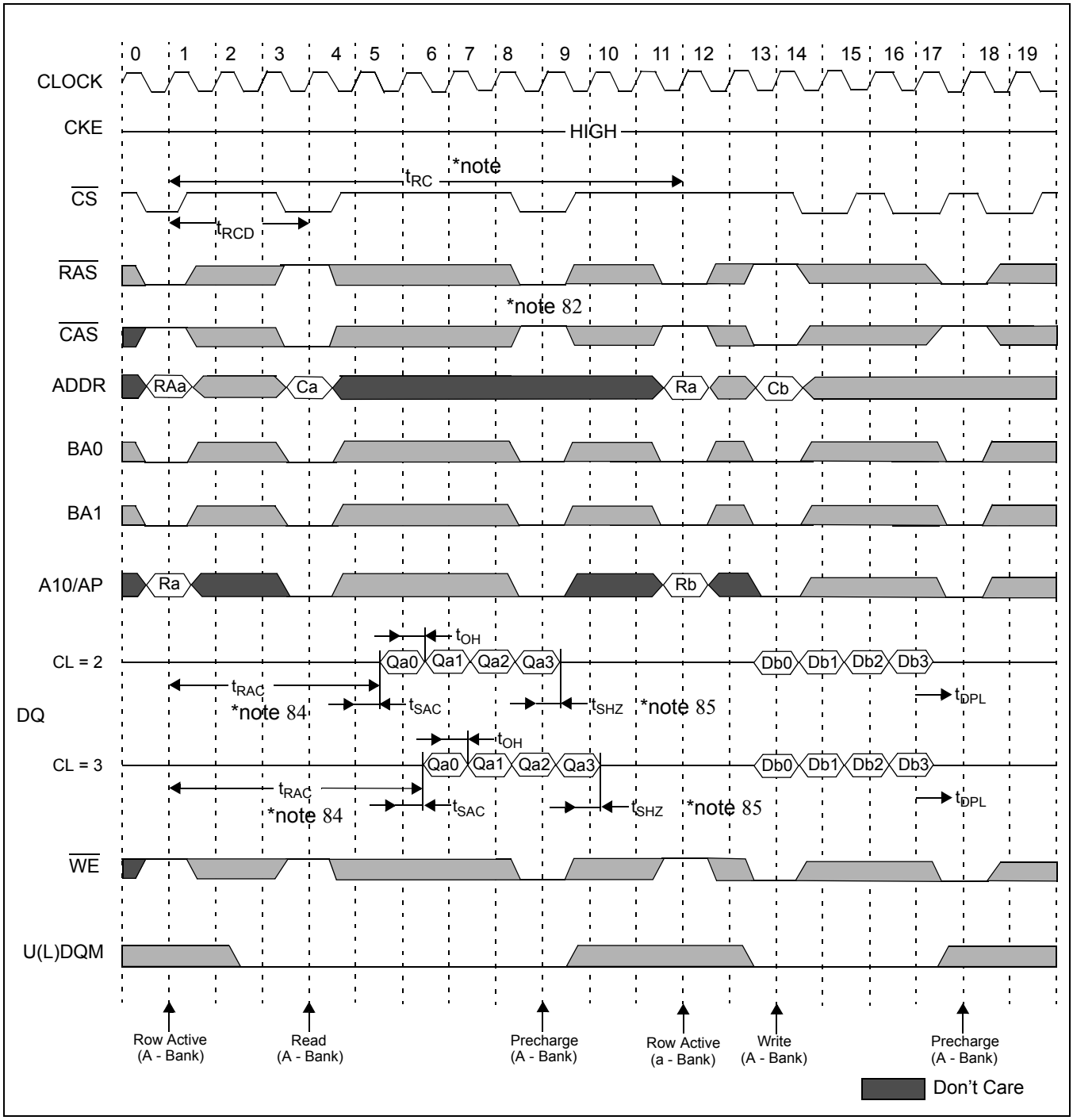
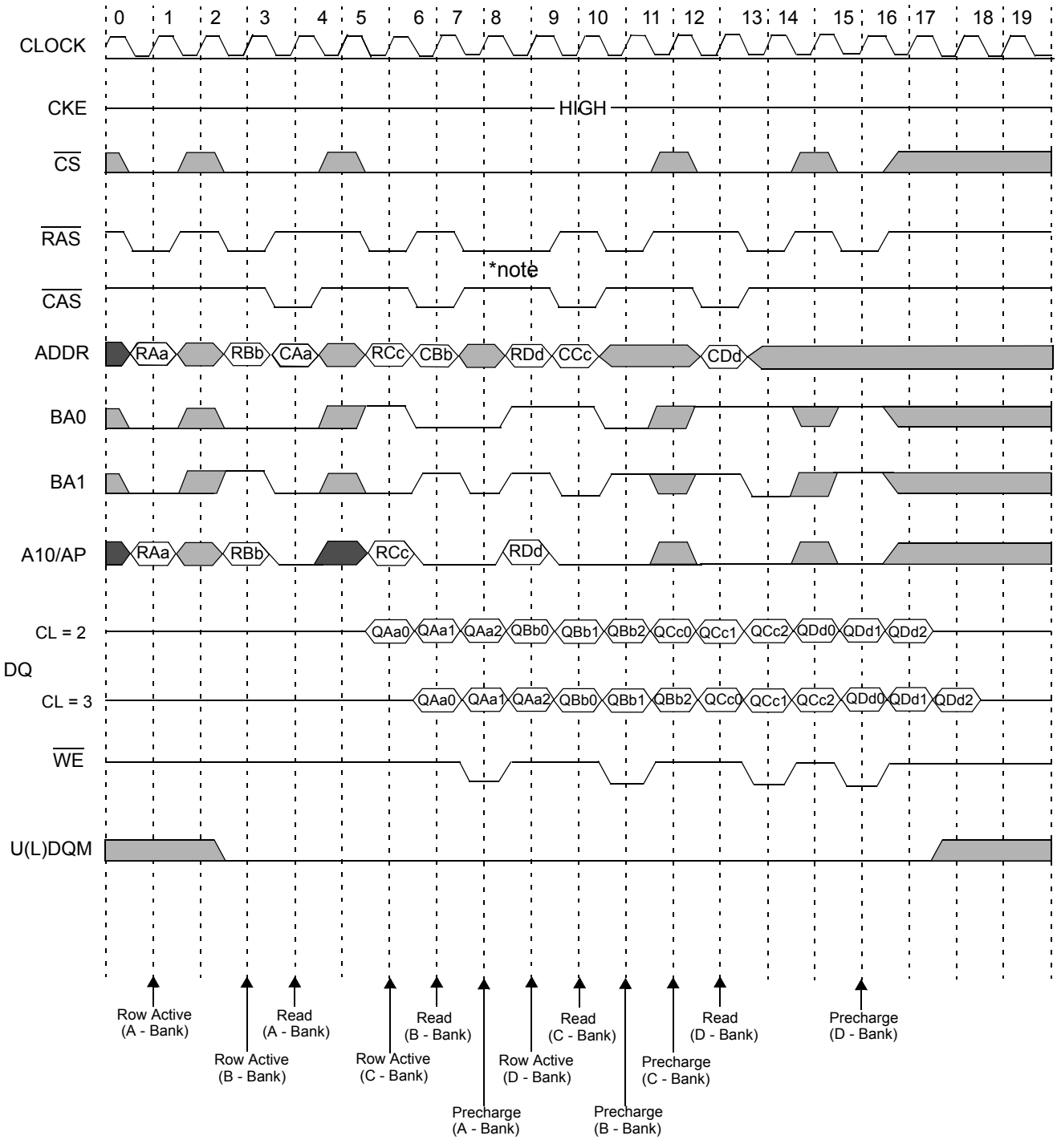


Figure 39. Read & Write Cycle at Same Bank @Burst Length=4, tDPL=2CLK (100MHz)



Notes:
85. Row precharge will interrupt writing. Last data input, tDPL before Row precharge, will be written.

Figure 40. Page Read & Write Cycle at Same Bank @ Burst Length=4, tDPL=2CLK

Deep Power Down

The LPSDRAM has an extremely low power mode called Deep Power Down. In this mode the device does not refresh internal data and data integrity is not guaranteed. Figure 41.shows the entry to this mode. Exit from this mode is similar to a power up sequence as shown in Figure 1.

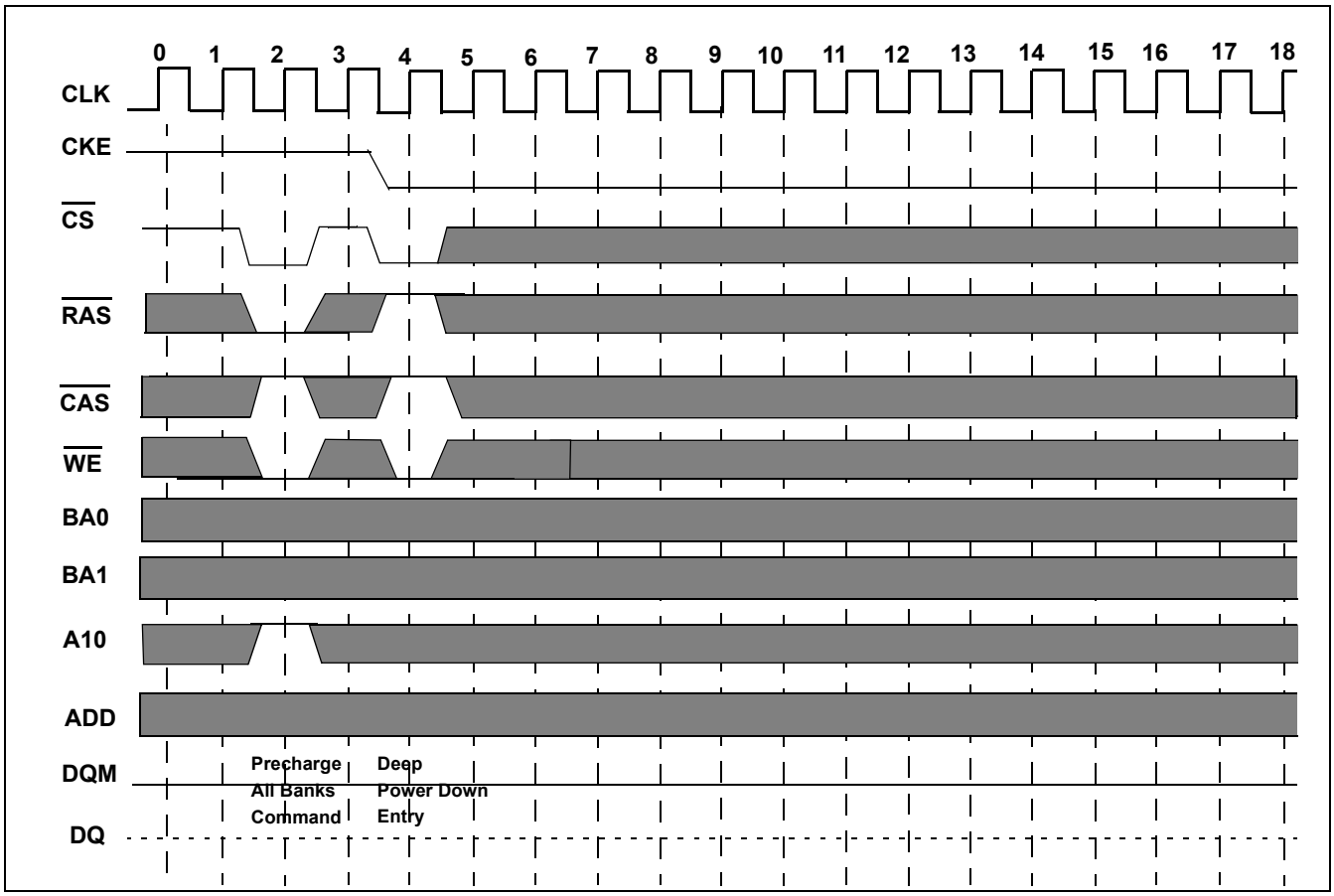


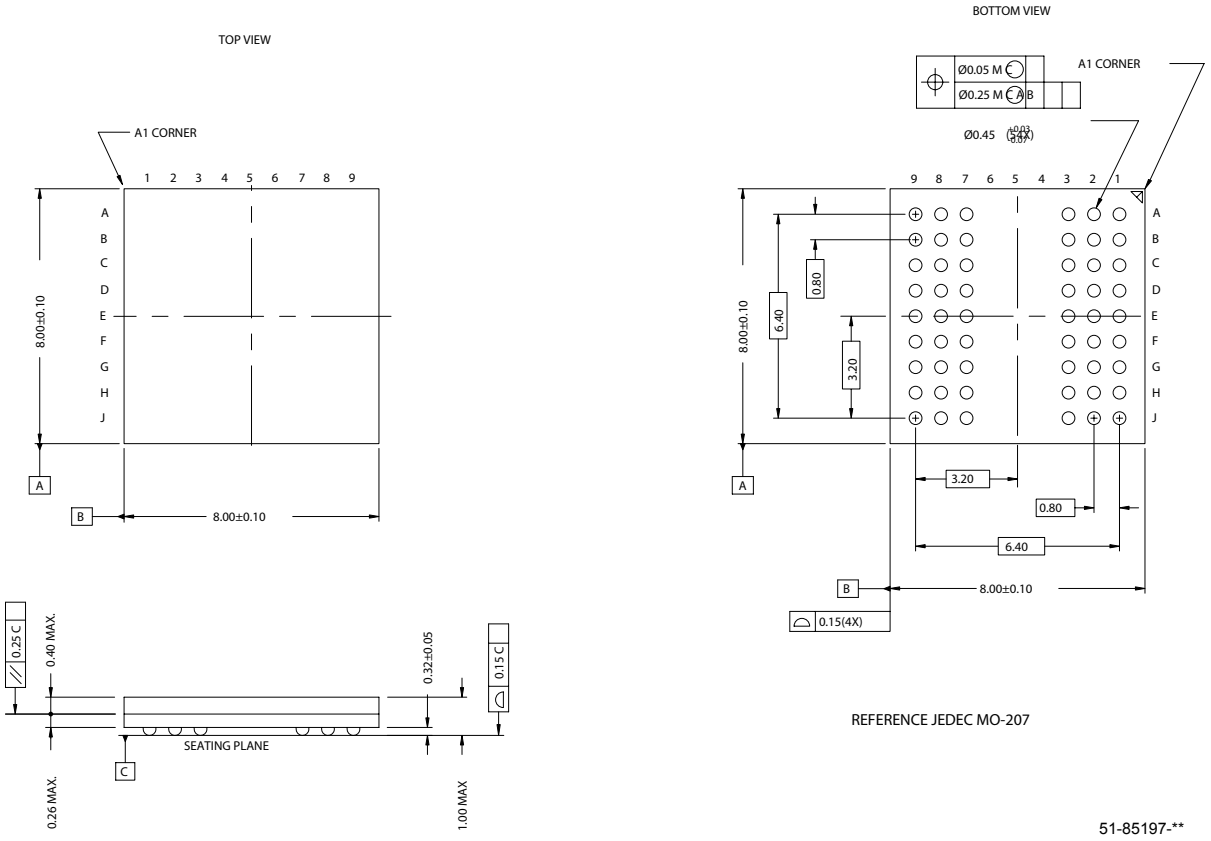
Figure 41. Deep Power Down Entry

Ordering Information

Speed (Mhz)	Ordering Code	Package Name	Package Type	Operating Range
100MHz	CYL008M162FFBU-1ABAI	BV54B	54 VFBGA (8 x 8 x 1.0 MM)	Industrial

Package Diagrams

54 VFBGA (8 x 8 x 1.0 MM)—045 MM Ball Dia. BV54B



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REV.	**ECN NO.**	**ISSUE DATE**	**ORIG. OF CHANGE**	**DESCRIPTION OF CHANGE**
**	223921	See ECN	HRT	New Data Sheet