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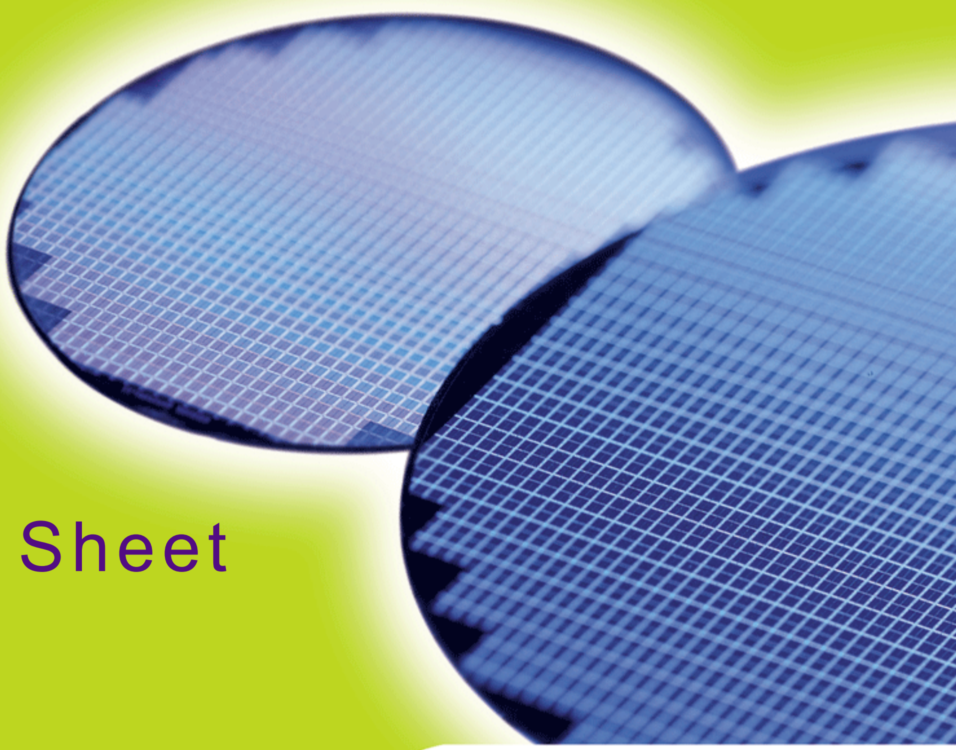
HY[B/I]18T256400B[C/F](L)
HY[B/I]18T256800B[C/F](L)
HY[B/I]18T256160B[C/F](L)

256-Mbit Double-Data-Rate-Two SDRAM
DDR2 SDRAM
RoHS Compliant Products



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HY[B/I]18T256400B[C/F](L), HY[B/I]18T256800B[C/F](L), HY[B/I]18T256160B[C/F](L) Revision History: 2007-08, Rev. 1.12	
Page	**Subjects (major changes since last revision)**
All	Adopted Internet Edition
122, 124	Corrected chapter 7: @DDR2-400: tDS1 & tDH1(base) = +25ps @DDR2-533: tDS1 & tDH1(base) = -25ps
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All	Editorial change
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1 Overview

This chapter gives an overview of the 256-Mbit Double-Data-Rate-Two SDRAM product family and describes its main characteristics.

1.1 Features

The 256-Mbit Double-Data-Rate-Two SDRAM offers the following key features:

- 1.8 V ± 0.1 V Power Supply
  1.8 V ± 0.1 V (SSTL_18) compatible I/O
- DRAM organizations with 4, 8 and 16 data in/outputs
- Double Data Rate architecture: two data transfers per clock cycle four internal banks for concurrent operation
- Programmable CAS Latency: 3, 4, 5 and 6
- Programmable Burst Length: 4 and 8
- Differential clock inputs (CK and $\overline{\text{CK}}$)
- Bi-directional, differential data strobes (DQS and $\overline{\text{DQS}}$) are transmitted / received with data. Edge aligned with read data and center-aligned with write data.
- DLL aligns DQ and DQS transitions with clock
- $\overline{\text{DQS}}$ can be disabled for single-ended data strobe operation
- Commands entered on each positive clock edge, data and data mask are referenced to both edges of DQS
- Data masks (DM) for write data
- Posted CAS by programmable additive latency for better command and data bus efficiency
- Off-Chip-Driver impedance adjustment (OCD) and On-Die-Termination (ODT) for better signal quality
- Auto-Precharge operation for read and write bursts
- Auto-Refresh, Self-Refresh and power saving Power-Down modes
- Average Refresh Period 7.8 µs at a T_{CASE} lower than 85 °C, 3.9 µs between 85 °C and 95 °C
- Programmable self refresh rate via EMRS2 setting
- Programmable partial array refresh via EMRS2 settings
- DCC enabling via EMRS2 setting
- Full and reduced Strength Data-Output Drivers
- 1K page size
- Packages: P(G)-TFBGA-60 for ×4 & ×8 components, P(G)-TFBGA-84 for ×16 components
- RoHS Compliant Products[1)]
- All Speed grades faster than DDR2–400 comply with DDR2–400 timing specifications when run at a clock rate of 200 MHz.

TABLE 1
Performance Tables for –25(F)

Product Type Speed Code			–25F	–2.5	Unit
Speed Grade			**DDR2–800D 5–5–5**	**DDR2–800E 6–6–6**	**—**
Max. Clock Frequency	@CL6	f_{CK6}	400	400	MHz
	@CL5	f_{CK5}	400	333	MHz
	@CL4	f_{CK4}	266	266	MHz
	@CL3	f_{CK3}	200	200	MHz
Min. RAS-CAS-Delay		t_{RCD}	12.5	15	ns
Min. Row Precharge Time		t_{RP}	12.5	15	ns
Min. Row Active Time		t_{RAS}	45	45	ns
Min. Row Cycle Time		t_{RC}	57.5	60	ns

1) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

TABLE 2
Performance Table for –3(S)

Product Type Speed Code			–3	–3S	Unit
Speed Grade			**DDR2–667C 4–4–4**	**DDR2–667D 5–5–5**	**—**
Max. Clock Frequency	@CL5	f_{CK5}	333	333	MHz
	@CL4	f_{CK4}	333	266	MHz
	@CL3	f_{CK3}	200	200	MHz
Min. RAS-CAS-Delay		t_{RCD}	12	15	ns
Min. Row Precharge Time		t_{RP}	12	15	ns
Min. Row Active Time		t_{RAS}	45	45	ns
Min. Row Cycle Time		t_{RC}	57	60	ns

TABLE 3
Performance table for –3.7

Product Type Speed Code			–3.7	Unit
Speed Grade			**DDR2–533C 4–4–4**	**—**
Max. Clock Frequency	@CL5	f_{CK5}	266	MHz
	@CL4	f_{CK4}	266	MHz
	@CL3	f_{CK3}	200	MHz
Min. RAS-CAS-Delay		t_{RCD}	15	ns
Min. Row Precharge Time		t_{RP}	15	ns
Min. Row Active Time		t_{RAS}	45	ns
Min. Row Cycle Time		t_{RC}	60	ns

TABLE 4
Performance Table for –5

Product Type Speed Code			–5	Units
Speed Grade			**DDR2–400B 3–3–3**	**—**
Max. Clock Frequency	@CL5	f_{CK5}	200	MHz
	@CL4	f_{CK4}	200	MHz
	@CL3	f_{CK3}	200	MHz
Min. RAS-CAS-Delay		t_{RCD}	15	ns
Min. Row Precharge Time		t_{RP}	15	ns
Min. Row Active Time		t_{RAS}	40	ns
Min. Row Cycle Time		t_{RC}	55	ns

1.2 Description

The 256-Mbit Double-Data-Rate-Two SDRAM is a high-speed CMOS Synchronous DRAM device containing 268,435,456 bits and internally configured as a quad-bank DRAM. The device is organized as either 16 Mbit × 4 I/O × 4 banks, 8 Mbit × 8 I/O × 4 banks or 4 Mbit ×16 I/O × 4 banks chip. These synchronous devices achieve high speed transfer rates starting at 400 Mb/sec/pin for general applications. See **Table 1** for performance figures.

The device is designed to comply with all DDR2 DRAM key features:

- Posted CAS with additive latency,
- Write latency = read latency - 1,
- Normal and weak strength data-output driver,
- Off-Chip Driver (OCD) impedance adjustment
- On-Die Termination (ODT) function.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and $\overline{\text{CK}}$ falling). All I/Os are synchronized with a single ended DQS or differential DQS-$\overline{\text{DQS}}$ pair in a source synchronous fashion.

A is used to convey row, column and bank address information in a RAS-CAS multiplexing style.

The DDR2 device operates with a 1.8 V ± 0.1 V power supply. An Auto-Refresh and Self-Refresh mode is provided along with various power-saving power-down modes.

The functionality described and the timing specifications included in this data sheet are for the DLL Enabled mode of operation.

The DDR2 SDRAM is available in P(G)-TFBGA-60 and P(G)-TFBGA-84 packages.

TABLE 5
Ordering Information for Lead-Free Products (RoHS Compliant)

Product Type	Org.	Speed	CAS-RCD-RP Latencies[1)]	Clock (MHz)	Package	Note
Standard Temperature Range (0 °C - +70 °C)						
HYB18T256400BF-25F	×4	DDR2-800D	5-5-5	400	PG-TFBGA-60	[2)] green Product
HYB18T256800BF-25F	×8	DDR2-800D	5-5-5	400	PG-TFBGA-60	
HYB18T256160BF-25F	×16	DDR2-800D	5-5-5	400	PG-TFBGA-84	
HYB18T256400BF-2.5	×4	DDR2-800E	6-6-6	400	PG-TFBGA-60	
HYB18T256800BF-2.5	×8	DDR2-800E	6-6-6	400	PG-TFBGA-60	
HYB18T256160BF-2.5	×16	DDR2-800E	6-6-6	400	PG-TFBGA-84	
HYB18T256400BF-3	×4	DDR2-667C	4-4-4	333	PG-TFBGA-60	
HYB18T256800BF-3	×8	DDR2-667C	4-4-4	333	PG-TFBGA-60	
HYB18T256160BF-3	×16	DDR2-667C	4-4-4	333	PG-TFBGA-84	
HYB18T256400BF-3S	×4	DDR2-667D	5-5-5	333	PG-TFBGA-60	
HYB18T256800BF-3S	×8	DDR2-667D	5-5-5	333	PG-TFBGA-60	
HYB18T256160BF-3S	×16	DDR2-667D	5-5-5	333	PG-TFBGA-84	
HYB18T256400BF-3.7	×4	DDR2-533C	4-4-4	266	PG-TFBGA-60	
HYB18T256800BF-3.7	×8	DDR2-533C	4-4-4	266	PG-TFBGA-60	
HYB18T256160BF-3.7	×16	DDR2-533C	4-4-4	266	PG-TFBGA-84	
HYB18T256400BFL-3.7	×4	DDR2-533C	4-4-4	266	PG-TFBGA-60	
HYB18T256800BFL-3.7	×8	DDR2-533C	4-4-4	266	PG-TFBGA-60	
HYB18T256160BFL-3.7	×16	DDR2-533C	4-4-4	266	PG-TFBGA-84	
HYB18T256400BF-5	×4	DDR2-400B	3-3-3	200	PG-TFBGA-60	
HYB18T256800BF-5	×8	DDR2-400B	3-3-3	200	PG-TFBGA-60	
HYB18T256160BF-5	×16	DDR2-400B	3-3-3	200	PG-TFBGA-84	

1) CAS: Column Address Strobe; RCD: Row Column Delay; RP: Row Precharge
2) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

TABLE 6
Ordering Information for Lead-Free Products (RoHS Compliant)

Product Type	Org.	Speed	CAS-RCD-RP Latencies[1]	Clock (MHz)	Package	Note
Industrial Temperature Range (–40 °C - +85 °C)						
HYI18T256400BF-25F	×4	DDR2-800D	5-5-5	400	PG-TFBGA-60	[2]
HYI18T256800BF-25F	×8	DDR2-800D	5-5-5	400	PG-TFBGA-60	
HYI18T256160BF-25F	×16	DDR2-800D	5-5-5	400	PG-TFBGA-84	
HYI18T256400BF-2.5	×4	DDR2-800E	6-6-6	400	PG-TFBGA-60	
HYI18T256800BF-2.5	×8	DDR2-800E	6-6-6	400	PG-TFBGA-60	
HYI18T256160BF-2.5	×16	DDR2-800E	6-6-6	400	PG-TFBGA-84	
HYI18T256400BF-3	×4	DDR2-667C	4-4-4	333	PG-TFBGA-60	
HYI18T256800BF-3	×8	DDR2-667C	4-4-4	333	PG-TFBGA-60	
HYI18T256160BF-3	×16	DDR2-667C	4-4-4	333	PG-TFBGA-84	
HYI18T256400BF-3S	×4	DDR2-667D	5-5-5	333	PG-TFBGA-60	
HYI18T256800BF-3S	×8	DDR2-667D	5-5-5	333	PG-TFBGA-60	
HYI18T256160BF-3S	×16	DDR2-667D	5-5-5	333	PG-TFBGA-84	
HYI18T256400BF-3.7	×4	DDR2-533C	4-4-4	266	PG-TFBGA-60	
HYI18T256800BF-3.7	×8	DDR2-533C	4-4-4	266	PG-TFBGA-60	
HYI18T256160BF-3.7	×16	DDR2-533C	4-4-4	266	PG-TFBGA-84	
HYI18T256400BF-5	×4	DDR2-400B	3-3-3	200	PG-TFBGA-60	
HYI18T256800BF-5	×8	DDR2-400B	3-3-3	200	PG-TFBGA-60	
HYI18T256160BF-5	×16	DDR2-400B	3-3-3	200	PG-TFBGA-84	

1) CAS: Column Address Strobe; RCD: Row Column Delay; RP: Row Precharge

2) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

TABLE 7
Ordering Information for Lead-Containing Products

Product Type	Org.	Speed	CAS-RCD-RP Latencies[1)]	Clock (MHz)	Package
Standard Temperature Range (0 °C - +70 °C)					
HYB18T256400BC-25F	×4	DDR2-800D	5-5-5	400	P-TFBGA-60
HYB18T256800BC-25F	×8	DDR2-800D	5-5-5	400	P-TFBGA-60
HYB18T256160BC-25F	×16	DDR2-800D	5-5-5	400	P-TFBGA-84
HYB18T256400BC-2.5	×4	DDR2-800E	6-6-6	400	P-TFBGA-60
HYB18T256800BC-2.5	×8	DDR2-800E	6-6-6	400	P-TFBGA-60
HYB18T256160BC-2.5	×16	DDR2-800E	6-6-6	400	P-TFBGA-84
HYB18T256400BC-3	×4	DDR2-667C	4-4-4	333	P-TFBGA-60
HYB18T256800BC-3	×8	DDR2-667C	4-4-4	333	P-TFBGA-60
HYB18T256160BC-3	×16	DDR2-667C	4-4-4	333	P-TFBGA-84
HYB18T256400BC-3S	×4	DDR2-667D	5-5-5	333	P-TFBGA-60
HYB18T256800BC-3S	×8	DDR2-667D	5-5-5	333	P-TFBGA-60
HYB18T256160BC-3S	×16	DDR2-667D	5-5-5	333	P-TFBGA-84
HYB18T256400BC-3.7	×4	DDR2-533C	4-4-4	266	P-TFBGA-60
HYB18T256800BC-3.7	×8	DDR2-533C	4-4-4	266	P-TFBGA-60
HYB18T256160BC-3.7	×16	DDR2-533C	4-4-4	266	P-TFBGA-84
HYB18T256400BC-5	×4	DDR2-400B	3-3-3	200	P-TFBGA-60
HYB18T256800BC-5	×8	DDR2-400B	3-3-3	200	P-TFBGA-60
HYB18T256160BC-5	×16	DDR2-400B	3-3-3	200	P-TFBGA-84

1) CAS: Column Address Strobe; RCD: Row Column Delay; RP: Row Precharge

TABLE 8
Ordering Information for Lead-Containing Products

Product Type	Org.	Speed	CAS-RCD-RP Latencies[1)]	Clock (MHz)	Package
Industrial Temperature Range (–40 °C - +85 °C)					
HYI18T256400BC-25F	×4	DDR2-800D	5-5-5	400	P-TFBGA-60
HYI18T256800BC-25F	×8	DDR2-800D	5-5-5	400	P-TFBGA-60
HYI18T256160BC-25F	×16	DDR2-800D	5-5-5	400	P-TFBGA-84
HYI18T256400BC-2.5	×4	DDR2-800E	6-6-6	400	P-TFBGA-60
HYI18T256800BC-2.5	×8	DDR2-800E	6-6-6	400	P-TFBGA-60
HYI18T256160BC-2.5	×16	DDR2-800E	6-6-6	400	P-TFBGA-84
HYI18T256400BC-3	×4	DDR2-667C	4-4-4	333	P-TFBGA-60
HYI18T256800BC-3	×8	DDR2-667C	4-4-4	333	P-TFBGA-60
HYI18T256160BC-3	×16	DDR2-667C	4-4-4	333	P-TFBGA-84
HYI18T256400BC-3S	×4	DDR2-667D	5-5-5	333	P-TFBGA-60
HYI18T256800BC-3S	×8	DDR2-667D	5-5-5	333	P-TFBGA-60
HYI18T256160BC-3S	×16	DDR2-667D	5-5-5	333	P-TFBGA-84
HYI18T256400BC-3.7	×4	DDR2-533C	4-4-4	266	P-TFBGA-60
HYI18T256800BC-3.7	×8	DDR2-533C	4-4-4	266	P-TFBGA-60
HYI18T256160BC-3.7	×16	DDR2-533C	4-4-4	266	P-TFBGA-84
HYI18T256400BC-5	×4	DDR2-400B	3-3-3	200	P-TFBGA-60
HYI18T256800BC-5	×8	DDR2-400B	3-3-3	200	P-TFBGA-60
HYI18T256160BC-5	×16	DDR2-400B	3-3-3	200	P-TFBGA-84

1) CAS: Column Address Strobe; RCD: Row Column Delay; RP: Row Precharge

Note: For product nomenclature see ***Chapter 9*** *of this data sheet*

2 Configuration

This chapter contains the chip configuration, addressing and block diagrams.

2.1 Chip Configuration for PG-TFBGA-60

The chip configuration of a DDR2 SDRAM is listed by function in **Table 9**. The abbreviations used in the Ball# columns are explained in **Table 10** and **Table 11** respectively. The ball numbering for the FBGA package is depicted in figures.

TABLE 9
Chip Configuration of DDR2 SDRAM

Ball#	Name	Ball Type	Buffer Type	Function
Clock Signals ×4×8 organization				
E8	CK	I	SSTL	**Clock Signal CK, Complementary Clock Signal CK**
F8	$\overline{\text{CK}}$	I	SSTL	
F2	CKE	I	SSTL	**Clock Enable**
Control Signals ×4×8 organizations				
F7	$\overline{\text{RAS}}$	I	SSTL	**Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)**
G7	$\overline{\text{CAS}}$	I	SSTL	
F3	$\overline{\text{WE}}$	I	SSTL	
G8	$\overline{\text{CS}}$	I	SSTL	**Chip Select**
Address Signals ×4×8 organizations				
G2	BA0	I	SSTL	**Bank Address Bus 1:0**
G3	BA1	I	SSTL	
H8	A0	I	SSTL	**Address Signal 12:0, Address Signal 10/Autoprecharge**
H3	A1	I	SSTL	
H7	A2	I	SSTL	
J2	A3	I	SSTL	
J8	A4	I	SSTL	
J3	A5	I	SSTL	
J7	A6	I	SSTL	
K2	A7	I	SSTL	
K8	A8	I	SSTL	
K3	A9	I	SSTL	
H2	A10	I	SSTL	
	AP	I	SSTL	
K7	A11	I	SSTL	
L2	A12	I	SSTL	

Ball#	Name	Ball Type	Buffer Type	Function
L8	A13	I	SSTL	**Address Signal 13**
	NC	–	–	*Note: 256 Mbit components and*
Data Signals ×4×8 organization				
C8	DQ0	I/O	SSTL	**Data Signal 3:0**
C2	DQ1	I/O	SSTL	
D7	DQ2	I/O	SSTL	
D3	DQ3	I/O	SSTL	
D1	DQ4	I/O	SSTL	**Data Signal 7:4**
D9	DQ5	I/O	SSTL	
B1	DQ6	I/O	SSTL	
B9	DQ7	I/O	SSTL	
Data Strobe×4×8 organizations				
B7	DQS	I/O	SSTL	**Data Strobe**
A8	$\overline{\text{DQS}}$	I/O	SSTL	
Data Strobe ×8 organisation				
B3	RDQS	O	SSTL	**Read Data Strobe**
A2	$\overline{\text{RDQS}}$	O	SSTL	
Data Mask ×4×8 organizations				
B3	DM	I	SSTL	**Data Mask**
Power Supplies ×4×8 organization				
A9,C1,C3,C7,C9	V_{DDQ}	PWR	–	**I/O Driver Power Supply**
A1	V_{DD}	PWR	–	**Power Supply**
A7,B2,B8,D2,D8	V_{SSQ}	PWR	–	**I/O Driver Power Supply**
A3,E3	V_{SS}	PWR	–	**Power Supply**
Power Supplies ×4×8 organizations				
E2	V_{REF}	AI	–	**I/O Reference Voltage**
E1	V_{DDL}	PWR	–	**Power Supply**
E9,H9,L1	V_{DD}	PWR	–	**Power Supply**
E7	V_{SSDL}	PWR	–	**Power Supply**
J1,K9	V_{SS}	PWR	–	**Power Supply**
Not Connected ×4×8 organization				
G1, L3,L7, L8	NC	NC	–	**Not Connected**
Not Connected ×4 organization				
A2, B1, B9, D1, D9	NC	NC	–	**Not Connected**
Other Balls ×4×8 organizations				
F9	ODT	I	SSTL	**On-Die Termination Control**

TABLE 10
Abbreviations for Ball Type

Abbreviation	Description
I	Standard input-only ball. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

TABLE 11
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding ball has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

FIGURE 1
Chip Configuration for ×4 components, PG-TFBGA-60 (top view)

1	2	3	4	5	6	7	8	9
V_{DD}	NC	V_{SS}		A		V_{SSQ}	$\overline{DQS}$	V_{DDQ}
NC	V_{SSQ}	DM		B		DQS	V_{SSQ}	NC
V_{DDQ}	DQ1	V_{DDQ}		C		V_{DDQ}	DQ0	V_{DDQ}
NC	V_{SSQ}	DQ3		D		DQ2	V_{SSQ}	NC
V_{DDL}	V_{REF}	V_{SS}		E		V_{SSDL}	CK	V_{DD}
	CKE	$\overline{WE}$		F		$\overline{RAS}$	$\overline{CK}$	ODT
NC	BA0	BA1		G		$\overline{CAS}$	$\overline{CS}$	
	A10/AP	A1		H		A2	A0	V_{DD}
V_{SS}	A3	A5		J		A6	A4	
	A7	A9		K		A11	A8	V_{SS}
V_{DD}	A12	NC		L		NC	NC,A13	

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Notes

1. *V_{DDL} and V_{SSDL} are power and ground for the DLL. V_{DDL} is connected to V_{DD} on the device. V_{DD}, V_{DDQ}, V_{SSDL}, V_{SS}, and V_{SSQ} are isolated on the device.*
2. *Ball position L8 is A13 for 512-Mbit and is Not Connected on 256-Mbit*

FIGURE 2
Chip Configuration for ×8 components, PG-TFBGA-60 (top view)

	1	2	3	4	5	6	7	8	9
A	V_{DD}	NC/$\overline{RDQS}$	V_{SS}				V_{SSQ}	$\overline{DQS}$	V_{DDQ}
B	DQ6	V_{SSQ}	DM/RDQS				DQS	V_{SSQ}	DQ7
C	V_{DDQ}	DQ1	V_{DDQ}				V_{DDQ}	DQ0	V_{DDQ}
D	DQ4	V_{SSQ}	DQ3				DQ2	V_{SSQ}	DQ5
E	V_{DDL}	V_{REF}	V_{SS}				V_{SSDL}	CK	V_{DD}
F		CKE	$\overline{WE}$				$\overline{RAS}$	$\overline{CK}$	ODT
G	NC	BA0	BA1				$\overline{CAS}$	$\overline{CS}$	
H		A10/AP	A1				A2	A0	V_{DD}
J	V_{SS}	A3	A5				A6	A4	
K		A7	A9				A11	A8	V_{SS}
L	V_{DD}	A12	NC				NC	NC, A13	

MPPT0560

Notes

1. *RDQS / $\overline{RDQS}$ are enabled by EMRS(1) command.*
2. *If RDQS / $\overline{RDQS}$ is enabled, the DM function is disabled*
3. *When enabled, RDQS & $\overline{RDQS}$ are used as strobe signals during reads.*
4. *V_{DDL} and V_{SSDL} are power and ground for the DLL. V_{DDL} is connected to V_{DD} on the device. V_{DD}, V_{DDQ}, V_{SSDL}, V_{SS}, and V_{SSQ} are isolated on the device.*
5. *Ball position L8 is A13 for 512-Mbit and is Not Connected on 256-Mbit.*

2.2 Chip Configuration for P(G)-TFBGA-84

The chip configuration of a DDR2 SDRAM is listed by function in **Table 9**. The abbreviations used in the Ball# Type columns are explained in **Table 10** and **Table 11** respectively.

TABLE 12
Chip Configuration of DDR SDRAM

Ball#	Name	Ball Type	Buffer Type	Function
Clock Signals ×16 Organization				
J8	CK	I	SSTL	**Clock Signal CK, $\overline{CK}$**
K8	$\overline{CK}$	I	SSTL	
K2	CKE	I	SSTL	**Clock Enable**
Control Signals ×16 Organization				
K7	$\overline{RAS}$	I	SSTL	**Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)**
L7	$\overline{CAS}$	I	SSTL	
K3	$\overline{WE}$	I	SSTL	
L8	$\overline{CS}$	I	SSTL	**Chip Select**
Address Signals ×16 Organization				
L2	BA0	I	SSTL	**Bank Address Bus 1:0**
L3	BA1	I	SSTL	
M8	A0	I	SSTL	**Address Signal 12:0,Address Signal 10/Autoprecharge**
M3	A1	I	SSTL	
M7	A2	I	SSTL	
N2	A3	I	SSTL	
N8	A4	I	SSTL	
N3	A5	I	SSTL	
N7	A6	I	SSTL	
P2	A7	I	SSTL	
P8	A8	I	SSTL	
P3	A9	I	SSTL	
M2	A10	I	SSTL	
	AP	I	SSTL	
P7	A11	I	SSTL	
R2	A12	I	SSTL	
Data Signals ×16 Organization				
G8	DQ0	I/O	SSTL	**Data Signal 15:0**
G2	DQ1	I/O	SSTL	
H7	DQ2	I/O	SSTL	
H3	DQ3	I/O	SSTL	
H1	DQ4	I/O	SSTL	
H9	DQ5	I/O	SSTL	
F1	DQ6	I/O	SSTL	

Ball#	Name	Ball Type	Buffer Type	Function
F9	DQ7	I/O	SSTL	**Data Signal 15:0**
C8	DQ8	I/O	SSTL	
C2	DQ9	I/O	SSTL	
D7	DQ10	I/O	SSTL	
D3	DQ11	I/O	SSTL	
D1	DQ12	I/O	SSTL	
D9	DQ13	I/O	SSTL	
B1	DQ14	I/O	SSTL	
B9	DQ15	I/O	SSTL	
Data Strobe ×16 Organization				
B7	UDQS	I/O	SSTL	**Data Strobe Upper Byte**
A8	$\overline{\text{UDQS}}$	I/O	SSTL	
F7	LDQS	I/O	SSTL	**Data Strobe Lower Byte**
E8	$\overline{\text{LDQS}}$	I/O	SSTL	
Data Mask ×16 Organization				
B3	UDM	I	SSTL	**Data Mask Upper Byte**
F3	LDM	I	SSTL	**Data Mask Lower Byte**
Power Supplies ×16 Organization				
J2	V_{REF}	AI	–	**I/O Reference Voltage**
C1, C3, C7, C9, E9, G1, G3, G7, G9	V_{DDQ}	PWR	–	**I/O Driver Power Supply**
J1	V_{DDL}	PWR	–	**Power Supply**
A1, E1, J9, M9, R1	V_{DD}	PWR	–	**Power Supply**
A7, A9, D2, D8, E7, F2, F8, H2, H8	V_{SSQ}	PWR	–	**Power Supply**
J7	V_{SSDL}	PWR	–	**Power Supply**
A3, E3, J3, N1, P9	V_{SS}	PWR	–	**Power Supply**
Not Connected ×16 Organization				
A2, E2, L1, R3, R7, R8	NC	NC	–	**Not Connected**
Other Balls ×16 Organization				
K9	ODT	I	SSTL	**On-Die Termination Control**

TABLE 13
Abbreviations for Ball Type

Abbreviation	Description
I	Standard input-only ball. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
PWR	Power
GND	Ground
NC	Not Connected

TABLE 14
Abbreviations for Buffer Type

Abbreviation	Description
SSTL	Serial Stub Terminated Logic (SSTL_18)
LV-CMOS	Low Voltage CMOS
CMOS	CMOS Levels
OD	Open Drain. The corresponding ball has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR.

FIGURE 3
Ball Configuration for ×16 components, PG-TFBGA-84 (top view)

1	2	3	4	5	6	7	8	9
V_{DD}	NC	V_{SS}		A		V_{SSQ}	$\overline{UDQS}$	V_{DDQ}
DQ14	V_{SSQ}	UDM		B		UDQS	V_{SSQ}	DQ15
V_{DDQ}	DQ9	V_{DDQ}		C		V_{DDQ}	DQ8	V_{DDQ}
DQ12	V_{SSQ}	DQ11		D		DQ10	V_{SSQ}	DQ13
V_{DD}	NC	V_{SS}		E		V_{SSQ}	$\overline{LDQS}$	V_{DDQ}
DQ6	V_{SSQ}	LDM		F		LDQS	V_{SSQ}	DQ7
V_{DDQ}	DQ1	V_{DDQ}		G		V_{DDQ}	DQ0	V_{DDQ}
DQ4	V_{SSQ}	DQ3		H		DQ2	V_{SSQ}	DQ5
V_{DDL}	V_{REF}	V_{SS}		J		VSSDL	CK	V_{DD}
	CKE	$\overline{WE}$		K		$\overline{RAS}$	$\overline{CK}$	ODT
NC	BA0	BA1		L		$\overline{CAS}$	$\overline{CS}$	
	A10/AP	A1		M		A2	A0	V_{DD}
V_{SS}	A3	A5		N		A6	A4	
	A7	A9		P		A11	A8	V_{SS}
V_{DD}	A12	NC		R		NC	NC	

MPPT0120

Notes

1. *UDQS/$\overline{UDQS}$ is data strobe for DQ[15:8], LDQS/$\overline{LDQS}$ is data strobe for DQ[7:0]*
2. *LDM is the data mask signal for DQ[7:0], UDM is the data mask signal for DQ[15:8]*
3. *V_{DDL} and V_{SSDL} are power and ground for the DLL. V_{DDL} is connected to V_{DD} on the device. V_{DD}, V_{DDQ}, V_{SSDL}, V_{SS}, and V_{SSQ} are isolated on the device.*

2.3 256-Mbit DDR2 Addressing

This chapter describes the 256-Mbit DDR2 addressing.

TABLE 15
DDR2 Addressing for ×4 Organization

Configuration	64Mb x 4[1]	Note
Bank Address	BA[1:0]	
Number of Banks	4	
Auto-Precharge	A10 / AP	
Row Address	A[12:0]	
Column Address	A11, A[9:0]	
Number of Column Address Bits	11	2)
Number of I/Os	4	
Page Size [Bytes]	1024 (1K)	3)

1) Referred to as 'org'
2) Referred to as 'colbits'
3) PageSize = $2^{colbits} \times$ org/8 [Bytes]

TABLE 16
DDR2 Addressing for ×8 Organization

Configuration	32Mb x 8[1]	Note
Bank Address	BA[1:0]	
Number of Banks	4	
Auto-Precharge	A10 / AP	
Row Address	A[12:0]	
Column Address	A[9:0]	
Number of Column Address Bits	10	2)
Number of I/Os	8	
Page Size [Bytes]	1024 (1K)	3)

1) Referred to as 'org'
2) Referred to as 'colbits'
3) PageSize = $2^{colbits} \times$ org/8 [Bytes]

TABLE 17
DDR2 Addressing for ×16 Organization

Configuration	16Mb x 16[1]	Note
Bank Address	BA[1:0]	
Number of Banks	4	
Auto-Precharge	A10 / AP	
Row Address	A[12:0]	

Configuration	16Mb x 16[1]	Note
Column Address	A[8:0]	
Number of Column Address Bits	9	[2]
Number of I/Os	16	
Page Size [Bytes]	1024 (1K)	[3]

1) Referred to as 'org'
2) Referred to as 'colbits'
3) PageSize = $2^{colbits} \times$ org/8 [Bytes]

3 Functional Description

This chapter contains the functional description.

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	PD		WR		DLL	TM		CL		BT		BL	
	reg. addr			w		w		w	w		w		w		w	

MPBT0410

TABLE 18
Mode Register Definition (BA[2:0] = 000_B)

Field	Bits	Type[1)]	Description
BA2	16	reg. addr.	**Bank Address [2]** *Note: BA2 not available on 256 Mbit and 512 Mbit components* 0_B **BA2** Bank Address
BA1	15		**Bank Address [1]** 0_B **BA1** Bank Address
BA0	14		**Bank Address [0]** 0_B **BA0** Bank Address
A13	13		**Address Bus[13]** *Note: A13 is not available for 256 Mbit and x16 512 Mbit configuration* 0_B **A13** Address bit 13
PD	12	w	**Active Power-Down Mode Select** 0_B **PD** Fast exit 1_B **PD** Slow exit
WR	[11:9]	w	**Write Recovery**[2)] *Note: All other bit combinations are illegal.* 001_B **WR** 2 010_B **WR** 3 011_B **WR** 4 100_B **WR** 5 101_B **WR** 6
DLL	8	w	**DLL Reset** 0_B **DLL** No 1_B **DLL** Yes
TM	7	w	**Test Mode** 0_B **TM** Normal Mode 1_B **TM** Vendor specific test mode

Field	Bits	Type[1]	Description
CL	[6:4]	w	**CAS Latency** *Note: All other bit combinations are illegal.* 011_B **CL** 3 100_B **CL** 4 101_B **CL** 5 110_B **CL** 6 111_B **CL** 7
BT	3	w	**Burst Type** 0_B **BT** Sequential 1_B **BT** Interleaved
BL	[2:0]	w	**Burst Length** *Note: All other bit combinations are illegal.* 010_B **BL** 4 011_B **BL** 8

1) w = write only register bits
2) Number of clock cycles for write recovery during auto-precharge. WR in clock cycles is calculated by dividing t_{WR} (in ns) by t_{CK} (in ns) and rounding up to the next integer: WR [cycles] $\geq t_{WR}$ (ns) / t_{CK} (ns). The mode register must be programmed to fulfill the minimum requirement for the analogue t_{WR} timing WR_{MIN} is determined by $t_{CK.MAX}$ and WR_{MAX} is determined by $t_{CK.MIN}$.

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	1	0	Q_{off}	RDQS	$\overline{DQS}$	OCD Program			R_{tt}	AL			R_{tt}	DIC	DLL
	reg. addr				w	w		w		w		w		w	w	w

MPBT0380

TABLE 19
Extended Mode Register Definition (BA[2:0] = 001_B)

Field	Bits	Type[1]	Description
BA2	16	reg. addr.	**Bank Address [2]** *Note: BA2 not available on 256 Mbit and 512 Mbit components* 0_B **BA2** Bank Address
BA1	15		**Bank Address [1]** 0_B **BA1** Bank Address
BA0	14		**Bank Address [0]** 1_B **BA0** Bank Address
A13	13	w	**Address Bus [13]** *Note: A13 is not available for 256 Mbit and x16 512 Mbit configuration* 0_B **A13** Address bit 13
Qoff	12	w	**Output Disable** 0_B **QOff** Output buffers enabled 1_B **QOff** Output buffers disabled

Field	Bits	Type[1)]	Description
RDQS	11	w	**Read Data Strobe Output (RDQS, $\overline{\text{RDQS}}$)** 0_B **RDQS** Disable 1_B **RDQS** Enable
$\overline{\text{DQS}}$	10	w	**Complement Data Strobe (DQS Output)** 0_B $\overline{\text{DQS}}$ Enable 1_B $\overline{\text{DQS}}$ Disable
OCD Program	[9:7]	w	**Off-Chip Driver Calibration Program** 000_B **OCD** OCD calibration mode exit, maintain setting 001_B **OCD** Drive (1) 010_B **OCD** Drive (0) 100_B **OCD** Adjust mode 111_B **OCD** OCD calibration default
AL	[5:3]	w	**Additive Latency** *Note: All other bit combinations are illegal.* 000_B **AL** 0 001_B **AL** 1 010_B **AL** 2 011_B **AL** 3 100_B **AL** 4 101_B **AL** 5
R_{TT}	6,2	w	**Nominal Termination Resistance of ODT** *Note: See* ***Table 30 "ODT DC Electrical Characteristics" on Page 31*** 00_B **RTT** ∞ (ODT disabled) 01_B **RTT** 75 Ohm 10_B **RTT** 150 Ohm 11_B **RTT** 50 Ohm
DIC	1	w	**Off-chip Driver Impedance Control** 0_B **DIC** Full (Driver Size = 100%) 1_B **DIC** Reduced
DLL	0	w	**DLL Enable** 0_B **DLL** Enable 1_B **DLL** Disable

1) w = write only register bits

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	0						SRF	0			DCC	PASR		

reg. addr

MPBT0520

TABLE 20
EMRS(2) Programming Extended Mode Register Definition (BA[2:0]=010_B)

Field	Bits	Type[1]	Description
BA2	16	w	**Bank Address** *Note: BA2 is not available on 256 Mbit and 512 Mbit components* 0_B **BA2** Bank Address
BA	[15:14]	w	**Bank Adress** 00_B **BA** MRS 01_B **BA** EMRS(1) 10_B **BA** EMRS(2) 11_B **BA** EMRS(3): Reserved
A	[13:8]	w	**Address Bus** *Note: A13 is not available for 256 Mbit and x16 512 Mbit configuration* 000000_B **A** Address bits
SRF	7	w	**Address Bus, High Temperature Self Refresh Rate for T_{CASE} > 85°C** 0_B **A7** disable 1_B **A7** enable [2]
A	[6:4]	w	**Address Bus** 000_B **A** Address bits
DCC	3	w	**Address Bus, Duty Cycle Correction (DCC)** 0_B **A3** DCC disabled 1_B **A3** DCC enabled
Partial Self Refresh for 4 banks			
PASR	[2:0]	w	**Address Bus, Partial Array Self Refresh for 4 Banks**[3] *Note: Only for 256 Mbit and 512 Mbit components* 000_B **PASR0** Full Array 001_B **PASR1** Half Array (BA[1:0]=00, 01) 010_B **PASR2** Quarter Array (BA[1:0]=00) 011_B **PASR3** Not defined 100_B **PASR4** 3/4 array (BA[1:0]=01, 10, 11) 101_B **PASR5** Half array (BA[1:0]=10, 11) 110_B **PASR6** Quarter array (BA[1:0]=11) 111_B **PASR7** Not defined

Field	Bits	Type[1)]	Description
Partial Self Refresh for 8 banks			
PASR	[2:0]	w	**Address Bus, Partial Array Self Refresh for 8 Banks**[3)] *Note: Only for 1G and 2G components* 000_B **PASR0** Full Array 001_B **PASR1** Half Array (BA[2:0]=000, 001, 010 & 011) 010_B **PASR2** Quarter Array (BA[2:0]=000, 001) 011_B **PASR3** 1/8 array (BA[2:0] = 000) 100_B **PASR4** 3/4 array (BA[2:0]= 010, 011, 100, 101, 110 & 111) 101_B **PASR5** Half array (BA[2:0]=100, 101, 110 & 111) 110_B **PASR6** Quarter array (BA[2:0]= 110 & 111) 111_B **PASR7** 1/8 array(BA[2:0]=111)

1) w = write only
2) When DRAM is operated at 85°C ≤ T_{Case} ≤ 95°C the extended self refresh rate must be enabled by setting bit A7 to "1" before the self refresh mode can be entered.
3) If PASR (Partial Array Self Refresh) is enabled, data located in areas of the array beyond the specified location will be lost if self refresh is entered. Data integrity will be maintained if t_{REF} conditions are met and no Self Refresh command is issued

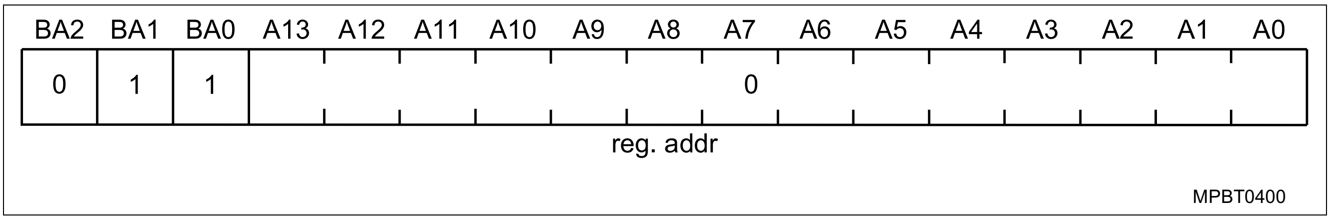


TABLE 21
EMR(3) Programming Extended Mode Register Definition(BA[2:0]=011_B)

Field	Bits	Type[1)]	Description
BA2	16	reg.addr	**Bank Address[2]** *Note: BA2 is not available on 256Mbit and 512Mbit components* 0_B **BA2** Bank Address
BA1	15		**Bank Adress[1]** 1_B **BA1** Bank Address
BA0	14		**Bank Adress[0]** 1_B **BA0** Bank Address
A	[13:0]	w	**Address Bus[13:0]** *Note: A13 is not available for 256 Mbit and x16 512 Mbit configuration* 00000000000000_B**A[13:0]** Address bits

1) w = write only

TABLE 22
ODT Truth Table

Input Pin	EMRS(1) Address Bit A10	EMRS(1) Address Bit A11
×4 Components		
DQ[3:0]	X	
DQS	X	
$\overline{\text{DQS}}$	0	X
DM	X	
×8 Components		
DQ[7:0]	X	
DQS	X	
$\overline{\text{DQS}}$	0	X
RDQS	X	1
$\overline{\text{RDQS}}$	0	1
DM	X	0
×16 Components		
DQ[7:0]	X	
DQ[15:8]	X	
LDQS	X	
$\overline{\text{LDQS}}$	0	X
UDQS	X	
$\overline{\text{UDQS}}$	0	X
LDM	X	
UDM	X	

TABLE 23
Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	× 0 0	0, 1, 2, 3	0, 1, 2, 3
	× 0 1	1, 2, 3, 0	1, 0, 3, 2
	×1 0	2, 3, 0, 1	2, 3, 0, 1
	×1 1	3, 0, 1, 2	3, 2, 1, 0
8	0 0 0	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	0 0 1	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	0 1 0	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	0 1 1	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	1 0 0	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	1 0 1	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	1 1 0	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	1 1 1	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

4 Truth Tables

The truth tables in this chapter summarize the commands and there signal coding to control a standard Double-Data-Rate-Two SDRAM.

TABLE 24
Command Truth Table

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1	A[12:11]	A10	A[9:0]	Note1)2)3)
	Previous Cycle	Current Cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			4)5)
Auto-Refresh	H	H	L	L	L	H	X	X	X	X	4)
Self-Refresh Entry	H	L	L	L	L	H	X	X	X	X	4)6)
Self-Refresh Exit	L	H	H	X	X	X	X	X	X	X	4)6)7)
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	4)5)
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	4)
Bank Activate	H	H	L	L	H	H	BA	Row Address			4)5)
Write	H	H	L	H	L	L	BA	Column	L	Column	4)5)8)
Write with Auto-Precharge	H	H	L	H	L	L	BA	Column	H	Column	4)5)8)
Read	H	H	L	H	L	H	BA	Column	L	Column	4)5)8)
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	4)5)8)
No Operation	H	X	L	H	H	H	X	X	X	X	4)
Device Deselect	H	X	H	X	X	X	X	X	X	X	4)
Power Down Entry	H	L	H	X	X	X	X	X	X	X	4)9)
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	4)9)
			L	H	H	H					

1) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
2) “X” means “H or L (but a defined logic level)”.
3) Operation that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
4) All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{WE}$, $\overline{RAS}$, $\overline{CAS}$, and CKE at the rising edge of the clock.
5) Bank addresses BA[1:0] determine which bank is to be operated upon. For (E)MRS BA[1:0] selects an (Extended) Mode Register.
6) V_{REF} must be maintained during Self Refresh operation.
7) Self Refresh Exit is asynchronous.
8) Burst reads or writes at BL = 4 cannot be terminated.
9) The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements.

TABLE 25
Clock Enable (CKE) Truth Table for Synchronous Transitions

Current State[1]	CKE		Command (N)[2] [3] RAS, CAS, WE	Action (N)[2]	Note[4][5]
	Previous Cycle[6] (N-1)	Current Cycle[6] (N)			
Power-Down	L	L	X	Maintain Power-Down	7)8)11)
	L	H	DESELECT or NOP	Power-Down Exit	7)9)10)11)
Self Refresh	L	L	X	Maintain Self Refresh	8)11)12)
	L	H	DESELECT or NOP	Self Refresh Exit	9)11)12)13)14)
Bank(s) Active	H	L	DESELECT or NOP	Active Power-Down Entry	7)9)10)11)15)
All Banks Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	9)10)11)15)
	H	L	AUTOREFRESH	Self Refresh Entry	7)11)14)16)
Any State other than listed above	H	H	Refer to the Command Truth Table		17)

1) Current state is the state of the DDR2 SDRAM immediately prior to clock edge N.
2) Command (N) is the command registered at clock edge N, and Action (N) is a result of Command (N)
3) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
4) CKE must be maintained HIGH while the device is in OCD calibration mode.
5) Operation that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
6) CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
7) The Power-Down Mode does not perform any refresh operations. The duration of Power-Down Mode is therefor limited by the refresh requirements
8) "X" means "don't care (including floating around V_{REF})" in Self Refresh and Power Down. However ODT must be driven HIGH or LOW in Power Down if the ODT function is enabled (Bit A2 or A6 set to "1" in EMRS(1)).
9) All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
10) Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.
11) $t_{CKE.MIN}$ of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of $t_{IS} + 2 \times t_{CK} + t_{IH}$.
12) V_{REF} must be maintained during Self Refresh operation.
13) On Self Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the t_{XSNR} period. Read commands may be issued only after t_{XSRD} (200 clocks) is satisfied.
14) Valid commands for Self Refresh Exit are NOP and DESELCT only.
15) Power-Down and Self Refresh can not be entered while Read or Write operations, (Extended) mode Register operations, Precharge or Refresh operations are in progress.
16) Self Refresh mode can only be entered from the All Banks Idle state.
17) Must be a legal command as defined in the Command Truth Table.

TABLE 26
Data Mask (DM) Truth Table

Name (Function)	DM	DQs	Note
Write Enable	L	Valid	1)
Write Inhibit	H	X	1)

1) Used to mask write data; provided coincident with the corresponding data.

5 Electrical Characteristics

This chapter describes the electrical characteristics.

5.1 Absolute Maximum Ratings

Caution is needed not to exceed absolute maximum ratings of the DRAM device listed in **Table 27** at any time.

TABLE 27
Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit	Note
		Min.	Max.		
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	–1.0	+2.3	V	1)
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	–0.5	+2.3	V	1)2)
V_{DDL}	Voltage on V_{DDL} pin relative to V_{SS}	–0.5	+2.3	V	1)2)
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.5	+2.3	V	1)
T_{STG}	Storage Temperature	–55	+100	°C	1)2)

1) When V_{DD} and V_{DDQ} and V_{DDL} are less than 500 mV; V_{REF} may be equal to or less than 300 mV.
2) Storage Temperature is the case surface temperature on the center/top side of the DRAM.

***Attention:** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

TABLE 28
DRAM Component Operating Temperature Range

Symbol	Parameter	Rating		Unit	Notes
		Min.	Max.		
T_{OPER}	Operating Temperature	0	95	°C	1)2)3)4) for HYB...
		–40	85	°C	for HYI...

1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
2) The operating temperature range are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C for standard products (HYB.....) and -40 - +85 for industrial temperature range products (HYI.....) under all other specification parameters.
3) Above 85 °C the Auto-Refresh command interval has to be reduced to t_{REFI}= 3.9 µs
4) When operating this product in the 85 °C to 95 °C TCASE temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to "1". When the High Temperature Self Refresh is enabled there is an increase of I_{DD6} by approximately 50%

5.2 DC Characteristics

TABLE 29
Recommended DC Operating Conditions (SSTL_18)

Symbol	Parameter	Rating			Unit	Note
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.7	1.8	1.9	V	1)
V_{DDDL}	Supply Voltage for DLL	1.7	1.8	1.9	V	1)
V_{DDQ}	Supply Voltage for Output	1.7	1.8	1.9	V	1)
V_{REF}	Input Reference Voltage	$0.49 \times V_{DDQ}$	$0.5 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V	2)3)
V_{TT}	Termination Voltage	$V_{REF} - 0.04$	V_{REF}	$V_{REF} + 0.04$	V	4)

1) V_{DDQ} tracks with V_{DD}, V_{DDDL} tracks with V_{DD}. AC parameters are measured with V_{DD}, V_{DDQ} and V_{DDDL} tied together.
2) The value of V_{REF} may be selected by the user to provide optimum noise margin in the system. Typically the value of V_{REF} is expected to be about $0.5 \times V_{DDQ}$ of the transmitting device and V_{REF} is expected to track variations in V_{DDQ}.
3) Peak to peak ac noise on V_{REF} may not exceed $\pm$ 2% V_{REF} (dc)
4) V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in die dc level of V_{REF}.

TABLE 30
ODT DC Electrical Characteristics

Parameter / Condition	Symbol	Min.	Nom.	Max.	Unit	Note
Termination resistor impedance value for EMRS(1)[A6,A2] = [0,1]; 75 Ohm	Rtt1(eff)	60	75	90	Ω	1)
Termination resistor impedance value for EMRS(1)[A6,A2] =[1,0]; 150 Ohm	Rtt2(eff)	120	150	180	Ω	1)
Termination resistor impedance value for EMRS(1)(A6,A2)=[1,1]; 50 Ohm	Rtt3(eff)	40	50	60	Ω	1)
Deviation of V_M with respect to V_{DDQ} / 2	delta V_M	–6.00	—	+ 6.00	%	2)

1) Measurement Definition for Rtt(eff): Apply $V_{IH(ac)}$ and $V_{IL(ac)}$ to test pin separately, then measure current $I(V_{IHac})$ and $I(V_{ILac})$ respectively. $Rtt(eff) = (V_{IH(ac)} - V_{IL(ac)}) / (I(V_{IHac}) - I(V_{ILac}))$.
2) Measurement Definition for V_M: Turn ODT on and measure voltage (V_M) at test pin (midpoint) with no load: delta $V_M = ((2 \times V_M / V_{DDQ}) - 1) \times 100\%$

TABLE 31
Input and Output Leakage Currents

Symbol	Parameter / Condition	Min.	Max.	Unit	Note
I_{IL}	Input Leakage Current; any input 0 V < VIN < V_{DD}	–2	+2	µA	1)
I_{OL}	Output Leakage Current; 0 V < VOUT < V_{DDQ}	–5	+5	µA	2)

1) All other pins not under test = 0 V
2) DQ's, LDQS, $\overline{\text{LDQS}}$, UDQS, $\overline{\text{UDQS}}$, DQS, $\overline{\text{DQS}}$, RDQS, $\overline{\text{RDQS}}$ are disabled and ODT is turned off

5.3 DC & AC Characteristics

DDR2 SDRAM pin timing are specified for either single ended or differential mode depending on the setting of the EMRS(1) "Enable $\overline{DQS}$" mode bit; timing advantages of differential mode are realized in system design. The method by which the DDR2 SDRAM pin timing are measured is mode dependent. In single ended mode, timing relationships are measured relative to the rising or falling edges of DQS crossing at V_{REF}.

In differential mode, these timing relationships are measured relative to the crosspoint of DQS and its complement, $\overline{DQS}$. This distinction in timing methods is verified by design and characterization but not subject to production test. In single ended mode, the $\overline{DQS}$ (and $\overline{RDQS}$) signals are internally disabled and don't care.

TABLE 32
DC & AC Logic Input Levels for DDR2-667 and DDR2-800

Symbol	Parameter	DDR2-667, DDR2-800		Units
		Min.	Max.	
$V_{IH(dc)}$	DC input logic high	V_{REF} + 0.125	V_{DDQ} + 0.3	V
$V_{IL(dc)}$	DC input low	–0.3	V_{REF} – 0.125	V
$V_{IH(ac)}$	AC input logic high	V_{REF} + 0.200	—	V
$V_{IL(ac)}$	AC input low	—	V_{REF} – 0.200	V

TABLE 33
DC & AC Logic Input Levels for DDR2-533 and DDR2-400

Symbol	Parameter	DDR2-533, DDR2-400		Units
		Min.	Max.	
$V_{IH(dc)}$	DC input logic high	V_{REF} + 0.125	V_{DDQ} + 0.3	V
$V_{IL(dc)}$	DC input low	–0.3	V_{REF} - 0.125	V
$V_{IH(ac)}$	AC input logic high	V_{REF} + 0.250	—	V
$V_{IL(ac)}$	AC input low	—	V_{REF} - 0.250	V

TABLE 34
Single-ended AC Input Test Conditions

Symbol	Condition	Value	Unit	Notes
V_{REF}	Input reference voltage	0.5 x V_{DDQ}	V	1)
$V_{SWING.MAX}$	Input signal maximum peak to peak swing	1.0	V	1)
SLEW	Input signal minimum Slew Rate	1.0	V / ns	2)3)

1) Input waveform timing is referenced to the input signal crossing through the V_{REF} level applied to the device under test.
2) The input signal minimum Slew Rate is to be maintained over the range from $V_{IH(ac).MIN}$ to V_{REF} for rising edges and the range from V_{REF} to $V_{IL(ac).MAX}$ for falling edges as shown in **Figure 4**
3) AC timings are referenced with input waveforms switching from $V_{IL(ac)}$ to $V_{IH(ac)}$ on the positive transitions and $V_{IH(ac)}$ to $V_{IL(ac)}$ on the negative transitions.

FIGURE 4
Single-ended AC Input Test Conditions Diagram

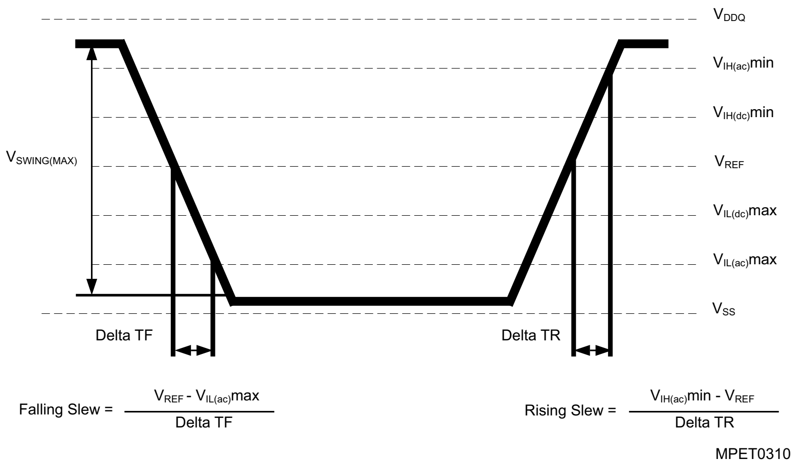
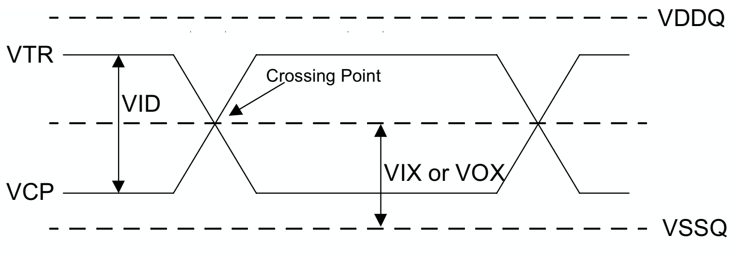


TABLE 35
Differential DC and AC Input and Output Logic Levels

Symbol	Parameter	Min.	Max.	Unit	Notes
$V_{IN(dc)}$	DC input signal voltage	–0.3	V_{DDQ} + 0.3	—	1)
$V_{ID(dc)}$	DC differential input voltage	0.25	V_{DDQ} + 0.6	—	2)
$V_{ID(ac)}$	AC differential input voltage	0.5	V_{DDQ} + 0.6	V	3)
$V_{IX(ac)}$	AC differential cross point input voltage	0.5 × V_{DDQ} – 0.175	0.5 × V_{DDQ} + 0.175	V	4)
$V_{OX(ac)}$	AC differential cross point output voltage	0.5 × V_{DDQ} – 0.125	0.5 × V_{DDQ} + 0.125	V	5)

1) $V_{IN(dc)}$ specifies the allowable DC execution of each input of differential pair such as CK, $\overline{\text{CK}}$, DQS, $\overline{\text{DQS}}$ etc.
2) $V_{ID(dc)}$ specifies the input differential voltage V_{TR}– V_{CP} required for switching. The minimum value is equal to $V_{IH(dc)} – V_{IL(dc)}$.
3) $V_{ID(ac)}$ specifies the input differential voltage $V_{TR} – V_{CP}$ required for switching. The minimum value is equal to $V_{IH(ac)} – V_{IL(ac)}$.
4) The value of $V_{IX(ac)}$ is expected to equal 0.5 × V_{DDQ} of the transmitting device and $V_{IX(ac)}$ is expected to track variations in V_{DDQ}. $V_{IX(ac)}$ indicates the voltage at which differential input signals must cross.
5) The value of $V_{OX(ac)}$ is expected to equal 0.5 × V_{DDQ} of the transmitting device and $V_{OX(ac)}$ is expected to track variations in V_{DDQ}. $V_{OX(ac)}$ indicates the voltage at which differential input signals must cross.

FIGURE 5
Differential DC and AC Input and Output Logic Levels Diagram



5.4 Output Buffer Characteristics

This chapter describes the Output Buffer Characteristics.

TABLE 36
SSTL_18 Output DC Current Drive

Symbol	Parameter	SSTL_18	Unit	Notes
I_{OH}	Output Minimum Source DC Current	–13.4	mA	1)2)
I_{OL}	Output Minimum Sink DC Current	13.4	mA	2)3)

1) V_{DDQ} = 1.7 V; V_{OUT} = 1.42 V. (V_{OUT}–V_{DDQ}) / I_{OH} must be less than 21 Ohm for values of V_{OUT} between V_{DDQ} and V_{DDQ} – 280 mV.
2) The values of $I_{OH(dc)}$ and $I_{OL(dc)}$ are based on the conditions given in 1) and 3). They are used to test drive current capability to ensure $V_{IH.MIN}$. plus a noise margin and $V_{IL.MAX}$ minus a noise margin are delivered to an SSTL_18 receiver. The actual current values are derived by shifting the desired driver operating points along 21 Ohm load line to define a convenient current for measurement.
3) V_{DDQ} = 1.7 V; V_{OUT} = 280 mV. V_{OUT} / I_{OL} must be less than 21 Ohm for values of V_{OUT} between 0 V and 280 mV.

TABLE 37
SSTL_18 Output AC Test Conditions

Symbol	Parameter	SSTL_18	Unit	Note
V_{OH}	Minimum Required Output Pull-up	V_{TT} + 0.603	V	1)
V_{OL}	Maximum Required Output Pull-down	V_{TT} – 0.603	V	1)
V_{OTR}	Output Timing Measurement Reference Level	0.5 × V_{DDQ}	V	

1) SSTL_18 test load for V_{OH} and V_{OL} is different from the referenced load described in **Chapter 8.1**. The SSTL_18 test load has a 20 Ohm series resistor additionally to the 25 Ohm termination resistor into V_{TT}. The SSTL_18 definition assumes that ± 335 mV must be developed across the effectively 25 Ohm termination resistor (13.4 mA × 25 Ohm = 335 mV). With an additional series resistor of 20 Ohm this translates into a minimum requirement of 603 mV swing relative to V_{TT}, at the ouput device (13.4 mA × 45 Ohm = 603 mV).

TABLE 38
OCD Default Characteristics

Symbol	Description	Min.	Nominal	Max.	Unit	Notes
—	Output Impedance	—			Ω	1)2)
—	Pull-up / Pull down mismatch	0	—	4	Ω	1)2)3)
—	Output Impedance step size for OCD calibration	0	—	1.5	Ω	4)
S_{OUT}	Output Slew Rate	1.5	—	5.0	V / ns	1)5)6)7)8)

1) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V
2) Impedance measurement condition for output source dc current: V_{DDQ} = 1.7 V, V_{OUT} = 1420 mV; (V_{OUT}–V_{DDQ}) / I_{OH} must be less than 23.4 ohms for values of V_{OUT} between V_{DDQ} and V_{DDQ} – 280 mV. Impedance measurement condition for output sink dc current: V_{DDQ} = 1.7 V; V_{OUT} = –280 mV; V_{OUT} / I_{OL} must be less than 23.4 Ohms for values of V_{OUT} between 0 V and 280 mV.
3) Mismatch is absolute value between pull-up and pull-down, both measured at same temperature and voltage.
4) This represents the step size when the OCD is near 18 ohms at nominal conditions across all process parameters and represents only the DRAM uncertainty. A 0 Ohm value (no calibration) can only be achieved if the OCD impedance is 18 ± 0.75 Ohms under nominal conditions.
5) Slew Rates according to **Chapter 8.2** $V_{IL(ac)}$ to $V_{IH(ac)}$ with the load specified in **Figure 76**.
6) The absolute value of the Slew Rate as measured from DC to DC is equal to or greater than the Slew Rate as measured from AC to AC. This is verified by design and characterization but not subject to production test.
7) Timing skew due to DRAM output Slew Rate mis-match between DQS / $\overline{DQS}$ and associated DQ's is included in t_{DQSQ} and t_{QHS} specification.
8) DRAM output Slew Rate specification applies to 400, 533 and 667 MT/s speed bins.

5.5 Input / Output Capacitance

This chapter contains the input / output capacitance.

TABLE 39
Input / Output Capacitance for DDR2-800

Symbol	Parameter	DDR2-800		
		Min.	Max.	Unit
CCK	Input capacitance, CK and $\overline{CK}$	1.0	2.0	pF
CDCK	Input capacitance delta, CK and $\overline{CK}$	—	0.25	pF
CI	Input capacitance, all other input-only pins	1.0	1.75	pF
CDI	Input capacitance delta, all other input-only pins	—	0.25	pF
CIO	Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$	2.5	3.5	pF
CDIO	Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$	—	0.5	pF

TABLE 40
Input / Output Capacitance for DDR2-667

Symbol	Parameter	DDR2-667		
		Min.	Max.	Unit
CCK	Input capacitance, CK and $\overline{CK}$	1.0	2.0	pF
CDCK	Input capacitance delta, CK and $\overline{CK}$	—	0.25	pF
CI	Input capacitance, all other input-only pins	1.0	2.0	pF
CDI	Input capacitance delta, all other input-only pins	—	0.25	pF
CIO	Input/output capacitance, DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$	2.5	3.5	pF
CDIO	Input/output capacitance delta, DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$	—	0.5	pF

TABLE 41
Input / Output Capacitance for DDR2-533

Symbol	Parameter	DDR2-533		
		Min.	Max.	Unit
CCK	Input capacitance, CK and $\overline{CK}$	1.0	2.0	pF
CDCK	Input capacitance delta, CK and $\overline{CK}$	—	0.25	pF
CI	Input capacitance, all other input-only pins	1.0	2.0	pF
CDI	Input capacitance delta, all other input-only pins	—	0.25	pF

Symbol	Parameter	DDR2-533		
		Min.	Max.	Unit
CIO	Input/output capacitance, DQ, DM, DQS, $\overline{\text{DQS}}$, RDQS, $\overline{\text{RDQS}}$	2.5	4.0	pF
CDIO	Input/output capacitance delta, DQ, DM, DQS, $\overline{\text{DQS}}$, RDQS, $\overline{\text{RDQS}}$	—	0.5	pF

TABLE 42
Input / Output Capacitance for DDR2-400

Symbol	Parameter	DDR2-400		
		Min.	Max.	Unit
CCK	Input capacitance, CK and $\overline{\text{CK}}$	1.0	2.0	pF
CDCK	Input capacitance delta, CK and $\overline{\text{CK}}$	—	0.25	pF
CI	Input capacitance, all other input-only pins	1.0	2.0	pF
CDI	Input capacitance delta, all other input-only pins	—	0.25	pF
CIO	Input/output capacitance, DQ, DM, DQS, $\overline{\text{DQS}}$, RDQS, $\overline{\text{RDQS}}$	2.5	4.0	pF
CDIO	Input/output capacitance delta, DQ, DM, DQS, $\overline{\text{DQS}}$, RDQS, $\overline{\text{RDQS}}$	—	0.5	pF

5.6 Overshoot and Undershoot Specification

This chapter contains overshoot and undershoot specification.

TABLE 43
AC Overshoot / Undershoot Specification for Address and Control Pins

Parameter	DDR2-400	DDR2-533	DDR2-667	DDR2-800	Unit
Maximum peak amplitude allowed for overshoot area	0.9	0.9	0.9	0.9	V
Maximum peak amplitude allowed for undershoot area	0.9	0.9	0.9	0.9	V
Maximum overshoot area above V_{DD}	1.33	1.00	0.80	0.66	V.ns
Maximum undershoot area below V_{SS}	1.33	1.00	0.80	0.66	V.ns

FIGURE 6
AC Overshoot / Undershoot Diagram for Address and Control Pins

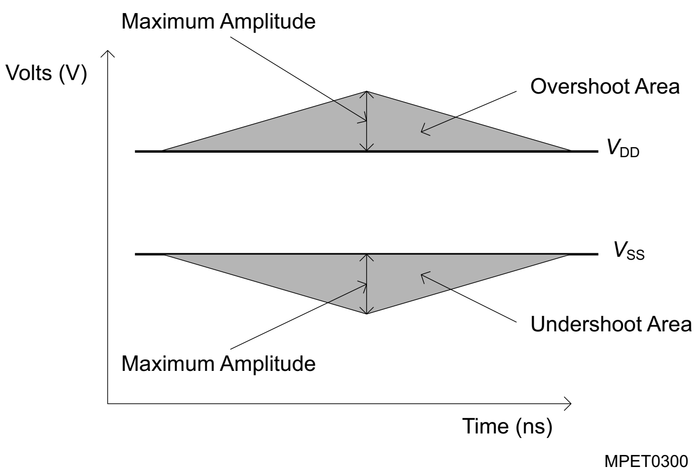
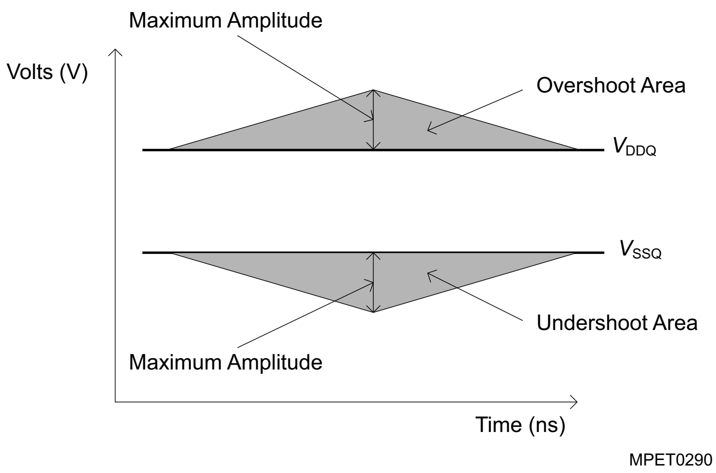


TABLE 44
AC Overshoot / Undershoot Spec. for Clock, Data, Strobe and Mask Pins

Parameter	DDR2-400	DDR2-533	DDR2-667	DDR2-800	Unit
Maximum peak amplitude allowed for overshoot area	0.9	0.9	0.9	0.9	V
Maximum peak amplitude allowed for undershoot area	0.9	0.9	0.9	0.9	V
Maximum overshoot area above V_{DDQ}	0.38	0.28	0.23	0.23	V.ns
Maximum undershoot area below V_{SSQ}	0.38	0.28	0.23	0.23	V.ns

FIGURE 7
AC Overshoot / Undershoot Diagram for Clock, Data, Strobe and Mask Pins



6 Specifications and Conditions

This chapter describes the Specifications and Conditions.

TABLE 45
I_{DD} Measurement Conditions

Parameter	Symbol	Note
Operating Current - One bank Active - Precharge $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RAS.MIN(IDD)}$, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are switching; Databus inputs are switching.	I_{DD0}	1)2)3)4)5)6)
Operating Current - One bank Active - Read - Precharge I_{OUT} = 0 mA, BL = 4, $t_{CK} = t_{CK(IDD)}$, $t_{RC} = t_{RC(IDD)}$, $t_{RAS} = t_{RAS.MIN(IDD)}$, $t_{RCD} = t_{RCD(IDD)}$, AL = 0, CL = CL(IDD); CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address and control inputs are switching; Databus inputs are switching.	I_{DD1}	1)2)3)4)5)6)
Precharge Power-Down Current All banks idle; CKE is LOW; $t_{CK} = t_{CK(IDD)}$;Other control and address inputs are stable; Data bus inputs are floating.	I_{DD2P}	1)2)3)4)5)6)
Precharge Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK(IDD)}$; Other control and address inputs are switching, Data bus inputs are switching.	I_{DD2N}	1)2)3)4)5)6)
Precharge Quiet Standby Current All banks idle; $\overline{CS}$ is HIGH; CKE is HIGH; $t_{CK} = t_{CK(IDD)}$; Other control and address inputs are stable, Data bus inputs are floating.	I_{DD2Q}	1)2)3)4)5)6)
Active Power-Down Current All banks open; $t_{CK} = t_{CK(IDD)}$, CKE is LOW; Other control and address inputs are stable; Data bus inputs are floating. MRS A12 bit is set to “0” (Fast Power-down Exit).	$I_{DD3P(0)}$	1)2)3)4)5)6)
Active Power-Down Current All banks open; $t_{CK} = t_{CK(IDD)}$, CKE is LOW; Other control and address inputs are stable, Data bus inputs are floating. MRS A12 bit is set to 1 (Slow Power-down Exit);	$I_{DD3P(1)}$	1)2)3)4)5)6)
Active Standby Current All banks open; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS.MAX(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are switching; Data Bus inputs are switching;	I_{DD3N}	1)2)3)4)5)6)
Operating Current Burst Read: All banks open; Continuous burst reads; BL = 4; AL = 0, CL = $CL_{(IDD)}$; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS.MAX.(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are switching; Data Bus inputs are switching; I_{OUT} = 0 mA.	I_{DD4R}	1)2)3)4)5)6)
Operating Current Burst Write: All banks open; Continuous burst writes; BL = 4; AL = 0, CL = $CL_{(IDD)}$; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS.MAX(IDD)}$, $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address inputs are switching; Data Bus inputs are switching;	I_{DD4W}	1)2)3)4)5)6)
Burst Refresh Current $t_{CK} = t_{CK(IDD)}$, Refresh command every $t_{RFC} = t_{RFC(IDD)}$ interval, CKE is HIGH, $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are switching, Data bus inputs are switching.	I_{DD5B}	1)2)3)4)5)6)
Distributed Refresh Current $t_{CK} = t_{CK(IDD)}$, Refresh command every t_{REFI} = 7.8 µs interval, CKE is LOW and $\overline{CS}$ is HIGH between valid commands, Other control and address inputs are switching, Data bus inputs are switching.	I_{DD5D}	1)2)3)4)5)6)

Parameter	Symbol	Note
Self-Refresh Current CKE ≤ 0.2 V; external clock off, CK and $\overline{CK}$ at 0 V; Other control and address inputs are floating, Data bus inputs are floating.	I_{DD6}	1)2)3)4)5)6)
Operating Bank Interleave Read Current 1. All banks interleaving reads, I_{OUT} = 0 mA; BL = 4, CL = $CL_{(IDD)}$, AL = $t_{RCD(IDD)}$ -1 × $t_{CK(IDD)}$; t_{CK} = $t_{CK(IDD)}$, t_{RC} = $t_{RC(IDD)}$, t_{RRD} = $t_{RRD(IDD)}$; CKE is HIGH, $\overline{CS}$ is HIGH between valid commands. Address bus inputs are stable during deselects; Data bus is switching. 2. Timing pattern:	I_{DD7}	1)2)3)4)5)6)7)
DDR2-400-333: A0 RA0 A1 RA1 A2 RA2 A3 RA3 D D D (11 clocks)		
DDR2-533-333: A0 RA0 D A1 RA1 D A2 RA2 D A3 RA3 D D D D (15 clocks)		
DDR2-667-444: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D (19 clocks)		
DDR2-667-555: A0 RA0 D D A1 RA1 D D A2 RA2 D D A3 RA3 D D D D D D (20 clocks)		
DDR2-800-555: A0 RA0 D D D A1 RA1 D D D A2 RA2 D D D A3 RA3 D D D D D(22 clocks)		
DDR2-800-666: A0 RA0 D D D A1 RA1 D D D A2 RA2 D D D A3 RA3 D D D D D D(23 clocks)		

1) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ± 0.1 V
2) I_{DD} specifications are tested after the device is properly initialized.
3) I_{DD} parameter are specified with ODT disabled.
4) Data Bus consists of DQ, DM, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, LDQS, $\overline{LDQS}$, UDQS and $\overline{UDQS}$.
5) Definitions for I_{DD}: see **Table 46**
6) Timing parameter minimum and maximum values for I_{DD} current measurements are defined in chapter 7..
7) A = Activate, RA = Read with Auto-Precharge, D=DESELECT

TABLE 46
Definition for I_{DD}

Parameter	Description
LOW	defined as $V_{IN} \leq V_{IL(ac).MAX}$
HIGH	defined as $V_{IN} \geq V_{IH(ac).MIN}$
STABLE	defined as inputs are stable at a HIGH or LOW level
FLOATING	defined as inputs are $V_{REF} = V_{DDQ} / 2$
SWITCHING	defined as: Inputs are changing between high and low every other clock (once per two clocks) for address and control signals, and inputs changing between high and low every other clock (once per clock) for DQ signals not including mask or strobes

TABLE 47
I_{DD} Specification

Symbol	-25F	-2.5	-3	-3S	-3.7	-5	Unit	Note
	DDR2 - 800	DDR2 - 800	DDR2 - 667	DDR2 - 667	DDR2 - 533	DDR2 - 400		
	Max.	Max.	Max.	Max.	Max.	Max.		
I_{DD0}	70	65	64	61	55	54	mA	×4/×8/x16
I_{DD1}	75	70	70	66	60	58	mA	×4/×8/x16
I_{DD2P}	6.5	6.5	6	6	6	6	mA	
I_{DD2N}	37	37	33	33	29	27	mA	
I_{DD2Q}	34	34	30	30	26	23	mA	
I_{DD3P}	22	22	19	19	17.5	16	mA	1)
	7.5	7.5	7.5	7.5	7	7	mA	2)
I_{DD3N}	44	44	39	39	33	29	mA	
I_{DD4R}	114	114	105	105	84	74	mA	x4/x8
	140	140	127	127	105	100	mA	x16
I_{DD4W}	124	124	108	108	90	75	mA	x4/x8
	160	160	140	140	115	105	mA	x16
I_{DD5B}	104	104	97	97	92	90	mA	
I_{DD5D}	7.5	7.5	7.5	7.5	7.5	7.5	mA	3)
I_{DD6}	4	4	4	4	4	4	mA	3) Standard
	—	—	—	—	2	—	mA	3) Low power
I_{DD7}	140	135	136	130	126	125	mA	x4/x8
	145	140	140	134	135	132	mA	x16

1) MRS(12)=0
2) MRS(12)=1
3) $0° \leq T_{CASE} \leq 85$ °C.

7 Timing Characteristics

This chapter contains speed grade definition, AC timing parameter and ODT tables.

7.1 Speed Grade Definitions

All Speed grades faster than DDR2-400B comply with DDR2-400B timing specifications (t_{CK} = 5ns with t_{RAS} = 40ns).

TABLE 48
Speed Grade Definition Speed Bins for DDR2–800

Speed Grade			**DDR2–800D**		**DDR2–800E**		**Unit**	**Note**
QAG Sort Name			**–2.5F**		**–2.5**			
CAS-RCD-RP latencies			**5–5–5**		**6–6–6**		t_{CK}	
Parameter		**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**—**	
Clock Frequency	@ CL = 3	t_{CK}	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	2.5	8	3	8	ns	1)2)3)4)
	@ CL = 6	t_{CK}	2.5	8	2.5	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70000	45	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	57.5	—	60	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	12.5	—	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	12.5	—	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) under the “Reference Load for Timing Measurements”.
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode; The input reference level for signals other than CK/CK, DQS / DQS, RDQS / RDQS is defined .
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

TABLE 49
Speed Grade Definition Speed Bins for DDR2–667

Speed Grade			**DDR2–667C**		**DDR2–667D**		**Unit**	**Notes**
QAG Sort Name			**–3**		**–3S**			
CAS-RCD-RP latencies			**4–4–4**		**5–5–5**		t_{CK}	
Parameter		**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**—**	
Clock Frequency	@ CL = 3	t_{CK}	5	8	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3	8	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3	8	3	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70000	45	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	57	—	60	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	12	—	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	12	—	15	—	ns	1)2)3)4)

1) imings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) under the “Reference Load for Timing Measurements”.
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode; The input reference level for signals other than CK/CK, DQS / DQS, RDQS / RDQS is defined.
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

TABLE 50
Speed Grade Definition Speed Bins for DDR2–533C

Speed Grade			**DDR2–533C**		**Unit**	**Note**
QAG Sort Name			**–3.7**			
CAS-RCD-RP latencies			**4–4–4**		t_{CK}	
Parameter		**Symbol**	**Min.**	**Max.**	**—**	
Clock Frequency	@ CL = 3	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	3.75	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	3.75	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	45	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	60	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) under the “Reference Load for Timing Measurements”.
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode; The input reference level for signals other than CK/CK, DQS / DQS, RDQS / RDQS is defined.

3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
4) The output timing reference voltage level is V_{TT}.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

TABLE 51
Speed Grade Definition Speed Bins for DDR2-400B

Speed Grade			DDR2–400B		Unit	Note
QAG Sort Name			–5			
CAS-RCD-RP latencies			3–3–3		t_{CK}	
Parameter		Symbol	Min.	Max.	—	
Clock Frequency	@ CL = 3	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 4	t_{CK}	5	8	ns	1)2)3)4)
	@ CL = 5	t_{CK}	5	8	ns	1)2)3)4)
Row Active Time		t_{RAS}	40	70000	ns	1)2)3)4)5)
Row Cycle Time		t_{RC}	55	—	ns	1)2)3)4)
RAS-CAS-Delay		t_{RCD}	15	—	ns	1)2)3)4)
Row Precharge Time		t_{RP}	15	—	ns	1)2)3)4)

1) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. For other Slew Rates see Chapter 8Timings are further guaranteed for normal OCD drive strength (EMRS(1) A1 = 0) under the "Reference Load for Timing Measurements" according to Chapter 8.1 only.
2) The CK/$\overline{CK}$ input reference level (for timing reference to CK/$\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode; The input reference level for signals other than CK/CK, DQS / DQS, RDQS / RDQS is defined in Chapter 8.3.
3) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
4) The output timing reference voltage level is V_{TT}. See section 8 for the reference load for timing measurements.
5) $t_{RAS.MAX}$ is calculated from the maximum amount of time a DDR2 device can operate without a refresh command which is equal to 9 x t_{REFI}.

7.2 Component AC Timing Parameters

List of Timing Parameters Tables.

TABLE 52
DRAM Component Timing Parameter by Speed Grade - DDR2–800

Parameter	Symbol	DDR2–800		Unit	Notes[1)2)3)4)5)6)7)]
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–400	+400	ps	8)
CAS to CAS command delay	t_{CCD}	2	—	nCK	
Average clock high pulse width	$t_{CH.AVG}$	0.48	0.52	$t_{CK.AVG}$	9)10)
Average clock period	$t_{CK.AVG}$	2500	8000	ps	9)10)
CKE minimum pulse width (high and low pulse width)	t_{CKE}	3	—	nCK	11)
Average clock low pulse width	$t_{CL.AVG}$	0.48	0.52	$t_{CK.AVG}$	9)10)
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{nRP}	—	nCK	12)13)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	t_{IS} + $t_{CK.AVG}$ + t_{IH}	—	ns	
DQ and DM input hold time	$t_{DH.BASE}$	125	—	ps	18)19)14)
DQ and DM input pulse width for each input	t_{DIPW}	0.35	—	$t_{CK.AVG}$	
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–350	+350	ps	8)
DQS input high pulse width	t_{DQSH}	0.35	—	$t_{CK.AVG}$	
DQS input low pulse width	t_{DQSL}	0.35	—	$t_{CK.AVG}$	
DQS-DQ skew for DQS & associated DQ signals	t_{DQSQ}	—	200	ps	15)
DQS latching rising transition to associated clock edges	t_{DQSS}	– 0.25	+ 0.25	$t_{CK.AVG}$	16)
DQ and DM input setup time	$t_{DS.BASE}$	50	—	ps	17)18)19)
DQS falling edge hold time from CK	t_{DSH}	0.2	—	$t_{CK.AVG}$	16)
DQS falling edge to CK setup time	t_{DSS}	0.2	—	$t_{CK.AVG}$	16)
CK half pulse width	t_{HP}	Min($t_{CH.ABS}$, $t_{CL.ABS}$)	—	ps	20)
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	8)21)
Address and control input hold time	$t_{IH.BASE}$	250	—	ps	22)24)
Control & address input pulse width for each input	t_{IPW}	0.6	—	$t_{CK.AVG}$	
Address and control input setup time	$t_{IS.BASE}$	175	—	ps	23)24)
DQ low impedance time from CK/$\overline{CK}$	$t_{LZ.DQ}$	2 x $t_{AC.MIN}$	$t_{AC.MAX}$	ps	8)21)
DQS/$\overline{DQS}$ low-impedance time from CK / $\overline{CK}$	$t_{LZ.DQS}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	8)21)
MRS command to ODT update delay	t_{MOD}	0	12	ns	34)
Mode register set command cycle time	t_{MRD}	2	—	nCK	
OCD drive mode output delay	t_{OIT}	0	12	ns	34)
DQ/DQS output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—	ps	25)
DQ hold skew factor	t_{QHS}	—	300	ps	26)

Parameter	Symbol	DDR2–800		Unit	Notes[1)2)3)4)5)6)7)]
		Min.	Max.		
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	27)28)
		—	3.9	µs	28)29)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	75	—	ns	30)
Precharge-All (4 banks) command period	t_{RP}	t_{RP}	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	$t_{CK.AVG}$	31)32)
Read postamble	t_{RPST}	0.4	0.6	$t_{CK.AVG}$	31)33)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	34)
Write preamble	t_{WPRE}	0.35	—	$t_{CK.AVG}$	
Write postamble	t_{WPST}	0.4	0.6	$t_{CK.AVG}$	
Write recovery time	t_{WR}	15	—	ns	34)
Internal write to read command delay	t_{WTR}	7.5	—	ns	34)35)
Exit power down to read command	t_{XARD}	2	—	nCK	
Exit active power-down mode to read command (slow exit, lower power)	t_{XARDS}	8 – AL	—	nCK	
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	nCK	
Exit self-refresh to a non-read command	t_{XSNR}	t_{RFC} +10	—	ns	34)
Exit self-refresh to read command	t_{XSRD}	200	—	nCK	
Write command to DQS associated clock edges	WL	RL – 1		nCK	

1) V_{DDQ} = 1.8 V ± 0.1V; V_{DD} = 1.8 V ± 0.1 V.
2) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
3) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. For other Slew Rates see **Chapter 8** of this datasheet.
4) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode. The input reference level for signals other than CK/$\overline{CK}$, DQS/$\overline{DQS}$, RDQS / $\overline{RDQS}$ is defined in **Chapter 8.3** of this datasheet.
5) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
6) The output timing reference voltage level is V_{TT}. See **Chapter 8** for the reference load for timing measurements.
7) New units, '$t_{CK.AVG}$' and 'nCK', are introduced in DDR2–667 and DDR2–800. Unit '$t_{CK.AVG}$' represents the actual $t_{CK.AVG}$ of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2–400 and DDR2–533, 't_{CK}' is used for both concepts. Example: t_{XP} = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm + 2, even if (Tm + 2 - Tm) is 2 x $t_{CK.AVG}$ + $t_{ERR.2PER(Min)}$.
8) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{ERR(6-10per)}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{ERR(6-10PER).MIN}$ = – 272 ps and $t_{ERR(6-10PER).MAX}$ = + 293 ps, then $t_{DQSCK.MIN(DERATED)}$ = $t_{DQSCK.MIN}$ – $t_{ERR(6-10PER).MAX}$ = – 400 ps – 293 ps = – 693 ps and $t_{DQSCK.MAX(DERATED)}$ = $t_{DQSCK.MAX}$ – $t_{ERR(6-10PER).MIN}$ = 400 ps + 272 ps = + 672 ps. Similarly, $t_{LZ.DQ}$ for DDR2–667 derates to $t_{LZ.DQ.MIN(DERATED)}$ = - 900 ps – 293 ps = – 1193 ps and $t_{LZ.DQ.MAX(DERATED)}$ = 450 ps + 272 ps = + 722 ps. (Caution on the MIN/MAX usage!)
9) Input clock jitter spec parameter. These parameters and the ones in **Chapter 7.3** are referred to as 'input clock jitter spec parameters' and these parameters apply to DDR2–667 and DDR2–800 only. The jitter specified is a random jitter meeting a Gaussian distribution.
10) These parameters are specified per their average values, however it is understood that the relationship as defined in **Chapter 7.3** between the average timing and the absolute instantaneous timing holds all the times (min. and max of SPEC values are to be used for calculations of **Chapter 7.3**).
11) $t_{CKE.MIN}$ of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + 2 x t_{CK} + t_{IH}.

12) DAL = WR + RU{t_{RP}(ns) / t_{CK}(ns)}, where RU stands for round up. WR refers to the tWR parameter stored in the MRS. For t_{RP}, if the result of the division is not already an integer, round up to the next highest integer. t_{CK} refers to the application clock period. Example: For DDR2–533 at t_{CK} = 3.75 ns with t_{WR} programmed to 4 clocks. t_{DAL} = 4 + (15 ns / 3.75 ns) clocks = 4 + (4) clocks = 8 clocks.
13) $t_{DAL.nCK}$ = WR [nCK] + $t_{nRP.nCK}$ = WR + RU{t_{RP} [ps] / $t_{CK.AVG}$[ps] }, where WR is the value programmed in the EMR.
14) Input waveform timing t_{DH} with differential data strobe enabled MR[bit10] = 0, is referenced from the differential data strobe crosspoint to the input signal crossing at the $V_{IH.DC}$ level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the $V_{IL.DC}$ level for a rising signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{IL.DC.MAX}$ and $V_{IH.DC.MIN}$. See **Figure 9**.
15) t_{DQSQ}: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS / $\overline{DQS}$ and associated DQ in any given cycle.
16) These parameters are measured from a data strobe signal ((L/U/R)DQS / $\overline{DQS}$) crossing to its respective clock signal (CK / $\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$, etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
17) Input waveform timing t_{DS} with differential data strobe enabled MR[bit10] = 0, is referenced from the input signal crossing at the $V_{IH.AC}$ level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the $V_{IL.AC}$ level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{il(DC)MAX}$ and $V_{ih(DC)MIN}$. See **Figure 9**.
18) If t_{DS} or t_{DH} is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
19) These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS / $\overline{DQS}$) crossing.
20) t_{HP} is the minimum of the absolute half period of the actual input clock. t_{HP} is an input parameter but not an input specification parameter. It is used in conjunction with t_{QHS} to derive the DRAM output timing t_{QH}. The value to be used for t_{QH} calculation is determined by the following equation; t_{HP} = MIN ($t_{CH.ABS}$, $t_{CL.ABS}$), where, $t_{CH.ABS}$ is the minimum of the actual instantaneous clock high time; $t_{CL.ABS}$ is the minimum of the actual instantaneous clock low time.
21) t_{HZ} and t_{LZ} transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (t_{HZ}), or begins driving (t_{LZ}) .
22) Input waveform timing is referenced from the input signal crossing at the $V_{IL.DC}$ level for a rising signal and $V_{IH.DC}$ for a falling signal applied to the device under test. See **Figure 10**.
23) Input waveform timing is referenced from the input signal crossing at the $V_{IH.AC}$ level for a rising signal and $V_{IL.AC}$ for a falling signal applied to the device under test. See **Figure 10**.
24) These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK / $\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$, etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
25) t_{QH} = t_{HP} – t_{QHS}, where: t_{HP} is the minimum of the absolute half period of the actual input clock; and t_{QHS} is the specification value under the max column. {The less half-pulse width distortion present, the larger the t_{QH} value is; and the larger the valid data eye will be.} Examples: 1) If the system provides t_{HP} of 1315 ps into a DDR2–667 SDRAM, the DRAM provides t_{QH} of 975 ps minimum. 2) If the system provides t_{HP} of 1420 ps into a DDR2–667 SDRAM, the DRAM provides t_{QH} of 1080 ps minimum.
26) t_{QHS} accounts for: 1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual t_{HP} at the input is transferred to the output; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and pchannel to n-channel variation of the output drivers.
27) The Auto-Refresh command interval has be reduced to 3.9 µs when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
28) 0 °C≤ T_{CASE} ≤ 85 °C
29) 85 °C < T_{CASE} ≤ 95 °C
30) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
31) t_{RPST} end point and t_{RPRE} begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (t_{RPST}), or begins driving (t_{RPRE}). **Figure 8** shows a method to calculate these points when the device is no longer driving (t_{RPST}), or begins driving (t_{RPRE}) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.
32) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.PER}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.PER.MIN}$ = – 72 ps and $t_{JIT.PER.MAX}$ = + 93 ps, then $t_{RPRE.MIN(DERATED)}$ = $t_{RPRE.MIN}$ + $t_{JIT.PER.MIN}$ = 0.9 x $t_{CK.AVG}$ – 72 ps = + 2178 ps and $t_{RPRE.MAX(DERATED)}$ = $t_{RPRE.MAX}$ + $t_{JIT.PER.MAX}$ = 1.1 x $t_{CK.AVG}$ + 93 ps = + 2843 ps. (Caution on the MIN/MAX usage!).
33) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.DUTY}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.DUTY.MIN}$ = – 72 ps and $t_{JIT.DUTY.MAX}$ = + 93 ps, then $t_{RPST.MIN(DERATED)}$ = $t_{RPST.MIN}$ + $t_{JIT.DUTY.MIN}$ = 0.4 x $t_{CK.AVG}$ – 72 ps = + 928 ps and $t_{RPST.MAX(DERATED)}$ = $t_{RPST.MAX}$ + $t_{JIT.DUTY.MAX}$ = 0.6 x $t_{CK.AVG}$ + 93 ps = + 1592 ps. (Caution on the MIN/MAX usage!).

34) For these parameters, the DDR2 SDRAM device is characterized and verified to support t_{nPARAM} = RU{t_{PARAM} / $t_{CK.AVG}$}, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support t_{nRP} = RU{t_{RP} / $t_{CK.AVG}$}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR2–667 5–5–5, of which t_{RP} = 15 ns, the device will support t_{nRP} = RU{t_{RP} / $t_{CK.AVG}$} = 5, i.e. as long as the input clock jitter specifications are met, Precharge command at Tm and Active command at Tm + 5 is valid even if (Tm + 5 - Tm) is less than 15 ns due to input clock jitter.

35) t_{WTR} is at lease two clocks (2 x t_{CK}) independent of operation frequency.

TABLE 53

DRAM Component Timing Parameter by Speed Grade - DDR2–667

Parameter	Symbol	DDR2–667		Unit	Notes[1)2)3)4)5)6)7)]
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–450	+450	ps	8)
CAS to CAS command delay	t_{CCD}	2	—	nCK	
Average clock high pulse width	$t_{CH.AVG}$	0.48	0.52	$t_{CK.AVG}$	9)10)
Average clock period	$t_{CK.AVG}$	3000	8000	ps	
CKE minimum pulse width (high and low pulse width)	t_{CKE}	3	—	nCK	11)
Average clock low pulse width	$t_{CL.AVG}$	0.48	0.52	$t_{CK.AVG}$	9)10)
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{nRP}	—	nCK	12)13)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	t_{IS} + $t_{CK.AVG}$ + t_{IH}	—	ns	
DQ and DM input hold time	$t_{DH.BASE}$	175	—	ps	18)19)14)
DQ and DM input pulse width for each input	t_{DIPW}	0.35	—	$t_{CK.AVG}$	
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–400	+400	ps	8)
DQS input high pulse width	t_{DQSH}	0.35	—	$t_{CK.AVG}$	
DQS input low pulse width	t_{DQSL}	0.35	—	$t_{CK.AVG}$	
DQS-DQ skew for DQS & associated DQ signals	t_{DQSQ}	—	240	ps	15)
DQS latching rising transition to associated clock edges	t_{DQSS}	– 0.25	+ 0.25	$t_{CK.AVG}$	16)
DQ and DM input setup time	$t_{DS.BASE}$	100	—	ps	17)18)19)
DQS falling edge hold time from CK	t_{DSH}	0.2	—	$t_{CK.AVG}$	16)
DQS falling edge to CK setup time	t_{DSS}	0.2	—	$t_{CK.AVG}$	16)
CK half pulse width	t_{HP}	Min($t_{CH.ABS}$, $t_{CL.ABS}$)	—	ps	20)
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	8)21)
Address and control input hold time	$t_{IH.BASE}$	275	—	ps	24)22)
Control & address input pulse width for each input	t_{IPW}	0.6	—	$t_{CK.AVG}$	
Address and control input setup time	$t_{IS.BASE}$	200	—	ps	23)24)
DQ low impedance time from CK/$\overline{CK}$	$t_{LZ.DQ}$	2 x $t_{AC.MIN}$	$t_{AC.MAX}$	ps	8)21)
DQS/$\overline{DQS}$ low-impedance time from CK / $\overline{CK}$	$t_{LZ.DQS}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	8)21)
MRS command to ODT update delay	t_{MOD}	0	12	ns	34)
Mode register set command cycle time	t_{MRD}	2	—	nCK	
OCD drive mode output delay	t_{OIT}	0	12	ns	34)
DQ/DQS output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—	ps	25)

Parameter	Symbol	DDR2–667		Unit	Notes[1)2)3)4)5)6)7)]
		Min.	Max.		
DQ hold skew factor	t_{QHS}	—	340	ps	26)
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	27)28)
		—	3.9	µs	28)29)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	75	—	ns	30)
Precharge-All (4 banks) command period	t_{RP}	t_{RP}	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	$t_{CK.AVG}$	31)32)
Read postamble	t_{RPST}	0.4	0.6	$t_{CK.AVG}$	31)33)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	34)
Write preamble	t_{WPRE}	0.35	—	$t_{CK.AVG}$	
Write postamble	t_{WPST}	0.4	0.6	$t_{CK.AVG}$	
Write recovery time	t_{WR}	15	—	ns	34)
Internal write to read command delay	t_{WTR}	7.5	—	ns	34)35)
Exit power down to read command	t_{XARD}	2	—	nCK	
Exit active power-down mode to read command (slow exit, lower power)	t_{XARDS}	7 – AL	—	nCK	
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	nCK	
Exit self-refresh to a non-read command	t_{XSNR}	t_{RFC} +10	—	ns	34)
Exit self-refresh to read command	t_{XSRD}	200	—	nCK	
Write command to DQS associated clock edges	WL	RL–1		nCK	

1) V_{DDQ} = 1.8 V ± 0.1V; V_{DD} = 1.8 V ± 0.1 V.
2) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
3) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. For other Slew Rates see **Chapter 8** of this datasheet.
4) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode. The input reference level for signals other than CK/$\overline{CK}$, DQS/$\overline{DQS}$, RDQS / $\overline{RDQS}$ is defined in **Chapter 8.3** of this datasheet.
5) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
6) The output timing reference voltage level is V_{TT}. See **Chapter 8** for the reference load for timing measurements.
7) New units, '$t_{CK.AVG}$' and 'nCK', are introduced in DDR2–667 and DDR2–800. Unit '$t_{CK.AVG}$' represents the actual $t_{CK.AVG}$ of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2–400 and DDR2–533, 't_{CK}' is used for both concepts. Example: t_{XP} = 2 [nCK] means; if Power Down exit is registered at Tm, an Active command may be registered at Tm + 2, even if (Tm + 2 - Tm) is 2 x $t_{CK.AVG}$ + $t_{ERR.2PER(Min)}$.
8) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{ERR(6-10per)}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{ERR(6-10PER).MIN}$ = – 272 ps and $t_{ERR(6-10PER).MAX}$ = + 293 ps, then $t_{DQSCK.MIN(DERATED)}$ = $t_{DQSCK.MIN}$ – $t_{ERR(6-10PER).MAX}$ = – 400 ps – 293 ps = – 693 ps and $t_{DQSCK.MAX(DERATED)}$ = $t_{DQSCK.MAX}$ – $t_{ERR(6-10PER).MIN}$ = 400 ps + 272 ps = + 672 ps. Similarly, $t_{LZ.DQ}$ for DDR2–667 derates to $t_{LZ.DQ.MIN(DERATED)}$ = - 900 ps – 293 ps = – 1193 ps and $t_{LZ.DQ.MAX(DERATED)}$ = 450 ps + 272 ps = + 722 ps. (Caution on the MIN/MAX usage!)
9) Input clock jitter spec parameter. These parameters and the ones in **Chapter 7.3** are referred to as 'input clock jitter spec parameters' and these parameters apply to DDR2–667 and DDR2–800 only. The jitter specified is a random jitter meeting a Gaussian distribution.
10) These parameters are specified per their average values, however it is understood that the relationship as defined in **Chapter 7.3** between the average timing and the absolute instantaneous timing holds all the times (min. and max of SPEC values are to be used for calculations of **Chapter 7.3**).

11) $t_{CKE.MIN}$ of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + 2 x t_{CK} + t_{IH}.
12) DAL = WR + RU{t_{RP}(ns) / t_{CK}(ns)}, where RU stands for round up. WR refers to the tWR parameter stored in the MRS. For t_{RP}, if the result of the division is not already an integer, round up to the next highest integer. t_{CK} refers to the application clock period. Example: For DDR2–533 at t_{CK} = 3.75 ns with t_{WR} programmed to 4 clocks. t_{DAL} = 4 + (15 ns / 3.75 ns) clocks = 4 + (4) clocks = 8 clocks.
13) $t_{DAL.nCK}$ = WR [nCK] + $t_{nRP.nCK}$ = WR + RU{t_{RP} [ps] / $t_{CK.AVG}$[ps] }, where WR is the value programmed in the EMR.
14) Input waveform timing t_{DH} with differential data strobe enabled MR[bit10] = 0, is referenced from the differential data strobe crosspoint to the input signal crossing at the $V_{IH.DC}$ level for a falling signal and from the differential data strobe crosspoint to the input signal crossing at the $V_{IL.DC}$ level for a rising signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{IL.DC.MAX}$ and $V_{IH.DC.MIN}$. See **Figure 9**.
15) t_{DQSQ}: Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output slew rate mismatch between DQS / $\overline{DQS}$ and associated DQ in any given cycle.
16) These parameters are measured from a data strobe signal ((L/U/R)DQS / $\overline{DQS}$) crossing to its respective clock signal (CK / $\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$, etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
17) Input waveform timing t_{DS} with differential data strobe enabled MR[bit10] = 0, is referenced from the input signal crossing at the $V_{IH.AC}$ level to the differential data strobe crosspoint for a rising signal, and from the input signal crossing at the $V_{IL.AC}$ level to the differential data strobe crosspoint for a falling signal applied to the device under test. DQS, DQS signals must be monotonic between $V_{il(DC)MAX}$ and $V_{ih(DC)MIN}$. See **Figure 9**.
18) If t_{DS} or t_{DH} is violated, data corruption may occur and the data must be re-written with valid data before a valid READ can be executed.
19) These parameters are measured from a data signal ((L/U)DM, (L/U)DQ0, (L/U)DQ1, etc.) transition edge to its respective data strobe signal ((L/U/R)DQS / $\overline{DQS}$) crossing.
20) t_{HP} is the minimum of the absolute half period of the actual input clock. t_{HP} is an input parameter but not an input specification parameter. It is used in conjunction with t_{QHS} to derive the DRAM output timing t_{QH}. The value to be used for t_{QH} calculation is determined by the following equation; t_{HP} = MIN ($t_{CH.ABS}$, $t_{CL.ABS}$), where, $t_{CH.ABS}$ is the minimum of the actual instantaneous clock high time; $t_{CL.ABS}$ is the minimum of the actual instantaneous clock low time.
21) t_{HZ} and t_{LZ} transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving (t_{HZ}), or begins driving (t_{LZ}) .
22) Input waveform timing is referenced from the input signal crossing at the $V_{IL.DC}$ level for a rising signal and $V_{IH.DC}$ for a falling signal applied to the device under test. See **Figure 10**.
23) Input waveform timing is referenced from the input signal crossing at the $V_{IH.AC}$ level for a rising signal and $V_{IL.AC}$ for a falling signal applied to the device under test. See **Figure 10**.
24) These parameters are measured from a command/address signal (CKE, CS, RAS, CAS, WE, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK / $\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT.PER}$, $t_{JIT.CC}$, etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.
25) t_{QH} = t_{HP} – t_{QHS}, where: t_{HP} is the minimum of the absolute half period of the actual input clock; and t_{QHS} is the specification value under the max column. {The less half-pulse width distortion present, the larger the t_{QH} value is; and the larger the valid data eye will be.} Examples: 1) If the system provides t_{HP} of 1315 ps into a DDR2–667 SDRAM, the DRAM provides t_{QH} of 975 ps minimum. 2) If the system provides t_{HP} of 1420 ps into a DDR2–667 SDRAM, the DRAM provides t_{QH} of 1080 ps minimum.
26) t_{QHS} accounts for: 1) The pulse duration distortion of on-chip clock circuits, which represents how well the actual t_{HP} at the input is transferred to the output; and 2) The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and pchannel to n-channel variation of the output drivers.
27) The Auto-Refresh command interval has be reduced to 3.9 µs when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
28) 0 °C≤ T_{CASE} ≤ 85 °C
29) 85 °C < T_{CASE} ≤ 95 °C
30) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
31) t_{RPST} end point and t_{RPRE} begin point are not referenced to a specific voltage level but specify when the device output is no longer driving (t_{RPST}), or begins driving (t_{RPRE}). **Figure 8** shows a method to calculate these points when the device is no longer driving (t_{RPST}), or begins driving (t_{RPRE}) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.
32) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.PER}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.PER.MIN}$ = – 72 ps and $t_{JIT.PER.MAX}$ = + 93 ps, then $t_{RPRE.MIN(DERATED)}$ = $t_{RPRE.MIN}$ + $t_{JIT.PER.MIN}$ = 0.9 x $t_{CK.AVG}$ – 72 ps = + 2178 ps and $t_{RPRE.MAX(DERATED)}$ = $t_{RPRE.MAX}$ + $t_{JIT.PER.MAX}$ = 1.1 x $t_{CK.AVG}$ + 93 ps = + 2843 ps. (Caution on the MIN/MAX usage!).

33) When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT.DUTY}$ of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR2–667 SDRAM has $t_{JIT.DUTY.MIN}$ = – 72 ps and $t_{JIT.DUTY.MAX}$ = + 93 ps, then $t_{RPST.MIN(DERATED)} = t_{RPST.MIN} + t_{JIT.DUTY.MIN}$ = 0.4 x $t_{CK.AVG}$ – 72 ps = + 928 ps and $t_{RPST.MAX(DERATED)} = t_{RPST.MAX} + t_{JIT.DUTY.MAX}$ = 0.6 x $t_{CK.AVG}$ + 93 ps = + 1592 ps. (Caution on the MIN/MAX usage!).
34) For these parameters, the DDR2 SDRAM device is characterized and verified to support $t_{nPARAM} = RU\{t_{PARAM} / t_{CK.AVG}\}$, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support $t_{nRP} = RU\{t_{RP} / t_{CK.AVG}\}$, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR2–667 5–5–5, of which t_{RP} = 15 ns, the device will support $t_{nRP} = RU\{t_{RP} / t_{CK.AVG}\}$ = 5, i.e. as long as the input clock jitter specifications are met, Precharge command at Tm and Active command at Tm + 5 is valid even if (Tm + 5 - Tm) is less than 15 ns due to input clock jitter.
35) t_{WTR} is at lease two clocks (2 x t_{CK}) independent of operation frequency.

FIGURE 8
Method for calculating transitions and endpoint

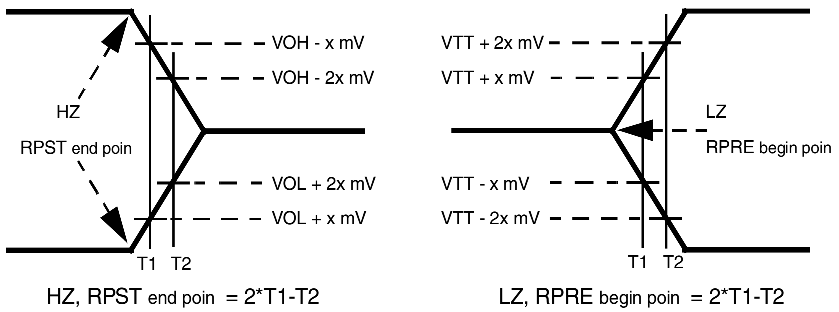


FIGURE 9
Differential input waveform timing - t_{DS} and t_{DS}

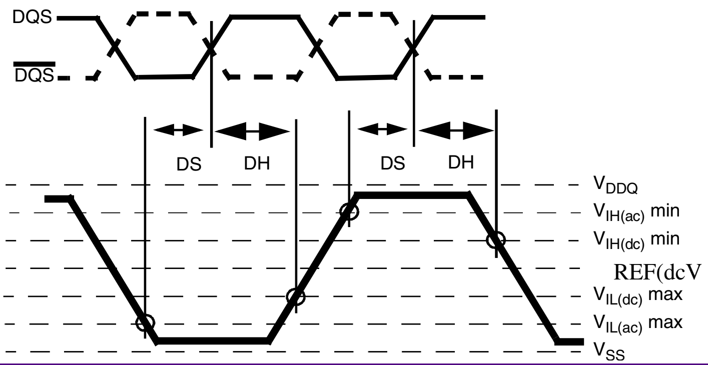


FIGURE 10
Differential input waveform timing - t_{IS} and t_{IH}

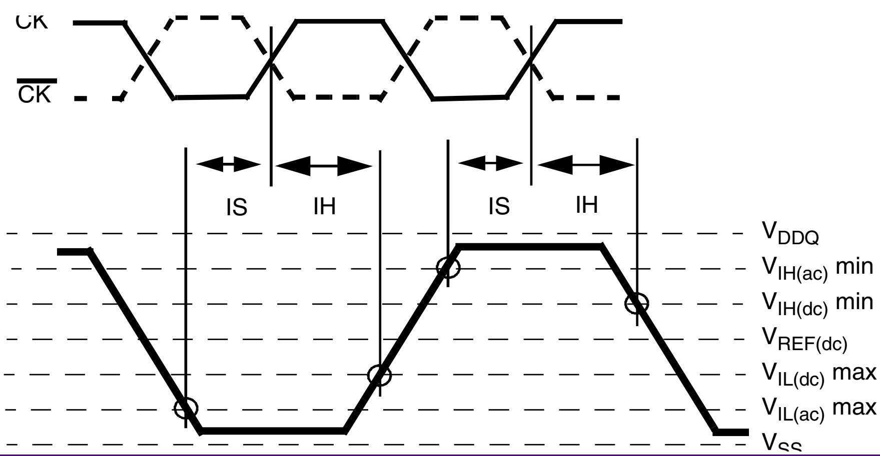


TABLE 54
DRAM Component Timing Parameter by Speed Grade - DDR2–533

Parameter	Symbol	DDR2–533		Unit	Notes[1)2)3)4)5)6)]
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–500	+500	ps	
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	t_{CK}	
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	7)17)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$	—	ns	8)
DQ and DM input hold time (differential data strobe)	t_{DH}(base)	225	—	ps	9)
DQ and DM input hold time (single ended data strobe)	t_{DH1}(base)	–25	—	ps	10)
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–450	+450	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	300	ps	10)
Write command to 1st DQS latching transition	t_{DQSS}	– 0.25	+ 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	t_{DS}(base)	100	—	ps	10)
DQ and DM input setup time (single ended data strobe)	t_{DS1}(base)	–25	—	ps	10)
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	
Clock half period	t_{HP}	MIN. ($t_{CL,}$ t_{CH})			11)
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	12)
Address and control input hold time	t_{IH}(base)	375	—	ps	10)
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	
Address and control input setup time	t_{IS}(base)	250	—	ps	10)
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	$2 \times t_{AC.MIN}$	$t_{AC.MAX}$	ps	13)
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	13)
MRS command to ODT update delay	t_{MOD}	0	12	ns	
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	ns	
Data output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$	—		
Data hold skew factor	t_{QHS}	—	400	ps	

Parameter	Symbol	DDR2–533		Unit	Notes[1)2)3)4)5)6)]
		Min.	Max.		
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	13)14)
Average periodic refresh Interval	t_{REFI}	—	3.9	µs	15)17)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	75	—	ns	16)
Precharge-All (4 banks) command period	t_{RP}	t_{RP}	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	13)
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	13)
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	13)17)
Active bank A to Active bank B command period	t_{RRD}	10	—	ns	15)21)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	
Write preamble	t_{WPRE}	0.25	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	18)
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	
Internal Write to Read command delay	t_{WTR}	7.5	—	ns	19)
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	20)
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	t_{CK}	20)
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	ns	
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}		t_{CK}	21)

1) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ±0.1 V.
2) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
3) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. For other Slew Rates see **Chapter 8** of this datasheet.
4) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode. The input reference level for signals other than CK/$\overline{CK}$, DQS/$\overline{DQS}$, RDQS / $\overline{RDQS}$ is defined in **Chapter 8.3** of this datasheet.
5) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
6) The output timing reference voltage level is V_{TT}. See **Chapter 8** for the reference load for timing measurements.
7) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MR.
8) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode.
9) For timing definition, refer to the Component data sheet.
10) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between DQS / $\overline{DQS}$ and associated DQ in any given cycle.
11) MIN (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).

12) The t_{HZ}, t_{RPST} and t_{LZ}, t_{RPRE} parameters are referenced to a specific voltage level, which specify when the device output is no longer driving (t_{HZ}, t_{RPST}), or begins driving (t_{LZ}, t_{RPRE}). t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions.These parameters are verified by design and characterization, but not subject to production test.
13) The Auto-Refresh command interval has be reduced to 3.9 µs when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
14) 0 °C$\leq T_{CASE} \leq$ 85 °C
15) 85 °C $< T_{CASE} \leq$ 95 °C
16) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
17) The t_{RRD} timing parameter depends on the page size of the DRAM organization. See **Table 5 "Ordering Information for Lead-Free Products (RoHS Compliant)" on Page 6**.
18) The maximum limit for the t_{WPST} parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
19) Minimum t_{WTR} is two clocks when operating the DDR2-SDRAM at frequencies $\leq$ 200 MHz.
20) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In "standard active power-down mode" (MR, A12 = "0") a fast power-down exit timing t_{XARD} can be used. In "low active power-down mode" (MR, A12 ="1") a slow power-down exit timing t_{XARDS} has to be satisfied.
21) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where WR_{MIN}[cycles] = t_{WR}(ns)/t_{CK}(ns) rounded up to the next integer value. t_{DAL} = WR + (t_{RP}/t_{CK}). For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.

TABLE 55
DRAM Component Timing Parameter by Speed Grade - DDR2-400

Parameter	Symbol	DDR2–400		Unit	Notes 1)2)3)4)5)6)
		Min.	Max.		
DQ output access time from CK / $\overline{CK}$	t_{AC}	–600	+600	ps	
$\overline{CAS}$ A to $\overline{CAS}$ B command period	t_{CCD}	2	—	t_{CK}	
CK, $\overline{CK}$ high-level width	t_{CH}	0.45	0.55	t_{CK}	
CKE minimum high and low pulse width	t_{CKE}	3	—	t_{CK}	
CK, $\overline{CK}$ low-level width	t_{CL}	0.45	0.55	t_{CK}	
Auto-Precharge write recovery + precharge time	t_{DAL}	WR + t_{RP}	—	t_{CK}	7)20)
Minimum time clocks remain ON after CKE asynchronously drops LOW	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$	—	ns	8)
DQ and DM input hold time (differential data strobe)	t_{DH}(base)	275	—	ps	9)
DQ and DM input hold time (single ended data strobe)	t_{DH1}(base)	–25	—	ps	10)
DQ and DM input pulse width (each input)	t_{DIPW}	0.35	—	t_{CK}	
DQS output access time from CK / $\overline{CK}$	t_{DQSCK}	–500	+500	ps	
DQS input low (high) pulse width (write cycle)	$t_{DQSL,H}$	0.35	—	t_{CK}	
DQS-DQ skew (for DQS & associated DQ signals)	t_{DQSQ}	—	350	ps	10)
Write command to 1st DQS latching transition	t_{DQSS}	– 0.25	+ 0.25	t_{CK}	
DQ and DM input setup time (differential data strobe)	t_{DS}(base)	150	—	ps	10)
DQ and DM input setup time (single ended data strobe)	t_{DS1}(base)	–25	—	ps	10)

Parameter	Symbol	DDR2–400		Unit	Notes[1)2)3)4)5)6)]
		Min.	Max.		
DQS falling edge hold time from CK (write cycle)	t_{DSH}	0.2	—	t_{CK}	
DQS falling edge to CK setup time (write cycle)	t_{DSS}	0.2	—	t_{CK}	
Clock half period	t_{HP}	MIN. (t_{CL}, t_{CH})			11)
Data-out high-impedance time from CK / $\overline{CK}$	t_{HZ}	—	$t_{AC.MAX}$	ps	12)
Address and control input hold time	t_{IH}(base)	475	—	ps	10)
Address and control input pulse width (each input)	t_{IPW}	0.6	—	t_{CK}	
Address and control input setup time	t_{IS}(base)	350	—	ps	10)
DQ low-impedance time from CK / $\overline{CK}$	$t_{LZ(DQ)}$	$2 \times t_{AC.MIN}$	$t_{AC.MAX}$	ps	13)
DQS low-impedance from CK / $\overline{CK}$	$t_{LZ(DQS)}$	$t_{AC.MIN}$	$t_{AC.MAX}$	ps	13)
MRS command to ODT update delay	t_{MOD}	0	12	ns	
Mode register set command cycle time	t_{MRD}	2	—	t_{CK}	
OCD drive mode output delay	t_{OIT}	0	12	ns	
Data output hold time from DQS	t_{QH}	$t_{HP} - t_{QHS}$		—	
Data hold skew factor	t_{QHS}	—	450	ps	
Average periodic refresh Interval	t_{REFI}	—	7.8	µs	13)14)
Average periodic refresh Interval	t_{REFI}	—	3.9	µs	15)17)
Auto-Refresh to Active/Auto-Refresh command period	t_{RFC}	75	—	ns	16)
Precharge-All (4 banks) command period	t_{RP}	t_{RP}	—	ns	
Read preamble	t_{RPRE}	0.9	1.1	t_{CK}	13)
Read postamble	t_{RPST}	0.40	0.60	t_{CK}	13)
Active bank A to Active bank B command period	t_{RRD}	7.5	—	ns	13)17)
Active bank A to Active bank B command period	t_{RRD}	10	—	ns	15)21)
Internal Read to Precharge command delay	t_{RTP}	7.5	—	ns	
Write preamble	t_{WPRE}	0.25	—	t_{CK}	
Write postamble	t_{WPST}	0.40	0.60	t_{CK}	18)
Write recovery time for write without Auto-Precharge	t_{WR}	15	—	ns	
Internal Write to Read command delay	t_{WTR}	10	—	ns	19)
Exit power down to any valid command (other than NOP or Deselect)	t_{XARD}	2	—	t_{CK}	20)
Exit active power-down mode to Read command (slow exit, lower power)	t_{XARDS}	6 – AL	—	t_{CK}	20)
Exit precharge power-down to any valid command (other than NOP or Deselect)	t_{XP}	2	—	t_{CK}	
Exit Self-Refresh to non-Read command	t_{XSNR}	t_{RFC} +10	—	ns	

Parameter	Symbol	DDR2–400		Unit	Notes[1)2)3)4)5)6)]
		Min.	Max.		
Exit Self-Refresh to Read command	t_{XSRD}	200	—	t_{CK}	
Write recovery time for write with Auto-Precharge	WR	t_{WR}/t_{CK}		t_{CK}	21)

1) V_{DDQ} = 1.8 V ± 0.1 V; V_{DD} = 1.8 V ±0.1 V.
2) Timing that is not specified is illegal and after such an event, in order to guarantee proper operation, the DRAM must be powered down and then restarted through the specified initialization sequence before normal operation can continue.
3) Timings are guaranteed with CK/$\overline{CK}$ differential Slew Rate of 2.0 V/ns. For DQS signals timings are guaranteed with a differential Slew Rate of 2.0 V/ns in differential strobe mode and a Slew Rate of 1 V/ns in single ended mode. For other Slew Rates see **Chapter 8** of this datasheet.
4) The CK / $\overline{CK}$ input reference level (for timing reference to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS / $\overline{DQS}$, RDQS / $\overline{RDQS}$, input reference level is the crosspoint when in differential strobe mode. The input reference level for signals other than CK/$\overline{CK}$, DQS/$\overline{DQS}$, RDQS / $\overline{RDQS}$ is defined in **Chapter 8.3** of this datasheet.
5) Inputs are not recognized as valid until V_{REF} stabilizes. During the period before V_{REF} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low.
6) The output timing reference voltage level is V_{TT}. See **Chapter 8** for the reference load for timing measurements.
7) For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MR.
8) The clock frequency is allowed to change during self-refresh mode or precharge power-down mode.
9) For timing definition, refer to the Component data sheet.
10) Consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers as well as output Slew Rate mis-match between DQS / $\overline{DQS}$ and associated DQ in any given cycle.
11) MIN (t_{CL}, t_{CH}) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for t_{CL} and t_{CH}).
12) The t_{HZ}, t_{RPST} and t_{LZ}, t_{RPRE} parameters are referenced to a specific voltage level, which specify when the device output is no longer driving (t_{HZ}, t_{RPST}), or begins driving (t_{LZ}, t_{RPRE}). t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions.These parameters are verified by design and characterization, but not subject to production test.
13) The Auto-Refresh command interval has be reduced to 3.9 µs when operating the DDR2 DRAM in a temperature range between 85 °C and 95 °C.
14) 0 °C≤ T_{CASE} ≤ 85 °C
15) 85 °C < T_{CASE} ≤ 95 °C
16) A maximum of eight Auto-Refresh commands can be posted to any given DDR2 SDRAM device.
17) The t_{RRD} timing parameter depends on the page size of the DRAM organization. See **Table 5 “Ordering Information for Lead-Free Products (RoHS Compliant)” on Page 6**.
18) The maximum limit for the t_{WPST} parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) degrades accordingly.
19) Minimum t_{WTR} is two clocks when operating the DDR2-SDRAM at frequencies ≤ 200 MHz.
20) User can choose two different active power-down modes for additional power saving via MRS address bit A12. In “standard active power-down mode” (MR, A12 = “0”) a fast power-down exit timing t_{XARD} can be used. In “low active power-down mode” (MR, A12 =”1”) a slow power-down exit timing t_{XARDS} has to be satisfied.
21) WR must be programmed to fulfill the minimum requirement for the t_{WR} timing parameter, where WR_{MIN}[cycles] = t_{WR}(ns)/t_{CK}(ns) rounded up to the next integer value. t_{DAL} = WR + (t_{RP}/t_{CK}). For each of the terms, if not already an integer, round to the next highest integer. t_{CK} refers to the application clock period. WR refers to the WR parameter stored in the MRS.

7.3 Jitter Definition and Clock Jitter Specification

Generally, jitter is defined as “the short-term variation of a signal with respect to its ideal position in time”. The following table provides an overview of the terminology.

TABLE 56
Average Clock and Jitter Symbols and Definition

Symbol	Parameter	Description	Units
$t_{CK.AVG}$	Average clock period	$t_{CK.AVG}$ is calculated as the average clock period within any consecutive 200-cycle window: $$tCK.AVG = \frac{1}{N} \cdot \left(\sum_{j=1}^{N} tCK_j \right) \quad (1)$$ N = 200	ps
$t_{JIT.PER}$	Clock-period jitter	$t_{JIT.PER}$ is defined as the largest deviation of any single t_{CK} from $t_{CK.AVG}$: $t_{JIT.PER}$ = Min/Max of $\{t_{CKi} - t_{CK.AVG}\}$ where i = 1 to 200 $t_{JIT.PER}$ defines the single-period jitter when the DLL is already locked. $t_{JIT.PER}$ is not guaranteed through final production testing.	ps
t_{JIT}(PER, LCK)	Clock-period jitter during DLL-locking period	t_{JIT}(PER,LCK) uses the same definition as $t_{JIT.PER}$, during the DLL-locking period only. t_{JIT}(PER,LCK) is not guaranteed through final production testing.	ps
$t_{JIT.CC}$	Cycle-to-cycle clock period jitter	$t_{JIT.CC}$ is defined as the absolute difference in clock period between two consecutive clock cycles: $t_{JIT.CC}$ = Max of ABS$\{t_{CKi+1} - t_{CKi}\}$ $t_{JIT.CC}$ defines the cycle- to- cycle jitter when the DLL is already locked. $t_{JIT.CC}$ is not guaranteed through final production testing.	ps
t_{JIT}(CC, LCK)	Cycle-to-cycle clock period jitter during DLL-locking period	t_{JIT}(CC,LCK) uses the same definition as $t_{JIT.CC}$ during the DLL-locking period only. t_{JIT}(CC,LCK) is not guaranteed through final production testing.	ps
$t_{ERR.2PER}$	Cumulative error across 2 cycles	$t_{ERR.2PER}$ is defined as the cumulative error across 2 consecutive cycles from $t_{CK.AVG}$: $$tERR(2per) = \left(\sum_{j=i}^{i+n-1} tCK_j \right) - n \times tCK(avg) \quad (2)$$ n = 2 for t_{ERR}(2per) where i = 1 to 200	ps

Symbol	Parameter	Description	Units
$t_{ERR.nPER}$	Cumulative error across n cycles	$t_{ERR.2PER}$ is defined as the cumulative error across n consecutive cycles from $t_{CK.AVG}$: $$tERR(nper) = \left(\sum_{j=i}^{i+n-1} tCK_j\right) - n \times tCK(avg) \quad (3)$$ where, i = 1 to 200 and n = 3 for $t_{ERR.3PER}$ n = 4 for $t_{ERR.4PER}$ n = 5 for $t_{ERR.5PER}$ $6 \leq n \leq 10$ for $t_{ERR.6-10PER}$ $11 \leq n \leq 50$ for $t_{ERR.11-50PER}$	ps
$t_{CH.AVG}$	Average high-pulse width	$t_{CH.AVG}$ is defined as the average high-pulse width, as calculated across any consecutive 200 high pulses: $$tCH(avg) = \frac{1}{(N \times tCK(avg))} \cdot \left(\sum_{j=1}^{N} tCH_j\right) \quad (4)$$ N = 200	$t_{CK.AVG}$
$t_{CL.AVG}$	Average low-pulse width	$t_{CL.AVG}$ is defined as the average low-pulse width, as calculated across any consecutive 200 low pulses: $$tCL(avg) = \frac{1}{(N \times tCK(avg))} \cdot \left(\sum_{j=1}^{N} tCL_j\right) \quad (5)$$ N = 200	$t_{CK.AVG}$
$t_{JIT.DUTY}$	Duty-cycle jitter	$t_{JIT.DUTY}$ = Min/Max of $\{t_{JIT.CH}, t_{JIT.CL}\}$, where: $t_{JIT.CH}$ is the largest deviation of any single t_{CH} from $t_{CH.AVG}$ $t_{JIT.CL}$ is the largest deviation of any single t_{CL} from $t_{CL.AVG}$ $t_{JIT.CH} = \{t_{CHi} - t_{CH.AVG} \times t_{CK.AVG}\}$ where i=1 to 200 $t_{JIT.CL} = \{t_{CLi} - t_{CL.AVG} \times t_{CK.AVG}\}$ where i=1 to 200	ps

The following parameters are specified per their average values however, it is understood that the following relationship between the average timing and the absolute instantaneous timing holds all the time.

TABLE 57
Absolute Jitter Value Definitions

Symbol	Parameter	Min.	Max.	Unit
$t_{CK.ABS}$	Clock period	$t_{CK.AVG(Min)} + t_{JIT.PER(Min)}$	$t_{CK.AVG(Max)} + t_{JIT.PER(Max)}$	ps
$t_{CH.ABS}$	Clock high-pulse width	$t_{CH.AVG(Min)}$ x $t_{CK.AVG(Min)} + t_{JIT.DUTY(Min)}$	$t_{CH.AVG(Max)}$ x $t_{CK.AVG(Max)} + t_{JIT.DUTY(Max)}$	ps
$t_{CL.ABS}$	Clock low-pulse width	$t_{CL.AVG(Min)}$ x $t_{CK.AVG(Min)} + t_{JIT.DUTY(Min)}$	$t_{CL.AVG(Max)}$ x $t_{CK.AVG(Max)} + t_{JIT.DUTY(Max)}$	ps

Example: for DDR2-667, $t_{CH.ABS.MIN}$ = (0.48 x 3000ps) – 125 ps = 1315 ps = 0.438 x 3000 ps.

Table 58 shows clock-jitter specifications.

TABLE 58
Clock-Jitter Specifications for –667 and –800

Symbol	Parameter	DDR2 -667		DDR2 -800		Unit
		Min.	Max.	Min.	Max.	
$t_{CK.AVG}$	Average clock period nominal w/o jitter	3000	8000	2500	8000	ps
$t_{JIT.PER}$	Clock-period jitter	–125	+125	–100	+100	ps
$t_{JIT(PER,LCK)}$	Clock-period jitter during DLL locking period	–100	+100	–80	+80	ps
$t_{JIT.CC}$	Cycle-to-cycle clock-period jitter	–250	+250	–200	+200	ps
$t_{JIT(CC,LCK)}$	Cycle-to-cycle clock-period jitter during DLL-locking period	–200	+200	–160	+160	ps
$t_{ERR.2PER}$	Cumulative error across 2 cycles	–175	+175	–150	+150	ps
$t_{ERR.3PER}$	Cumulative error across 3 cycles	–225	+225	–175	+175	ps
$t_{ERR.4PER}$	Cumulative error across 4 cycles	–250	+250	–200	+200	ps
$t_{ERR.5PER}$	Cumulative error across 5 cycles	–250	+250	–200	+200	ps
$t_{ERR(6-10PER)}$	Cumulative error across n cycles with n = 6 .. 10, inclusive	–350	+350	–300	+300	ps
$t_{ERR(11-50PER)}$	Cumulative error across n cycles with n = 11 .. 50, inclusive	–450	+450	–450	+450	ps
$t_{CH.AVG}$	Average high-pulse width	0.48	0.52	0.48	0.52	$t_{CK.AVG}$
$t_{CL.AVG}$	Average low-pulse width	0.48	0.52	0.48	0.52	$t_{CK.AVG}$
$t_{JIT.DUTY}$	Duty-cycle jitter	–125	+125	–100	+100	ps

7.4 ODT AC Electrical Characteristics

This chapter describes the ODT AC electrical characteristics.

TABLE 59
ODT AC Characteristics and Operating Conditions for DDR2-533 and DDR2-400

Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	t_{CK}	
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 1 ns	ns	1)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{AOFD}	ODT turn-off delay	2.5	2.5	t_{CK}	
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	2)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	t_{CK}	
t_{AXPD}	ODT Power Down Exit Latency	8	—	t_{CK}	

1) ODT turn on time min. is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from t_{AOND}, which is interpreted differently per speed bin. For DDR2-400/533, t_{AOND} is 10 ns (= 2 x 5 ns) after the clock edge that registered a first ODT HIGH if t_{CK} = 5 ns.
2) ODT turn off time min. is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}. Both are measured from t_{AOFD}, which is interpreted differently per speed bin. For DDR2-400/533, t_{AOFD} is 12.5 ns (= 2.5 x 5 ns) after the clock edge that registered a first ODT HIGH if t_{CK} = 5 ns.

TABLE 60
ODT AC Characteristics and Operating Conditions for DDR2-667 and DDR2-800

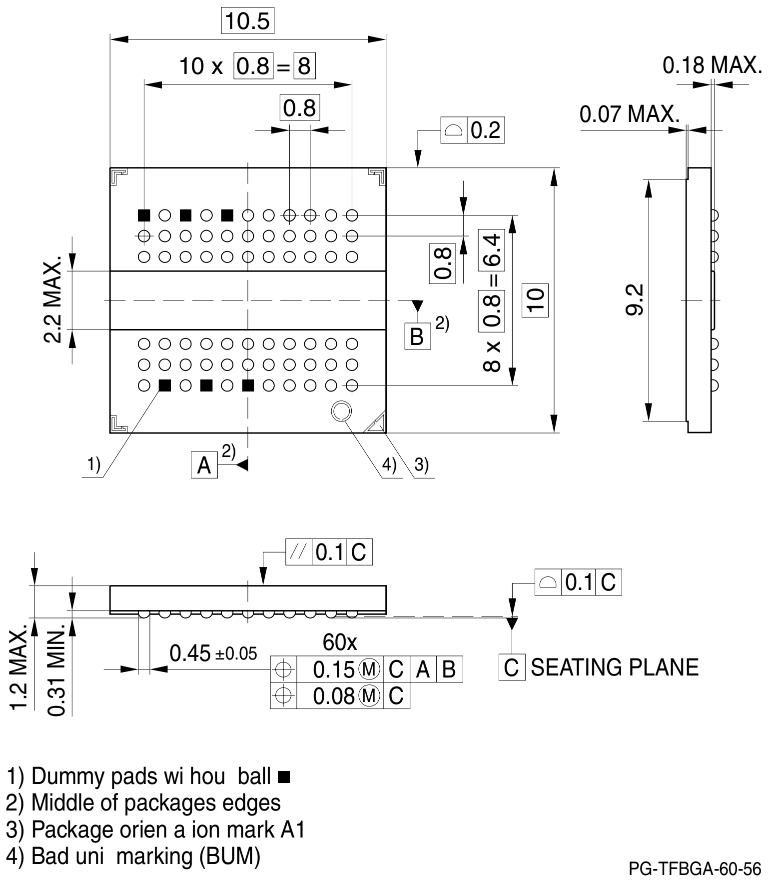
Symbol	Parameter / Condition	Values		Unit	Note
		Min.	Max.		
t_{AOND}	ODT turn-on delay	2	2	n_{CK}	1)
t_{AON}	ODT turn-on	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.7 ns	ns	1)2)
t_{AONPD}	ODT turn-on (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	1)
t_{AOFD}	ODT turn-off delay	2.5	2.5	n_{CK}	1)
t_{AOF}	ODT turn-off	$t_{AC.MIN}$	$t_{AC.MAX}$ + 0.6 ns	ns	1)3)
t_{AOFPD}	ODT turn-off (Power-Down Modes)	$t_{AC.MIN}$ + 2 ns	2.5 t_{CK} + $t_{AC.MAX}$ + 1 ns	ns	1)
t_{ANPD}	ODT to Power Down Mode Entry Latency	3	—	n_{CK}	1)
t_{AXPD}	ODT Power Down Exit Latency	8	—	n_{CK}	1)

1) New units, "$t_{CK.AVG}$" and "n_{CK}", are introduced in DDR2-667 and DDR2-800. Unit "$t_{CK.AVG}$" represents the actual $t_{CK.AVG}$ of the input clock under operation. Unit "n_{CK}" represents one clock cycle of the input clock, counting the actual clock edges. Note that in DDR2-400 and DDR2-533, "t_{CK}" is used for both concepts. Example: t_{XP} = 2 [n_{CK}] means; if Power Down exit is registered at T_m, an Active command may be registered at T_m + 2, even if (T_m + 2 - T_m) is 2 x $t_{CK.AVG}$ + $t_{ERR.2PER(Min)}$.
2) ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on. ODT turn on time max is when the ODT resistance is fully on. Both are measured from t_{AOND}, which is interpreted differently per speed bin. For DDR2-667/800, t_{AOND} is 2 clock cycles after the clock edge that registered a first ODT HIGH counting the actual input clock edges.
3) ODT turn off time min is when the device starts to turn off ODT resistance. ODT turn off time max is when the bus is in high impedance. Both are measured from t_{AOFD}, which is interpreted differently per speed bin. For DDR2-667/800, if $t_{CK(avg)}$ = 3 ns is assumed, t_{AOFD} is 1.5 ns (= 0.5 x 3 ns) after the second trailing clock edge counting from the clock edge that registered a first ODT LOW and by counting the actual input clock edges.

8 Package Dimensions

This chapter contains the package dimension figures.

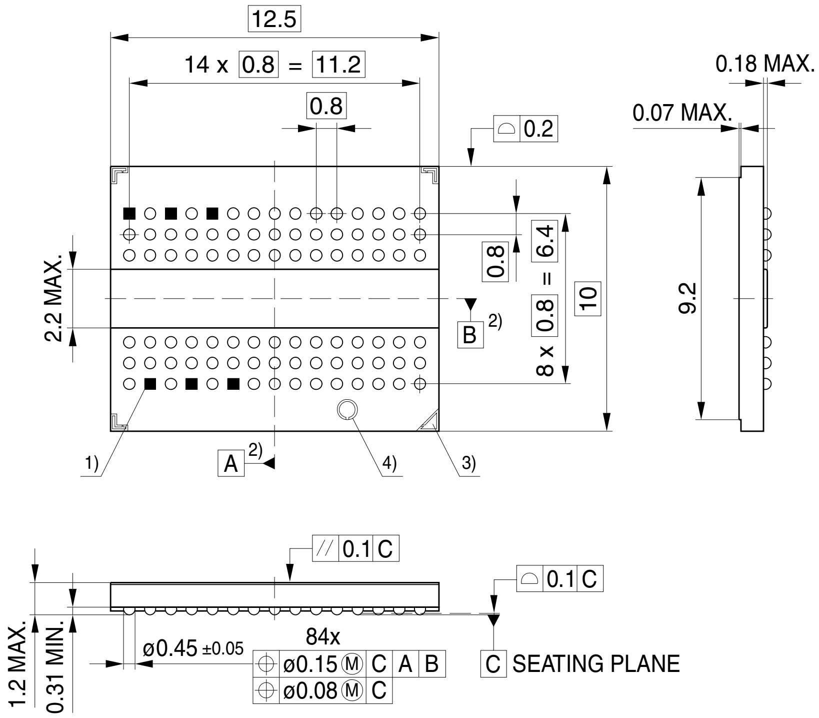
FIGURE 11
Package Outline P(G)-TFBGA-60



Notes

1. *Drawing according to ISO 8015*
2. *Dimensions in mm*
3. *General tolerances +/- 0.15*

FIGURE 12
Package Outline P(G)-TFBGA-84



1) Dummy pads wi hou ball ■
2) Middle of packages edges
3) Package orien a ion mark A1
4) Bad uni marking (BUM)

PG-TFBGA-84-55

Notes

1. *Drawing according to ISO 8015*
2. *Dimensions in mm*
3. *General tolerances +/- 0.15*

9 Product Nomenclature

For reference the Qimonda SDRAM component nomenclature is enclosed in this chapter.

TABLE 61
Examples for Nomenclature Fields

Example for	Field Number										
	1	2	3	4	5	6	7	8	9	10	11
DDR2 SDRAM	HYB	18	T	256	40		0	A	F		–3
DDR2 SDRAM	HYI	18	T	256	16		0	B	F	L	–3.7

TABLE 62
DDR2 Memory Components

Field	Description	Values	Coding
1	Qimonda Component Prefix	HYB	Memory components
		HYI	Memory components, industrial temperature range (-40°C – +85 °C)
2	Interface Voltage [V]	18	SSTL_18
3	DRAM Technology	T	DDR2
4	Component Density [Mbit]	256	256 Mbit
		512	512 Mbit
		1G	1 Gbit
		2G	2 Gbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	look up table
8	Die Revision	A(0 ..9)	First
		B(0 ..9)	Second
		C(0 ..9)	Third
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free
10	Power	–	Standard power product
		L	Low power product

Field	Description	Values	Coding
11	Speed Grade	–1.9	DDR2–1066
		–25F	DDR2–800 5–5–5
		–2.5	DDR2–800 6–6–6
		–3	DDR2–667 4–4–4
		–3S	DDR2–667 5–5–5
		–3.7	DDR2–533 4–4–4
		–5	DDR2–400 3–3–3

List of Figures

List of Tables

Table of Contents

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Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Qimonda Office.

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Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Qimonda Office.
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