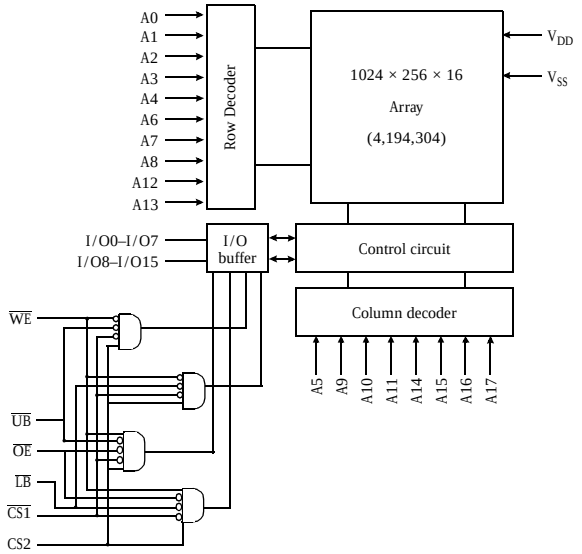
1.65V to 3.6V 256K×16 Intelliwatt™ low power CMOS SRAM with two Chip Enables

Features

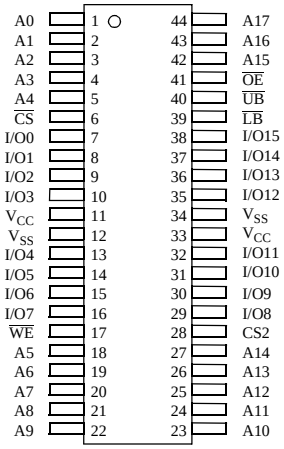
- AS6UA25617
- Intelliwatt™ active power circuitry
- Industrial temperature: -40° C to 85° C
- Organization: 262,144 words × 16 bits
- 2.7V to 3.6V at 55 ns
- 2.3V to 2.7V at 70 ns
- 1.65V to 2.3V at 100 ns
- $\overline{CS1}$ and CS2 for chip selection
- Low power consumption: ACTIVE
  - 54 mW at 3.6V and 55 ns
  - 27 mW at 2.7V and 70 ns
  - 14 mW at 2.3 V and 100 ns
- Low power consumption: STANDBY
  - 29 µW max at 3.6V
  - 11 µW max at 2.7V
  - 9 µW max at 2.3V
- 1.2V data retention
- Equal access and cycle times
- Easy memory expansion with $\overline{CS}$, $\overline{OE}$ inputs
- Smallest footprint package
  - 44-pin TSOP II
  - 48-ball FBGA
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram



Pin arrangement (top view)

TSOP II



48-CSP Ball-Grid-Array Package

	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A_0	A_1	A_2	CS2
B	I/O_8	$\overline{UB}$	A_3	A_4	$\overline{CS1}$	I/O_0
C	I/O_9	I/O_{10}	A_5	A_6	I/O_1	I/O_2
D	V_{SS}	I/O_{11}	A_{17}	A_7	I/O_3	V_{CC}
E	V_{CC}	I/O_{12}	NC	A_{16}	I/O_4	V_{SS}
F	I/O_{14}	I/O_{13}	A_{14}	A_{15}	I/O_5	I/O_6
G	I/O_{15}	NC	A_{12}	A_{13}	$\overline{WE}$	I/O_7
H	NC	A_8	A_9	A_{10}	A_{11}	NC

Selection guide

Product	V_{CC} Range Min (V)	V_{CC} Range Typ[2] (V)	V_{CC} Range Max (V)	Speed (ns)	Power Dissipation (Industrial) Operating (I_{CC}) Max (mA)	Power Dissipation (Industrial) Standby (I_{SB2}) Max (µA)
AS6UA25617	2.7	3.0	3.6	55	15	8
AS6UA25617	2.3	2.5	2.7	70	10	4
AS6UA25617*	1.65	2.0	2.3	100	7	4

* Advance information.

Functional description

The AS6UA25617 is a low-power CMOS 4,194,304-bit Static Random Access Memory (SRAM) device organized as 262,144 words × 16 bits. It is designed for memory applications where slow data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 55/70/100 ns are ideal for low-power applications. Active high and low chip enables ($\overline{CS1}$ and CS2) permit easy memory expansion with multiple-bank memory systems.

When $\overline{CS1}$ is high, or $\overline{UB}$ and $\overline{LB}$ are high or CS2 is low, the device enters standby mode: the AS6UA25617 is guaranteed not to exceed 28 µW power consumption at 3.6V and 5 5ns; 100 µW at 2.7V and 70 ns; or 60 µW at 2.3V and 100 ns. The device also returns data when V_{CC} is reduced to 1.5V for even lower power consumption.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CS1}$) low, $\overline{UB}$ and/or $\overline{LB}$ low, and CS2 high. Data on the input pins I/O0-I/O15 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CS1}$, CS2 (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$), chip enable ($\overline{CS1}$) low, $\overline{UB}$ and/or $\overline{LB}$ low, with write enable ($\overline{WE}$) and CS2 high. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, or ($\overline{UB}$) and ($\overline{LB}$), output drivers stay in high-impedance mode.

This device provides multiple center power and ground pins, and separate byte enable controls, allowing individual bytes to be written and read. $\overline{LB}$ controls the lower bits, I/O0–I/O7, and $\overline{UB}$ controls the higher bits, I/O8–I/O15.

All chip inputs and outputs are CMOS-compatible, and operation is from either a single 1.65V to 3.6V supply. Device is available in the JEDEC standard 48-ball FBGA and the 44-pin TSOPII packages.

Absolute maximum ratings

Parameter	Device	Symbol	Min	Max	Unit
Voltage on V_{CC} relative to V_{SS}		V_{tIN}	–0.5	V_{CC} + 0.5	V
Voltage on any I/O pin relative to GND		$V_{tI/O}$	–0.5		V
Power dissipation		P_D	–	1.0	W
Storage temperature (plastic)		T_{stg}	–65	+150	°C
Temperature with V_{CC} applied		T_{bias}	–55	+125	°C
DC output current (low)		I_{OUT}	–	20	mA

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O_{1-8}	I/O_{9-16}	Mode	Power
H	X	X	X	X	X	High-Z	High-Z	Deselected	Standby
X	L	X	X	X	X	High-Z	High-Z	Deselected	Standby
X	X	X	X	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	D_{OUT}	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	D_{OUT}	Upper Byte Read	Active
L	H	L	H	L	L	D_{OUT}	D_{OUT}	Word Read	Active
L	H	X	L	L	H	D_{IN}	High-Z	Lower Byte Write	Active
L	H	X	L	H	L	High-Z	D_{IN}	Upper Byte Write	Active
L	H	X	L	L	L	D_{IN}	D_{IN}	Word Write	Active

Key: X = Don't care, L = Low, H = High

Recommended operating condition (over the operating range)

Parameter	Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = 2.1mA	V_{CC} = 2.7V	2.4		V
		I_{OH} = 1.5mA	V_{CC} = 2.3V	2.0		
		I_{OH} = 1.65mA	V_{CC} = 1.65V	1.5		
V_{OL}	Output LOW Voltage	I_{OL} = 2.1mA	V_{CC} = 2.7V		0.4	V
		I_{OL} = 0.5mA	V_{CC} = 2.3V		0.4	
		I_{OL} = 0.1mA	V_{CC} = 1.65V		0.2	
V_{IH}	Input HIGH Voltage		V_{CC} = 2.7V	2.2	V_{CC} + 0.5	V
			V_{CC} = 2.3V	2.0	V_{CC} + 0.3	
			V_{CC} = 1.65V	1.4	V_{CC} + 0.3	
V_{IL}	Input LOW Voltage		V_{CC} = 2.7V	-0.5	0.8	V
			V_{CC} = 2.3V	-0.3	0.6	
			V_{CC} = 1.65V	-0.3	0.4	
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		-1	+1	µA
I_{OZ}	Output Load Current	GND ≤ V_O ≤ V_{CC}; Outputs High Z		-1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	I_{OUT} = 0mA	V_{CC} = 3.6V		15	mA
		f = 1 MHz	V_{CC} = 2.7V		10	
		V_{IN} = CMOS	V_{CC} = 2.3V		7	
I_{CC} @ 1 MHz	V_{CC} Operating Supply Current at 1 MHz	I_{OUT} = 0mA	V_{CC} = 3.6V		2	mA
		f = 1 MHz	V_{CC} = 2.7V		1	
		V_{IN} = CMOS	V_{CC} = 2.3V		1	
I_{SB1}	Chip Enable(s) Power Down Current; TTL Inputs	$\overline{CS1}$ ≥ V_{IH}	V_{CC} = 3.6V		100	µA
		CS2 ≤ V_{IL}, or	V_{CC} = 2.7V			
		$\overline{UB}$ = $\overline{LB}$ ≥ V_{IH}				
		V_{IN} ≥ V_{IH}, or	V_{CC} = 2.3V			
		V_{IN} ≤ V_{IL}				
I_{SB2}	Chip Enable(s) Power Down Current; CMOS Inputs	$\overline{CS1}$ ≥ V_{CC} - 0.1V	V_{CC} = 3.6V		8	µA
		CS2 ≤ + 0.1V, or	V_{CC} = 2.7V		4	
		$\overline{UB}$ = $\overline{LB}$ ≥ V_{CC} - 0.1V				
		V_{IN} ≥ V_{CC} - 0.1V or	V_{CC} = 2.3V		4	
		V_{IN} ≤ 0.3V, f = 0				
I_{SBDR}	Data Retention	$\overline{CS1}$ ≥ V_{CC} - 0.1V	V_{CC} = 1.2V		2	µA
		CS2 ≤ + 0.1V, or				
		$\overline{UB}$ = $\overline{LB}$ = V_{CC} - 0.1V				
		V_{IN} ≥ V_{CC} - 0.1V or				
		V_{IN} ≤ 0.1V, f = 0				

Capacitance (f = 1 MHz, T_a = Room temperature, V_{CC} = NOMINAL)[2]

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CS1}$, CS2, $\overline{WE}$, $\overline{OE}$, $\overline{LB}$, $\overline{UB}$	V_{IN} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	V_{IN} = V_{OUT} = 0V	7	pF

SRAM

Read cycle (over the operating range)[3,9]

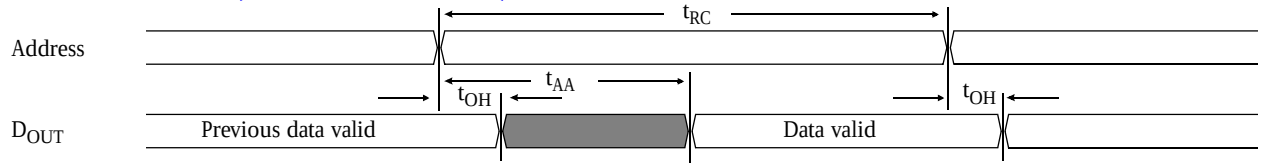
Parameter	Symbol	-55		-70		-100		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	55	–	70	–	100	–	ns	
Address access time	t_{AA}	–	55	–	70	–	100	ns	3
Chip enables access time	$t_{ACS1,2}$	–	55	–	70	–	100	ns	3
Output enable ($\overline{OE}$) access time	t_{OE}	–	25	–	35	–	50	ns	
Output hold from address change	t_{OH}	10	–	10	–	15	–	ns	5
Chip enables low to output in low Z	t_{CLZ}	10	–	10	–	10	–	ns	4, 5
Chip enables high to output in high Z	t_{CHZ}	0	10	0	10	0	10	ns	4, 5
$\overline{OE}$ low to output in low Z	t_{OLZ}	10	–	10	–	10	–	ns	4, 5
$\overline{UB}$/$\overline{LB}$ access time	t_{BA}	–	55	–	70	–	100	ns	
$\overline{UB}$/$\overline{LB}$ low to low Z	t_{BLZ}	10	–	10	–	10	–	ns	4, 5
$\overline{UB}$/$\overline{LB}$ high to high Z	t_{BHZ}	0	10	–	10	–	10	ns	4, 5
$\overline{OE}$ high to output in high Z	t_{OHZ}	0	10	–	10	–	10	ns	4, 5
Power up time	t_{PU}	0	–	0	–	0	–	ns	4, 5
Power down time	t_{PD}	–	55	–	70	–	100	ns	4, 5

Shaded areas indicate preliminary information.

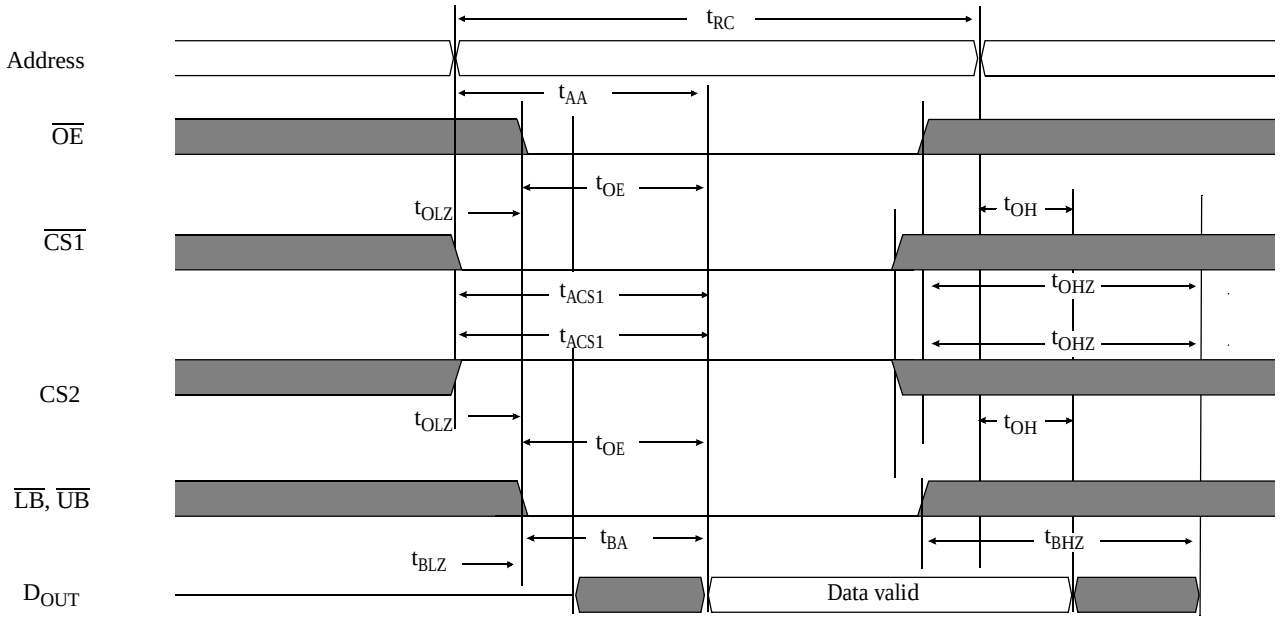
Key to switching waveforms

Rising input Falling input Undefined/don't care

Read waveform 1 (address controlled)[3,6,7,9]



Read waveform 2 (Chip enables, $\overline{OE}$, $\overline{UB}$, $\overline{LB}$ controlled)[3,6,8,9]

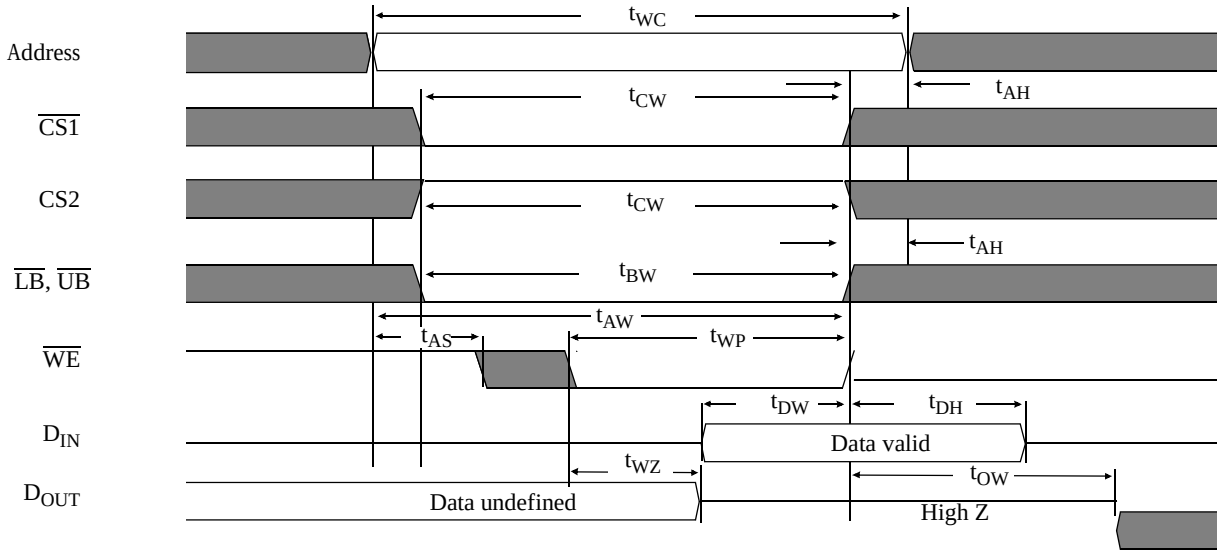


Write cycle (over the operating range)[11]

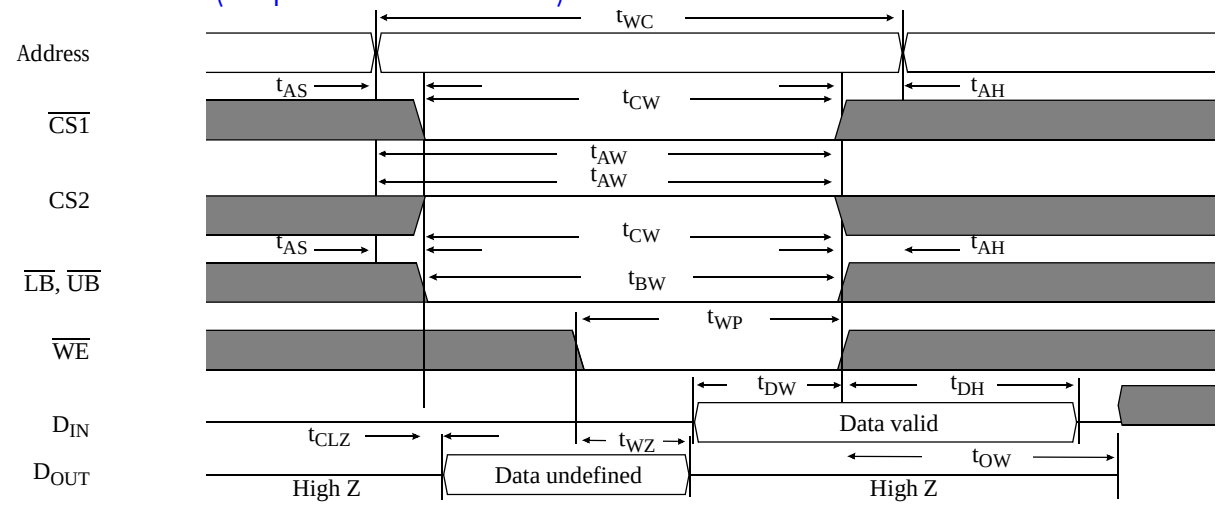
Parameter	Symbol	55		70		100		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	55	–	70	–	100	–	ns	
Chip enable to write end	t_{CW}	40	–	60	–	80	–	ns	12
Address setup to write end	t_{AW}	40	–	60	–	80	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	ns	12
Write pulse width	t_{WP}	35	–	55	–	70	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	25	–	30	–	40	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	ns	4, 5
Write enable to output in high Z	t_{WZ}	0	20	0	20	0	20	ns	4, 5
Output active from write end	t_{OW}	5	–	5	–	5	–	ns	4, 5
$\overline{UB}$/$\overline{LB}$ low to end of write	t_{BW}	35	–	55	–	70	–	ns	

Shaded areas indicate preliminary information.

Write waveform 1 ($\overline{WE}$ controlled)[10,11]



Write waveform 2 (Chip enables controlled)[10,11]

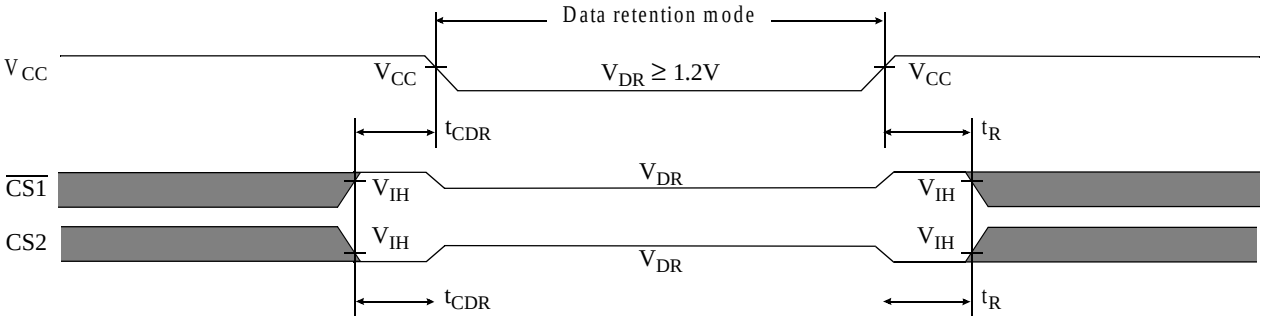


SRAM

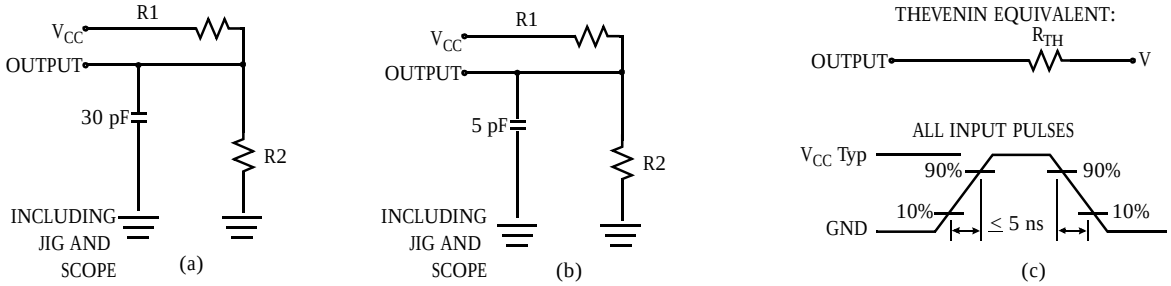
Data retention characteristics (over the operating range)[13,5]

Parameter	Sym	Test conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	V_{CC} = 1.2V $\overline{CS1} \geq V_{CC}-0.1V$ or $\overline{UB} = \overline{LB} > V_{CC} - 0.1V$ $V_{IN} \geq V_{CC}-0.1V$ *or* $V_{IN} \leq 0.1V$	1.2V	–	V
Data retention current	I_{CCDR}		–	2	µA
Chip deselect to data retention time	t_{CDR}		0	–	ns
Operation recovery time	t_R		t_{RC}	–	ns

Data retention waveform



AC test loads and waveforms



Parameters	3.0V	2.5V	2.0V	Unit
R1	1105	16670	15294	Ohms
R2	1550	15380	11300	Ohms
R_{TH}	645	8000	6500	Ohms
V_{TH}	1.75V	1.2V	0.85V	Volts

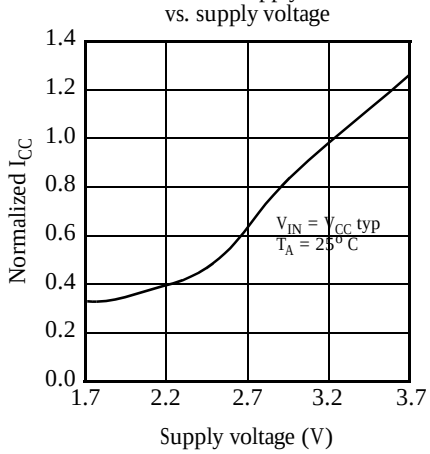
Notes

1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CS1}$ is required to meet I_{SB} specification.
2 This parameter is sampled, but not 100% tested.
3 For test conditions, see *AC Test Conditions*.
4 t_{CLZ} and t_{CHZ} are specified with C_L = 5pF as in Figure C. Transition is measured ±500 mV from steady-state voltage.
5 This parameter is guaranteed, but not tested.
6 $\overline{WE}$ is HIGH for read cycle.
7 $\overline{CS1}$ and $\overline{OE}$ are LOW and CS2 is HIGH for read cycle.
8 Address valid prior to or coincident with $\overline{CS1}$ transition LOW and CS2 HIGH.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CS1}$ or $\overline{WE}$ must be HIGH or CS2 LOW during address transitions. Either $\overline{CE}$ or $\overline{WE}$ asserting high terminates a write cycle.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 N/A.
13 2V data retention applies to commercial temperature range operation only.
14 C=30pF, except at high Z and low Z parameters, where C=5pF.

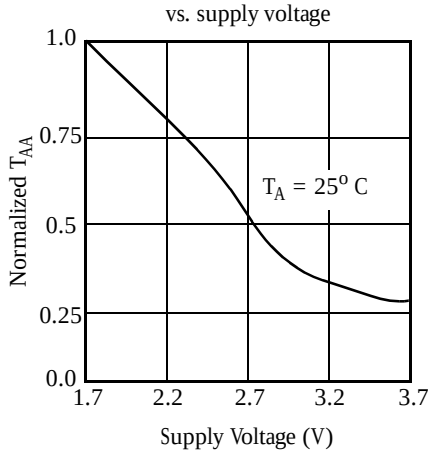
SRAM

Typical DC and AC characteristics

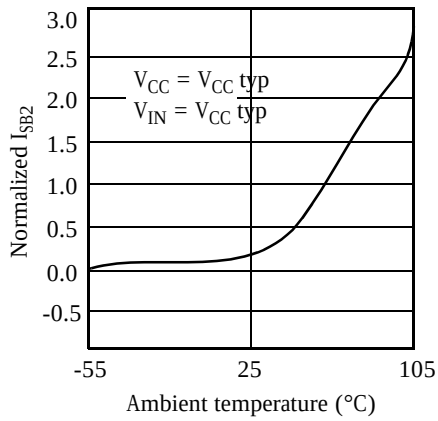
Normalized supply current vs. supply voltage



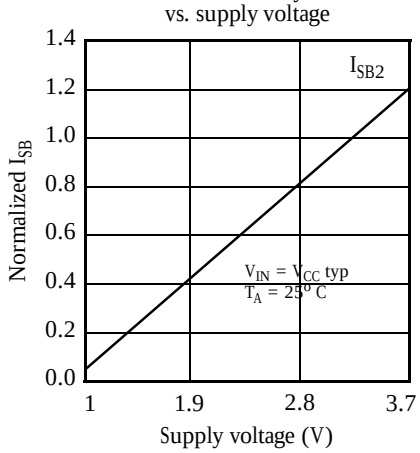
Normalized access time vs. supply voltage



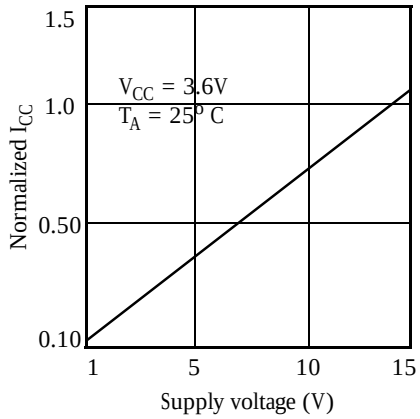
Normalized standby current vs. ambient temperature



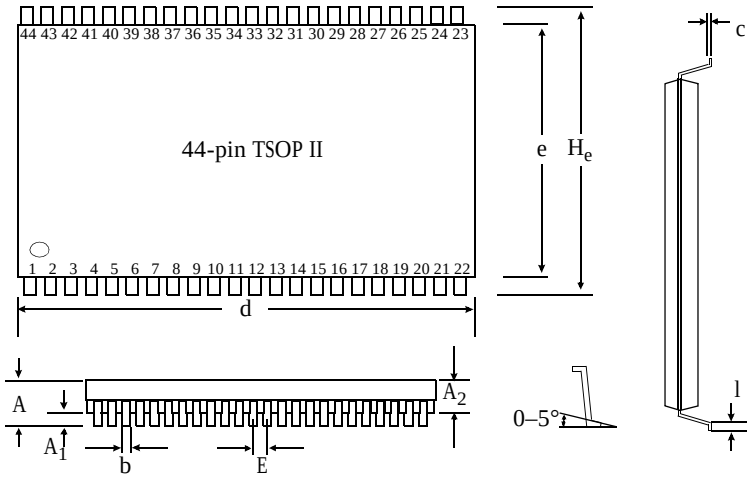
Normalized standby current vs. supply voltage



Normalized I_{CC} vs. Cycle Time



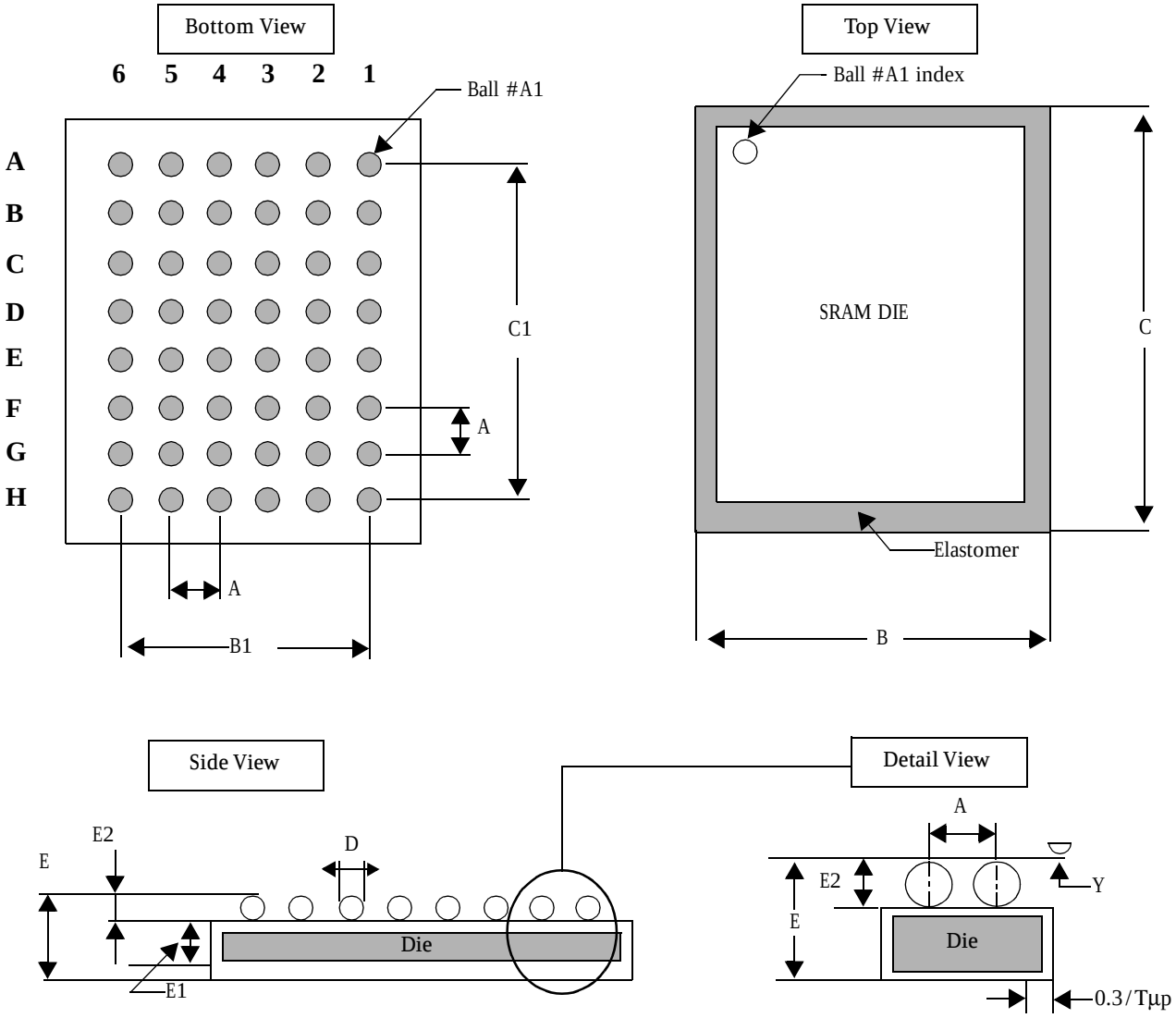
Package diagrams and dimensions



	44-pin TSOP II	
	Min (mm)	Max (mm)
A		1.2
A_1	0.05	
A_2	0.95	1.05
b	0.25	0.45
c	0.15 (typical)	
d	20.85	21.05
e	10.06	10.26
H_e	11.56	11.96
E	0.80 (typical)	
l	0.40	0.60

SRAM

48-ball FBGA



	Minimum	Typical	Maximum
A	–	0.75	–
B	6.90	7.00	7.10
B1	–	3.75	–
C	10.90	11.00	11.10
C1	–	5.25	–
D	0.30	0.35	0.40
E	–	–	1.20
E1	–	0.68	–
E2	0.22	0.25	0.27
Y	–	–	0.08

Notes

1. Bump counts: 48 (8 row x 6 column).
2. Pitch: (x,y) = 0.75 mm x 0.75 mm (typ).
3. Units: millimeters.
4. All tolerances are +/- 0.050 unless otherwise specified.
5. Typ: typical.
6. Y is coplanarity: 0.08 (max).

Ordering codes

Speed (ns)	Ordering Code	Package Type	Operating Range
55/70/100	AS6UA25617-BI	48-ball fine pitch BGA	Industrial
	AS6UZ25617-TI	44-pin TSOP II	

Part numbering system

AS6UA	25617	Package	I
SRAM Intelliwatt™ prefix	Device number	B=CSP BGA T=TSOP II	Temperature range, I=Industrial: -40°C to 85°C