## Features

- **Edge-Controlled Power Down Pin**
- **Zero Power Equivalent of ATF16V8B**
- **Edge-Sensing Zero Standby Power (10 μA Typical)**
- **Industry Standard Architecture**
  Emulates Many 20-Pin PALs®
  Low Cost Easy-to-Use Software Tools
- **High Speed Electrically Erasable Programmable Logic Devices**
  10 ns Maximum Pin-to-Pin Delay
- **CMOS and TTL Compatible Inputs and Outputs**
  Latch Feature Holds Outputs to Previous Logic States
- **Advanced Flash Technology**
  Reprogrammable
  100% Tested
- **High Reliability CMOS Process**
  20 Year Data Retention
  100 Erase/Write Cycles
  2,000 V ESD Protection
  200 mA Latchup Immunity
- **Commercial, and Industrial Temperature Ranges**
- **Dual-in-Line and Surface Mount Packages in Standard Pinouts**

High Performance Flash PLD

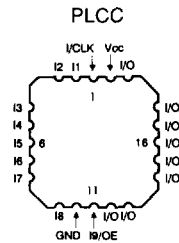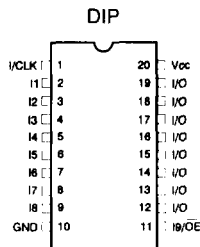## Advance Information

Block Diagram
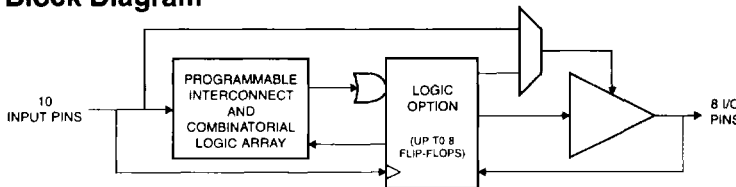
Description

The ATF16V8CZ is a high performance CMOS (Electrically Erasable) Programmable Logic Devices (PLDs) which utilize Atmel's proven electrically erasable Flash memory technology. Speeds down to 10 ns and power dissipation as low as 10 μA are offered. All speed ranges are specified over the full 5 V ± 10% range for industrial temperature ranges, and 5 V ± 5% for commercial ranges.

The ATF16V8CZ provides the zero power CMOS PLD solution, with "zero" standby power (10 μA typical). The ATF16V8CZ powers down automatically through Atmel's patented In-

(continued)

Pin Configurations

Pin Name	Function
CLK	Clock
I	Logic Inputs
I/O	Bidirectional Buffers
OE	Output Enable
VCC	+5 V Supply

DIP

I/CLK 1 — 20 Vcc
I1 2 — 19 I/O
I2 3 — 18 I/O
I3 4 — 17 I/O
I4 5 — 16 I/O
I5 6 — 15 I/O
I6 7 — 14 I/O
I7 8 — 13 I/O
I8 9 — 12 I/O
GND 10 — 11 I9/OE

PLCC

I/CLK Vcc
I2 I1 ↓ ↓ I/O
I3 — I/O
I4 — I/O
I5 6 16 I/O
I6 — I/O
I7 — I/O
I8 ↑ ↑ I/OI/O
GND I9/OE

0453A

Description (Continued)

put Transition Detection (ITD) circuitry to the "zero" standby power mode when the device remains idle. Pin "keeper" circuits on input and output pins reduce static power consumed by pull-up resistors.

The ATF16V8CZ incorporates a superset of the generic architectures, which allows direct replacement of the 16R8 family and most 20-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allow highly complex logic functions to be realized.

D.C. and A.C. Operating Conditions

	Commercial	Industrial	Military
Operating Temperature (Case)	0°C - 70°C	-40°C - 85°C	-55°C - 125°C
V$_{CC}$ Power Supply	5 V ± 5%	5 V ± 10%	5 V ± 10%

Functional Description

The ATF16V8CZ macrocell can be configured in one of three different modes. Each mode makes the ATF16V8CZ look like a different device. The ATF16V8CZ can be a registered output, combinatorial I/O, combinatorial output, or dedicated input. Most PLD compilers can choose the right mode automatically. The user can also force the selection by supplying the compiler with a mode selection. The determining factors would be the usage of registered versus combinatorial outputs and dedicated outputs versus outputs with output enable control.

The ATF16V8CZ powers down automatically to a "zero" standby power mode (10 µA typical) through the ITD circuitry when all inputs are idle. This feature allows the user flexibility to manage total system power and enhance reliability all without sacrificing speed. Static power loss due to pull-up resistors is reduced through input and output pin "keeper" circuits which hold pins to their previous logic levels when idle.

The universal architecture of the ATF16V8CZ can be programmed to emulate many 20-pin PAL devices. The user can download the subset device JEDEC programming file to the PLD programmer, and the ATF16V8CZ can be configured to act like the chosen device.

Unused product terms are automatically disabled by the compiler to decrease power consumption. A Security Fuse, when programmed, protects the contents of the ATF16V8CZ. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the Security Fuse.

Compiler Mode Selection

	Registered	Complex	Simple	Auto Select
ABEL, Atmel-ABEL	P16V8R	P16V8C	P16V8AS	P16V8
CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8
LOG/iC	GAL16V8_R	GAL16V8_C7	GAL16V8_C8	GAL16V8
OrCAD-PLD	"Registered"	"Complex"	"Simple"	GAL16V8A
PLDesigner	P16V8R	P16V8C	P16V8C	P16V8A
Tango-PLD	G16V8R	G16V8C	G16V8AS	G16V8

ATF16V8CZ