*PRELIMINARY*

# LH530800A-Y

**CMOS 1M (128K × 8)**
**Mask-Programmable ROM**

## FEATURES

- 131,072 × 8 bit organization
- Access time:
  500 ns (MAX.) at 2.6 V ≤ $V_{CC}$ < 4.5 V
  150 ns (MAX.) at 4.5 V ≤ $V_{CC}$ < 5.5 V
- Low-power consumption:
  Operating: 193 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully-static operation
- Three-state outputs
- Mask-programmable control pin:
  Pin 24 = OE/$\overline{OE}$
- Wide range power supply:
  2.6 V to 5.5 V
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  44-pin, 10 × 10 mm$^2$ QFP

## DESCRIPTION

The LH530800A-Y is a 1M-bit mask-programmable ROM organized as 131,072 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

## PIN CONNECTIONS

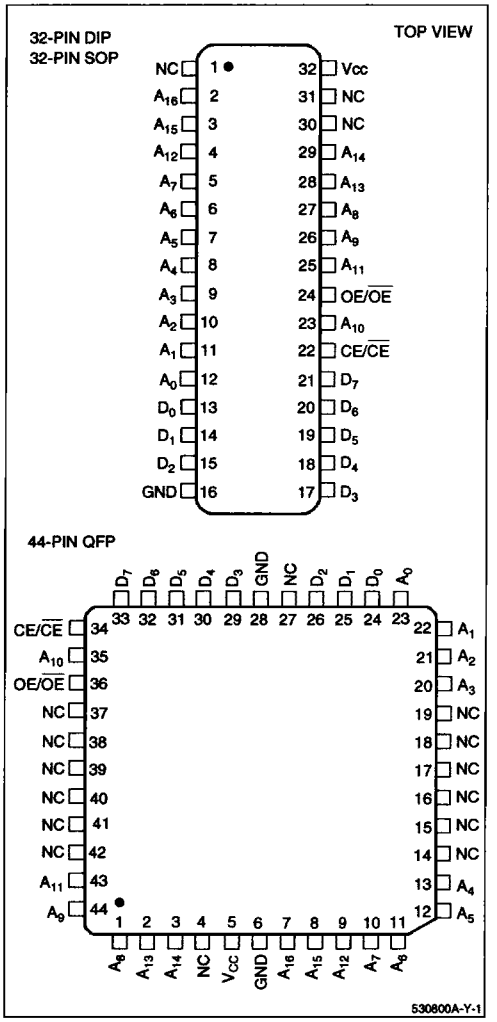



**Figure 1. Pin Connections for DIP, SOP, and QFP Packages**

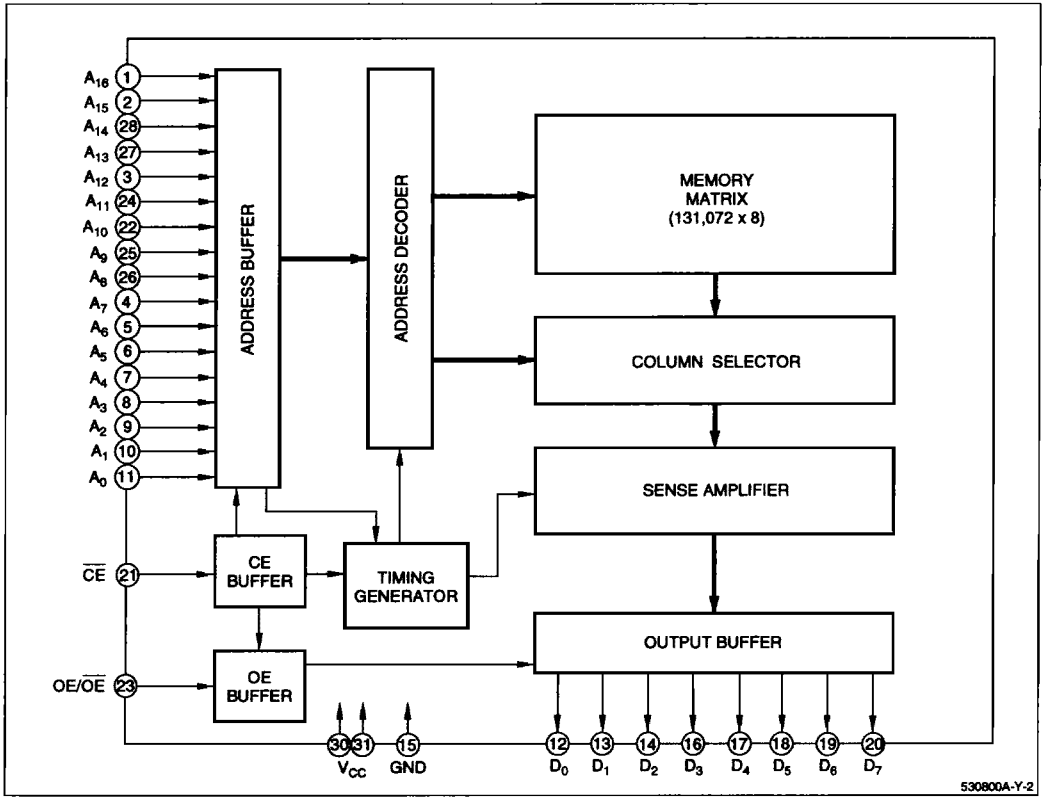



**Figure 2. LH530800A-Y Block Diagram**

## PIN DESCRIPTION

| SIGNAL | PIN NAME | NOTE |
|---|---|---|
| $A_0$ - $A_{16}$ | Address input | |
| $D_0$ - $D_7$ | Data Output | |
| CE | Chip enable input | |
| OE/$\overline{OE}$ | Output enable input | 1 |

| SIGNAL | PIN NAME | NOTE |
|---|---|---|
| $V_{CC}$ | Power supply | |
| GND | Ground | |
| NC | Non connection | |

**NOTE:**
1. Active levels of OE/$\overline{OE}$ are mask-programmable.

## TRUTH TABLE

| CE | OE/$\overline{OE}$ | $D_0$ - $D_7$ | SUPPLY CURRENT | NOTE |
|---|---|---|---|---|
| H | X | High-Z | Standby ($I_{SB}$) | 1 |
| L | L/H | High-Z | Operating ($I_{CC}$) | |
| L | H/L | $D_{OUT}$ | Operating ($I_{CC}$) | |

**NOTE:**
1. X = H or L

## ABSOLUTE MAXIMUM RATINGS

| PARAMETER | SYMBOL | RATING | UNIT |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | -0.3 to +7.0 | V |
| Input voltage | $V_{IN}$ | -0.3 to $V_{CC}$ +0.3 | V |
| Output voltage | $V_{OUT}$ | -0.3 to $V_{CC}$ +0.3 | V |
| Operating temperature | Topr | 0 to +70 | °C |
| Storage temperature | Tstg | -65 to +150 | °C |

## RECOMMENDED OPERATING CONDITIONS ($T_A$ = 0 to +70°C)

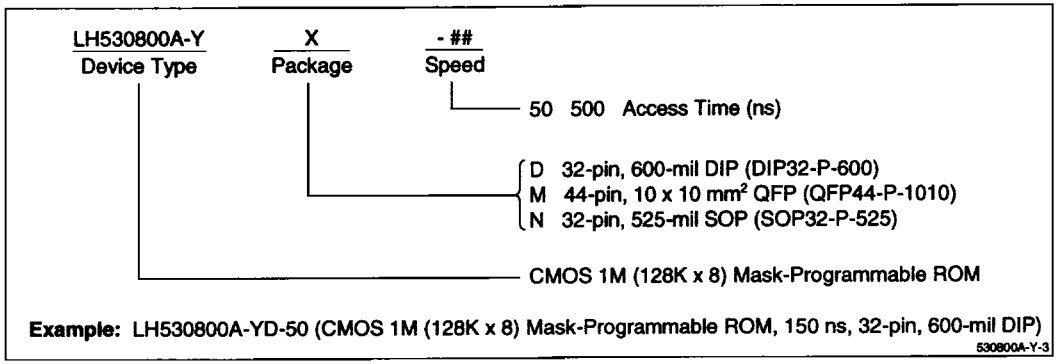
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 2.6 | | 5.5 | V |

## DC CHARACTERISTICS ($V_{CC}$ = 2.6 V to 5.5 V, $T_A$ = 0 to +70°C)

| PARAMETER | SYMBOL | CONDITIONS | MIN. | TYP. | MAX. | UNIT | NOTE |
|---|---|---|---|---|---|---|---|
| Input 'Low' voltage | $V_{IL}$ | | -0.3 | | 0.4 | V | |
| Input 'High' voltage | $V_{IH}$ | | 0.8 × $V_{CC}$ | | $V_{CC}$ + 0.3 | V | |
| Output 'Low' voltage | $V_{OL}$ | $I_{OL}$ = 400 µA | | | 0.4 | V | |
| Output 'High' voltage | $V_{OH}$ | $I_{OH}$ = -100 µA | 0.8 × $V_{CC}$ | | | V | |
| Input leakage current | $\lvert I_{LI} \rvert$ | $V_{IN}$ = 0 V to $V_{CC}$ | | | 10 | µA | |
| Output leakage current | $\lvert I_{LO} \rvert$ | $V_{OUT}$ = 0 V to $V_{CC}$ | | | 10 | µA | 1 |
| Operating current | $I_{CC1}$ | $t_{RC}$ = 150 ns | | | 35 | mA | 2 |
| | $I_{CC2}$ | $t_{RC}$ = 500 ns | | | 18 | mA | 3 |
| | $I_{CC3}$ | $t_{RC}$ = 500 ns | | | 12 | mA | 4 |
| Standby current | $I_{SB1}$ | $\overline{CE}$ = $V_{IH}$ | | | 2 | mA | |
| | $I_{SB2}$ | $\overline{CE}$ = $V_{CC}$ - 0.2 V | | | 100 | µA | |
| Input capacitance | $C_{IN}$ | f = 1 MHz, $t_A$ = 25°C | | | 10 | pF | |
| Output capacitance | $C_{OUT}$ | | | | 10 | pF | |

**NOTES:**
1. $\overline{CE}/\overline{OE}$ = $V_{IH}$, OE = $V_{IL}$, outputs open
2. 4.5 V ≤ $V_{CC}$ ≤ 5.5 V
3. 3.4 V < $V_{CC}$ < 4.5 V
4. 2.6 V ≤ $V_{CC}$ ≤ 3.4 V

## ORDERING INFORMATION




**Example:** LH530800A-YD-50 (CMOS 1M (128K x 8) Mask-Programmable ROM, 150 ns, 32-pin, 600-mil DIP)

530800A-Y-3