

RJK0854DPB

Silicon N Channel Power MOS FET Power Switching

REJ03G1883-0100

Rev.1.00

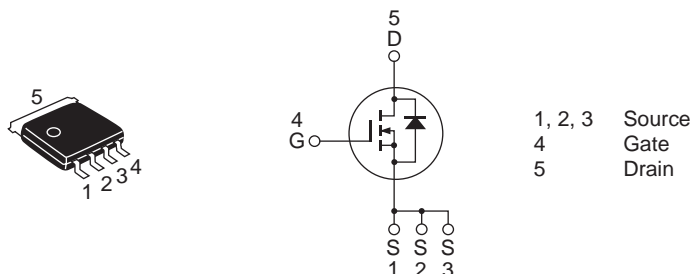
Nov 30, 2009

Features

- High speed switching
- Low drive current
- Low on-resistance
- $R_{DS(on)} = 10 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)
- Pb-free
- Halogen-free
- High density mounting

Outline

RENESAS Package code: PTZZ0005DA-A
(Package name: LFPAK)



Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	80	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	25	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	100	A
Body-drain diode reverse drain current	I_{DR}	25	A
Avalanche current	I_{AP} ^{Note 2}	25	A
Avalanche energy	E_{AR} ^{Note 2}	8.3	mJ
Channel dissipation	P_{ch} ^{Note3}	55	W
Channel to Case Thermal Resistance	θ_{ch-C}	2.27	$^\circ\text{C/W}$
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$

2. Value at $L=10\mu\text{H}$, $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$

3. $T_c = 25^\circ\text{C}$

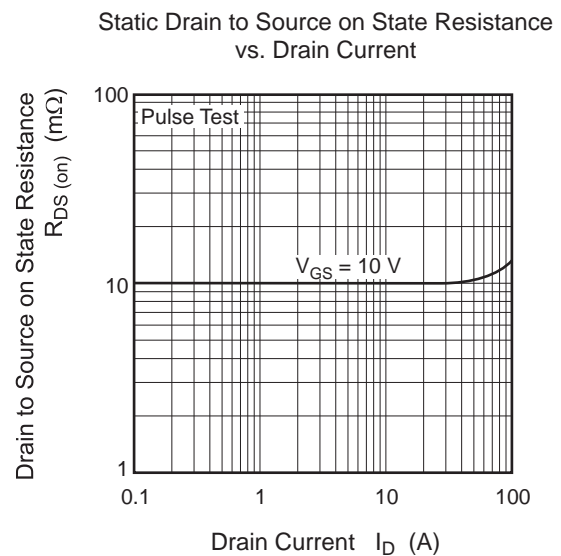
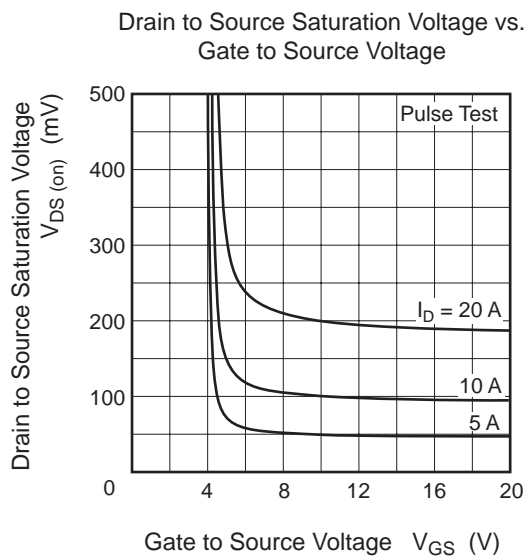
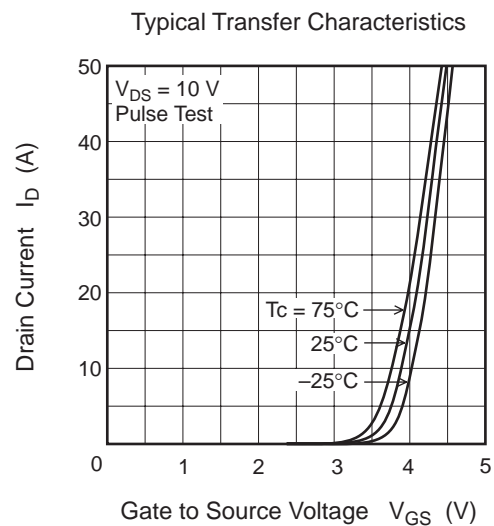
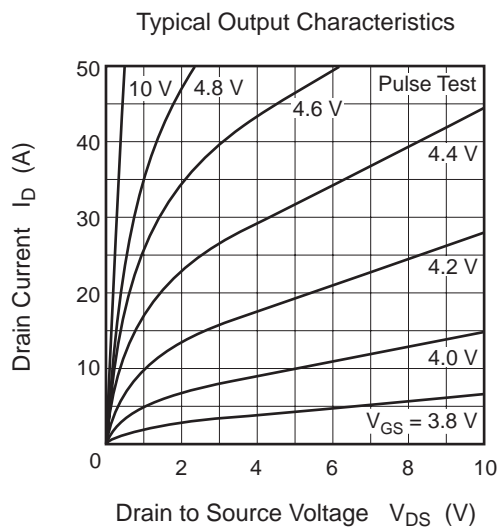
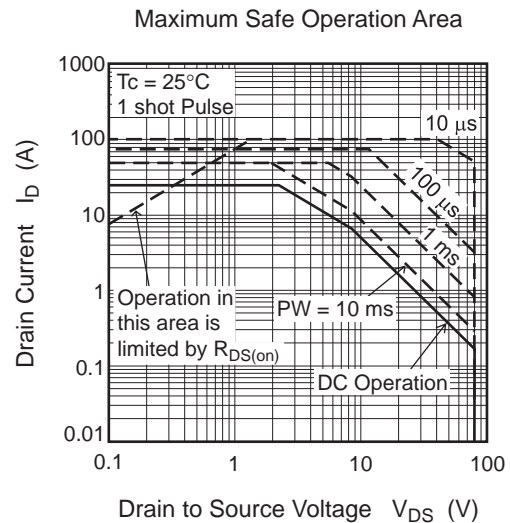
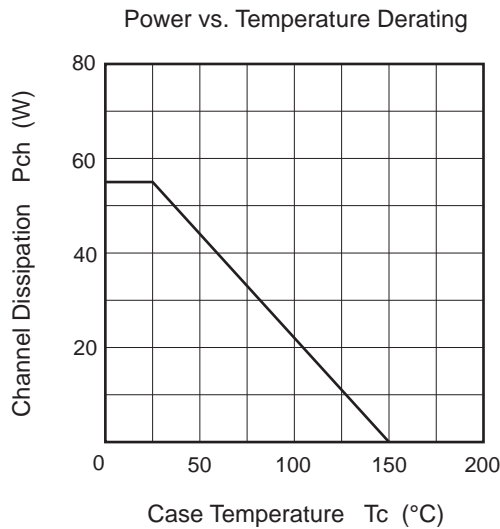
Electrical Characteristics

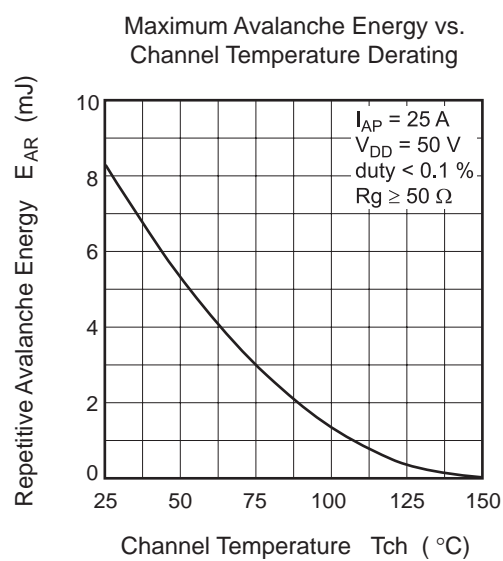
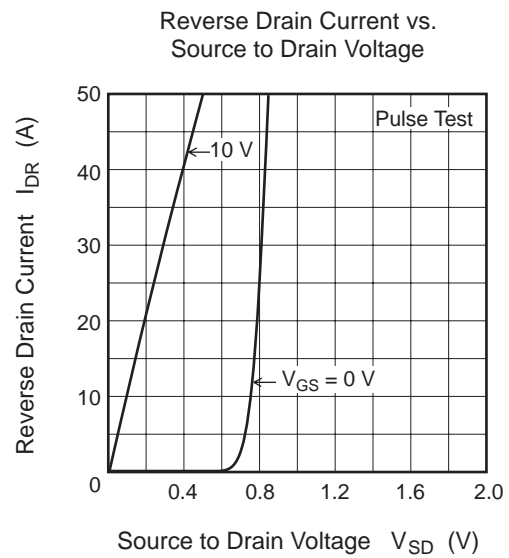
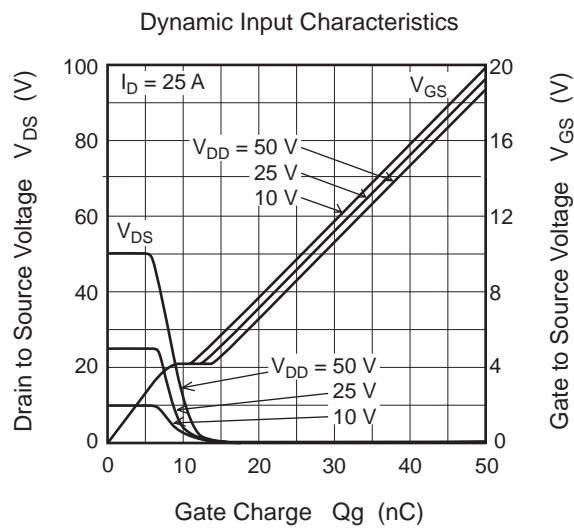
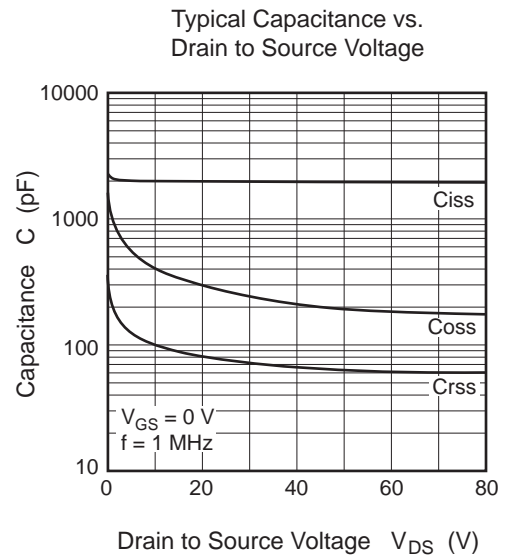
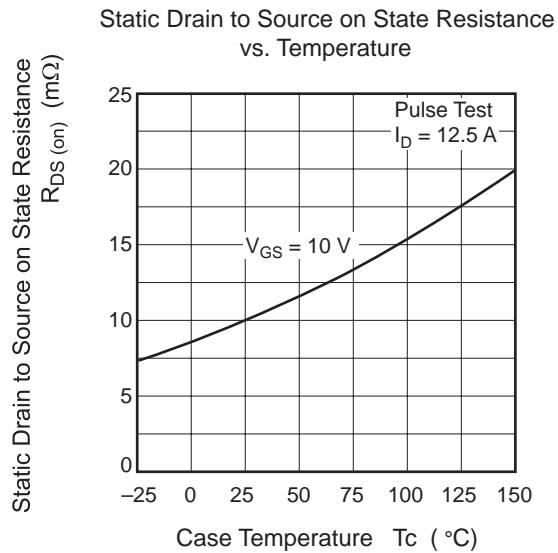
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	80	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0 \text{ V}$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0 \text{ V}$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 80 \text{ V}$, $V_{GS} = 0 \text{ V}$
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	10	13	$\text{m}\Omega$	$I_D = 12.5 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	—	36	—	S	$I_D = 12.5 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	2000	—	pF	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	405	—	pF	
Reverse transfer capacitance	C_{rss}	—	100	—	pF	
Gate Resistance	R_g	—	0.5	—	Ω	
Total gate charge	Q_g	—	27	—	nC	$V_{DD} = 25 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 25 \text{ A}$
Gate to source charge	Q_{gs}	—	9.0	—	nC	
Gate to drain charge	Q_{gd}	—	4.5	—	nC	
Turn-on delay time	$t_{d(on)}$	—	12	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 12.5 \text{ A}$, $V_{DD} \cong 30 \text{ V}$, $R_L = 2.4 \Omega$, $R_g = 4.7 \Omega$
Rise time	t_r	—	5.5	—	ns	
Turn-off delay time	$t_{d(off)}$	—	32	—	ns	
Fall time	t_f	—	6.9	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.8	1.1	V	$I_F = 25 \text{ A}$, $V_{GS} = 0 \text{ V}$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	42	—	ns	$I_F = 25 \text{ A}$, $V_{GS} = 0 \text{ V}$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

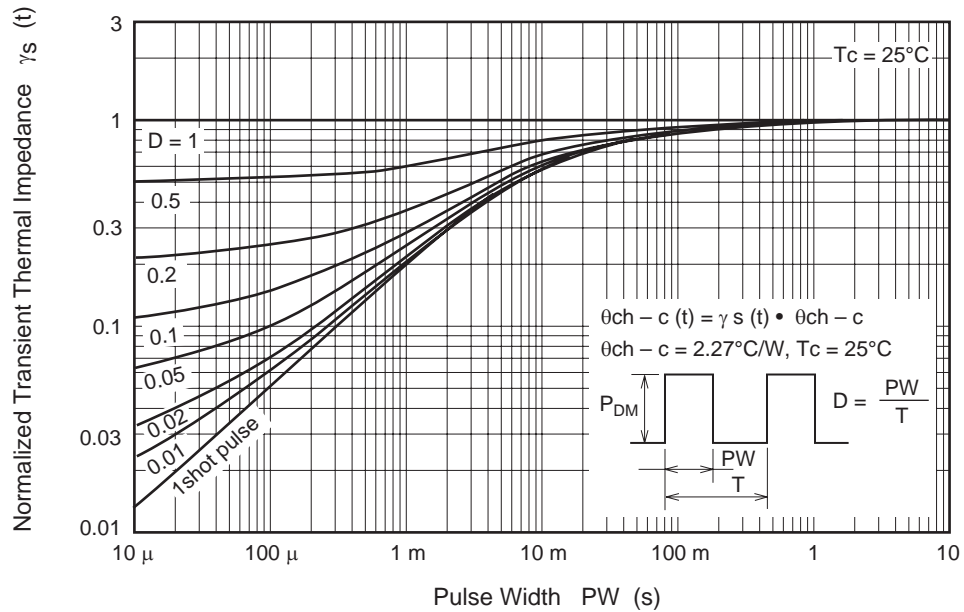
Notes: 4. Pulse test

Main Characteristics

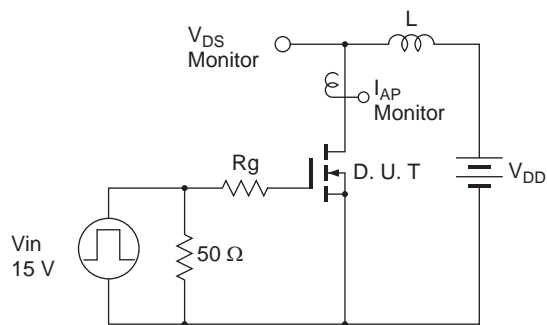




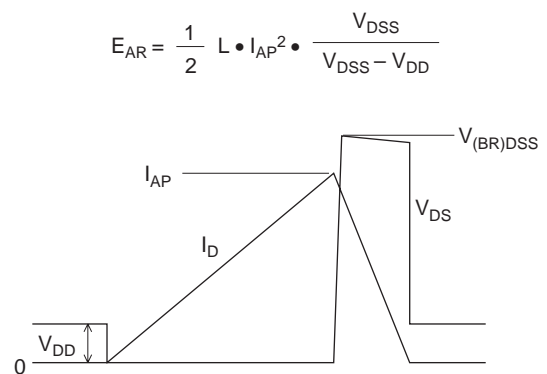
Normalized Transient Thermal Impedance vs. Pulse Width



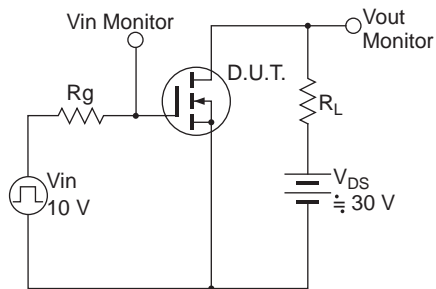
Avalanche Test Circuit



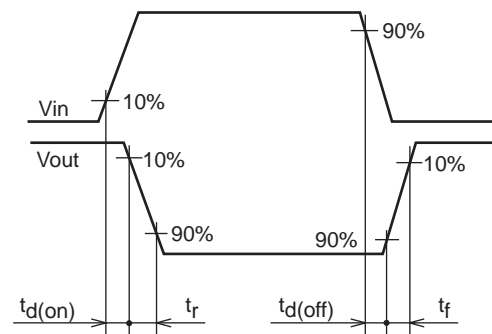
Avalanche Waveform



Switching Time Test Circuit



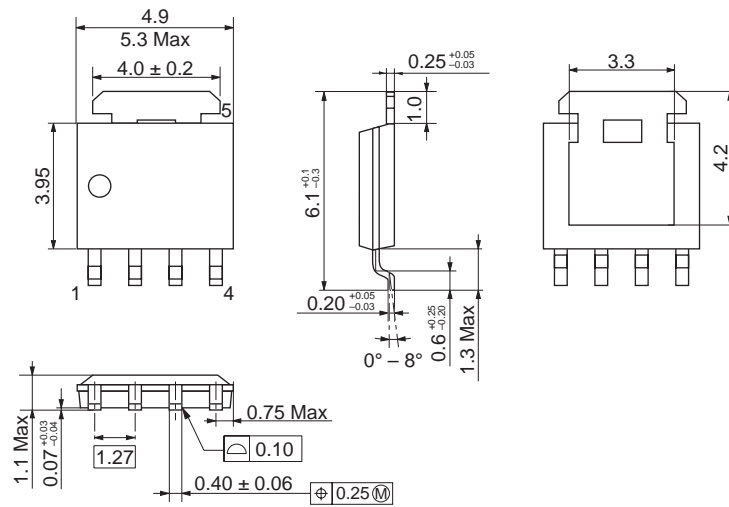
Switching Time Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
LPAK	SC-100	PTZZ0005DA-A	LPAKV	0.080g

Unit: mm



(Ni/Pd/Au plating)

Ordering Information

Part No.	Quantity	Shipping Container
RJK0854DPB-00-J5	2500 pcs	Taping

Notes:

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