

# MC74LCX16245

## Low-Voltage CMOS 16-Bit Transceiver

### With 5 V-Tolerant Inputs and Outputs (3-State, Non-Inverting)

The MC74LCX16245 is a high performance, non-inverting 16-bit transceiver operating from a 2.3 to 3.6 V supply. The device is byte controlled. Each byte has separate Output Enable inputs which can be tied together for full 16-bit operation. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A  $V_I$  specification of 5.5 V allows MC74LCX16245 inputs to be safely driven from 5.0 V devices. The MC74LCX16245 is suitable for memory address driving and all TTL level bus oriented transceiver applications.

The 4.5 ns maximum propagation delays support high performance applications. Current drive capability is 24 mA at both A and B ports. The Transmit/Receive ( $T/\bar{R}_n$ ) inputs determine the direction of data flow through the bidirectional transceiver. Transmit (active-HIGH) enables data from A ports to B ports; Receive (active-LOW) enables data from B to A ports. The Output Enable inputs ( $\overline{OE}_n$ ), when HIGH, disable both A and B ports by placing them in a HIGH Z condition.

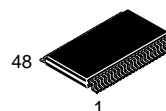
#### Features

- Designed for 2.3 to 3.6 V  $V_{CC}$  Operation
- 4.5 ns Maximum  $t_{pd}$
- 5.0 V Tolerant – Interface Capability With 5.0 V TTL Logic
- Supports Live Insertion and Withdrawal
- $I_{OFF}$  Specification Guarantees High Impedance When  $V_{CC} = 0$  V
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current in All Three Logic States (20  $\mu$ A)  
Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance: Human Body Model >2000 V;  
Machine Model >200 V
- These are Pb-Free Devices\*



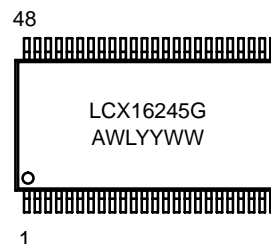
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TSSOP-48  
DT SUFFIX  
CASE 1201

#### MARKING DIAGRAM



A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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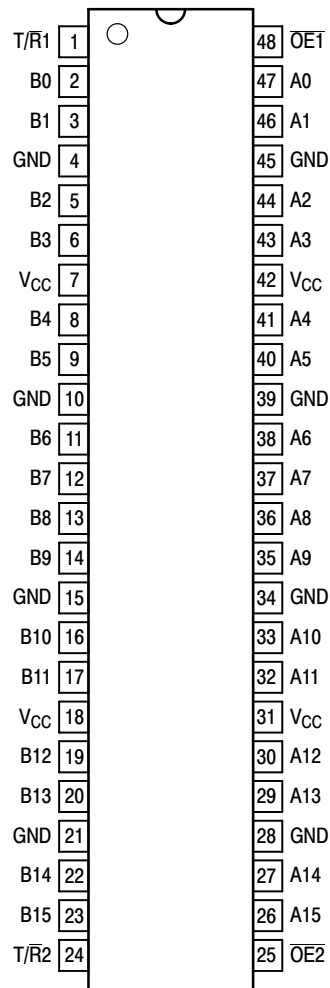


Figure 1. Pinout: 48-Lead (Top View)

Table 1. PIN NAMES

Pins	Function
$\overline{OE}n$	Output Enable Inputs
$T/R\overline{n}$	Transmit/Receive Inputs
A0 – A15	Side A Inputs or 3-State Outputs
B0 – B15	Side B Inputs or 3-State Outputs

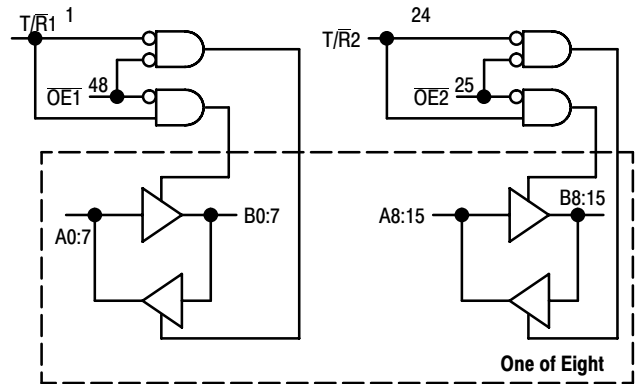


Figure 2. Logic Diagram

## TRUTH TABLE

Inputs		Outputs	Inputs		Outputs
OE1	T/R1		OE2	T/R2	
L	L	Bus B0:7 Data to Bus A0:7	L	L	Bus B8:15 Data to Bus A8:15
L	H	Bus A0:7 Data to Bus B0:7	L	H	Bus A8:15 Data to Bus B8:15
H	X	High Z State on A0:7, B0:7	H	X	High Z State on A8:15, B8:15

H = High Voltage Level

L = Low Voltage Level

Z = High Impedance State

X = High or Low Voltage Level and Transitions Are Acceptable; for  $I_{CC}$  reasons, DO NOT FLOAT Inputs

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## ORDERING INFORMATION

Device	Package	Shipping†
MC74LCX16245DT	TSSOP-48*	39 Units / Rail
MC74LCX16245DTG	TSSOP-48*	39 Units / Rail
MC74LCX16245DTR2	TSSOP-48*	2500 / Tape & Reel
M74LCX16245DTR2G	TSSOP-48*	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

## MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Unit
$V_{CC}$	DC Supply Voltage	-0.5 to +7.0		V
$V_I$	DC Input Voltage	$-0.5 \leq V_I \leq +7.0$		V
$V_O$	DC Output Voltage	$-0.5 \leq V_O \leq +7.0$	Output in 3-State	V
		$-0.5 \leq V_O \leq V_{CC} + 0.5$	Output in HIGH or LOW State. (Note 1)	V
$I_{IK}$	DC Input Diode Current	-50	$V_I < GND$	mA
$I_{OK}$	DC Output Diode Current	-50	$V_O < GND$	mA
		+50	$V_O > V_{CC}$	mA
$I_O$	DC Output Source/Sink Current	$\pm 50$		mA
$I_{CC}$	DC Supply Current Per Supply Pin	$\pm 100$		mA
$I_{GND}$	DC Ground Current Per Ground Pin	$\pm 100$		mA
$T_{STG}$	Storage Temperature Range	-65 to +150		°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1.  $I_O$  absolute maximum rating must be observed.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit	
$V_{CC}$	Supply Voltage	Operating	2.0	2.5, 3.3	3.6	V
		Data Retention Only	1.5	2.5, 3.3	3.6	
$V_I$	Input Voltage	0		5.5	V	
$V_O$	Output Voltage (HIGH or LOW State) (3-State)	0		$V_{CC}$	V	
		0		5.5		
$I_{OH}$	HIGH Level Output Current $V_{CC} = 3.0\text{ V} - 3.6\text{ V}$ $V_{CC} = 2.7\text{ V} - 3.0\text{ V}$ $V_{CC} = 2.3\text{ V} - 2.7\text{ V}$			-24 -12 -8	mA	
$I_{OL}$	LOW Level Output Current $V_{CC} = 3.0\text{ V} - 3.6\text{ V}$ $V_{CC} = 2.7\text{ V} - 3.0\text{ V}$ $V_{CC} = 2.3\text{ V} - 2.7\text{ V}$			+24 +12 +8	mA	
$T_A$	Operating Free-Air Temperature	-40		+85	°C	
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate, $V_{IN}$ from 0.8 V to 2.0 V, $V_{CC} = 3.0\text{ V}$	0		10	ns/V	

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## DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Unit
			Min	Max	
$V_{IH}$	HIGH Level Input Voltage (Note 2)	$2.3\text{ V} \leq V_{CC} \leq 2.7\text{ V}$	1.7		V
		$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$	2.0		
$V_{IL}$	LOW Level Input Voltage (Note 2)	$2.3\text{ V} \leq V_{CC} \leq 2.7\text{ V}$		0.7	V
		$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$		0.8	
$V_{OH}$	HIGH Level Output Voltage	$2.3\text{ V} \leq V_{CC} \leq 3.6\text{ V}; I_{OL} = 100\ \mu\text{A}$	$V_{CC} - 0.2$		V
		$V_{CC} = 2.3\text{ V}; I_{OH} = -8\text{ mA}$	1.8		
		$V_{CC} = 2.7\text{ V}; I_{OH} = -12\text{ mA}$	2.2		
		$V_{CC} = 3.0\text{ V}; I_{OH} = -18\text{ mA}$	2.4		
		$V_{CC} = 3.0\text{ V}; I_{OH} = -24\text{ mA}$	2.2		
$V_{OL}$	LOW Level Output Voltage	$2.3\text{ V} \leq V_{CC} \leq 3.6\text{ V}; I_{OL} = 100\ \mu\text{A}$		0.2	V
		$V_{CC} = 2.3\text{ V}; I_{OL} = 8\text{ mA}$		0.6	
		$V_{CC} = 2.7\text{ V}; I_{OL} = 12\text{ mA}$		0.4	
		$V_{CC} = 3.0\text{ V}; I_{OL} = 16\text{ mA}$		0.4	
		$V_{CC} = 3.0\text{ V}; I_{OL} = 24\text{ mA}$		0.55	
$I_I$	Input Leakage Current	$2.3\text{ V} \leq V_{CC} \leq 3.6\text{ V}; 0\text{ V} \leq V_I \leq 5.5\text{ V}$		$\pm 5.0$	$\mu\text{A}$
$I_{OZ}$	3-State Output Current	$2.3 \leq V_{CC} \leq 3.6\text{ V}; 0\text{V} \leq V_O \leq 5.5\text{ V}; V_I = V_{IH}\text{ or } V_{IL}$		$\pm 5.0$	$\mu\text{A}$
$I_{OFF}$	Power-Off Leakage Current	$V_{CC} = 0\text{ V}; V_I\text{ or } V_O = 5.5\text{ V}$		10	$\mu\text{A}$
$I_{CC}$	Quiescent Supply Current	$2.3 \leq V_{CC} \leq 3.6\text{ V}; V_I = \text{GND or } V_{CC}$		20	$\mu\text{A}$
		$2.3 \leq V_{CC} \leq 3.6\text{ V}; 3.6 \leq V_I\text{ or } V_O \leq 5.5\text{ V}$		$\pm 20$	$\mu\text{A}$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$2.3 \leq V_{CC} \leq 3.6\text{ V}; V_{IH} = V_{CC} - 0.6\text{ V}$		500	$\mu\text{A}$

2. These values of  $V_I$  are used to test DC electrical characteristics only.

## AC CHARACTERISTICS $t_R = t_F = 2.5\text{ ns}; R_L = 500\ \Omega$

Symbol	Parameter	Waveform	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$						Unit
			$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ $C_L = 50\text{ pF}$		$V_{CC} = 2.7\text{ V}$ $C_L = 50\text{ pF}$		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ $C_L = 30\text{ pF}$		
			Min	Max	Min	Max	Min	Max	
$t_{PLH}$ $t_{PHL}$	Propagation Delay Input to Output	1	1.5	4.5	1.5	5.2	1.5	5.4	ns
			1.5	4.5	1.5	5.2	1.5	5.4	
$t_{PZH}$ $t_{PZL}$	Output Enable Time to High and Low Level	2	1.5	6.5	1.5	7.2	1.5	8.5	ns
			1.5	6.5	1.5	7.2	1.5	8.5	
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time From High and Low Level	2	1.5	6.4	1.5	6.9	1.5	7.7	ns
			1.5	6.4	1.5	6.9	1.5	7.7	
$t_{OSHL}$ $t_{OSLH}$	Output-to-Output Skew (Note 3)			1.0					ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW ( $t_{OSHL}$ ) or LOW-to-HIGH ( $t_{OSLH}$ ); parameter guaranteed by design.

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## DYNAMIC SWITCHING CHARACTERISTICS

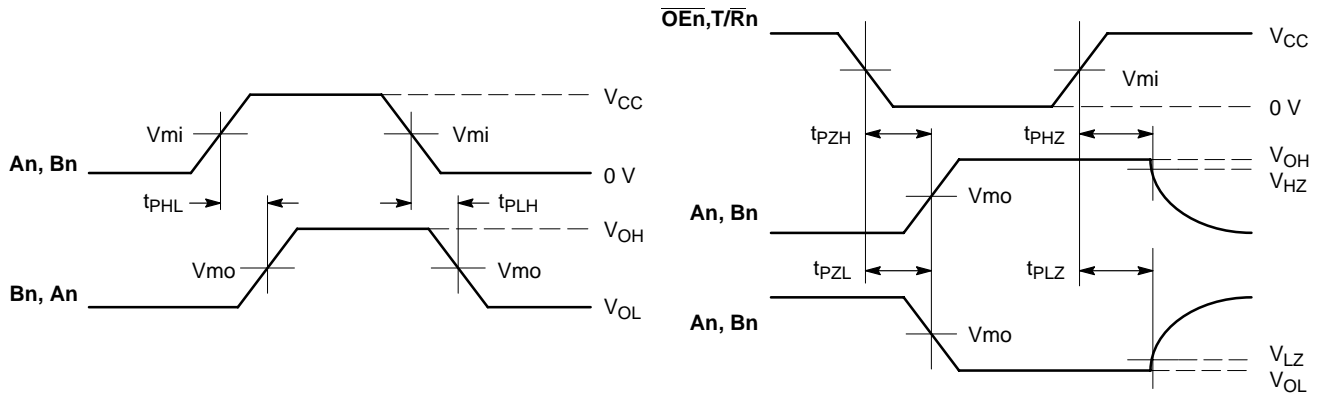
Symbol	Characteristic	Condition	T <sub>A</sub> = +25°C			Unit
			Min	Typ	Max	
V <sub>OLP</sub>	Dynamic LOW Peak Voltage (Note 4)	V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V		0.8		V
		V <sub>CC</sub> = 2.5 V, C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5 V, V <sub>IL</sub> = 0 V		0.6		V
V <sub>OLV</sub>	Dynamic LOW Valley Voltage (Note 4)	V <sub>CC</sub> = 3.3 V, C <sub>L</sub> = 50 pF, V <sub>IH</sub> = 3.3 V, V <sub>IL</sub> = 0 V		-0.8		V
		V <sub>CC</sub> = 2.5 V, C <sub>L</sub> = 30 pF, V <sub>IH</sub> = 2.5 V, V <sub>IL</sub> = 0 V		-0.6		V

4. Number of outputs defined as "n". Measured with "n-1" outputs switching from HIGH-to-LOW or LOW-to-HIGH. The remaining output is measured in the LOW state.

## CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	7	pF
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	8	pF
C <sub>PD</sub>	Power Dissipation Capacitance	10 MHz, V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = 0 V or V <sub>CC</sub>	20	pF

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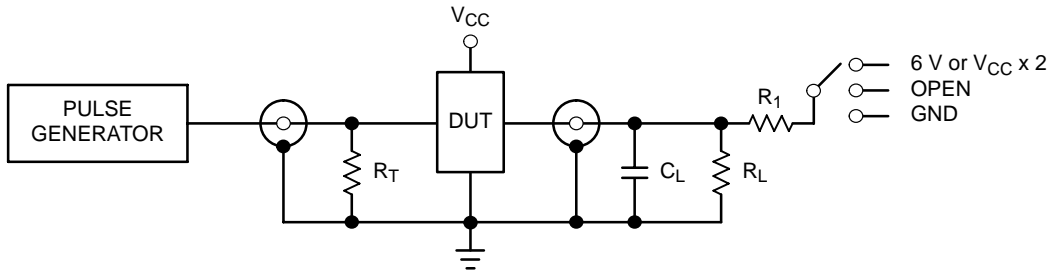
**WAVEFORM 1 – PROPAGATION DELAYS**  
 $t_R = t_F = 2.5$  ns, 10% to 90%;  $f = 1$  MHz;  $t_W = 500$  ns

**WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES**  
 $t_R = t_F = 2.5$  ns, 10% to 90%;  $f = 1$  MHz;  $t_W = 500$  ns

**Figure 3. AC Waveforms**

**Table 2. AC WAVEFORMS**

Symbol	$V_{CC}$		
	$3.3\text{ V} \pm 0.3\text{ V}$	$2.7\text{ V}$	$2.5\text{ V} \pm 0.2\text{ V}$
$V_{mi}$	1.5 V	1.5 V	$V_{CC} / 2$
$V_{mo}$	1.5 V	1.5 V	$V_{CC} / 2$
$V_{HZ}$	$V_{OL} + 0.3\text{ V}$	$V_{OL} + 0.3\text{ V}$	$V_{OL} + 0.15\text{ V}$
$V_{LZ}$	$V_{OH} - 0.3\text{ V}$	$V_{OH} - 0.3\text{ V}$	$V_{OH} - 0.15\text{ V}$



**Figure 4. Test Circuit**

**Table 3. TEST CIRCUIT**

TEST	SWITCH
$t_{PLH}, t_{PHL}$	Open
$t_{PZL}, t_{PLZ}$	6 V at $V_{CC} = 3.3 \pm 0.3\text{ V}$ 6 V at $V_{CC} = 2.5 \pm 0.2\text{ V}$
Open Collector/Drain $t_{PLH}$ and $t_{PHL}$	6 V
$t_{PZH}, t_{PHZ}$	GND

$C_L = 50$  pF at  $V_{CC} = 3.3 \pm 0.3\text{ V}$  or equivalent (includes jig and probe capacitance)

$C_L = 30$  pF at  $V_{CC} = 2.5 \pm 0.2\text{ V}$  or equivalent (includes jig and probe capacitance)

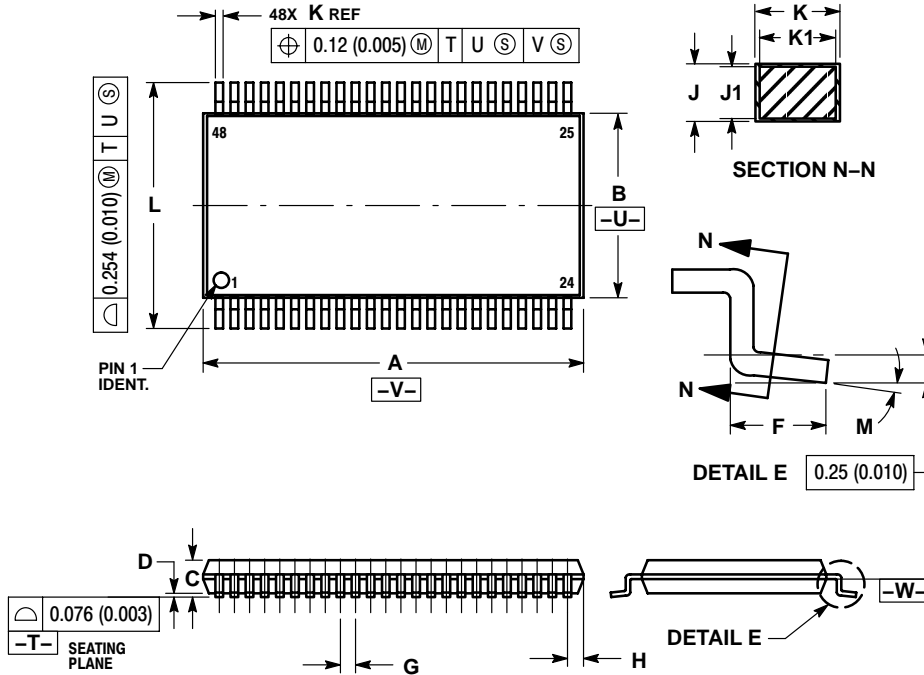
$R_L = R_1 = 500\ \Omega$  or equivalent

$R_T = Z_{OUT}$  of pulse generator (typically 50  $\Omega$ )

# MC74LCX16245

## PACKAGE DIMENSIONS

TSSOP-48  
DT SUFFIX  
CASE 1201-01  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.37	---	0.015	---
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0 °	8 °	0 °	8 °

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