

Ultralow Offset Voltage Op Amp

AD 0P-07

FEATURES

Ten Times More Gain than Other OP-07 Devices

(3.0M min)

Ultralow Offset Voltage: 10μV Ultralow Offset Voltage Drift: 0.2μV/°C

Ultrastable vs. Time: 0.2µV/°C
Ultralow Noise: 0.35µV p-p
No External Components Required

Monolithic Construction

High Common-Mode Input Range: ±14.0V Wide Power Supply Voltage Range: ±3V to ±18V

Fits 725, 108A/308A Sockets

Military Parts and Plus Parts Available 8-Pin Plastic Mini-DIP, Cerdip, TO-99 Hermetic Metal Can, or SOIC

Available in Wafer-Trimmed Chip Form Surface Mount (SOIC) Available in Tape and Reel

PRODUCT DESCRIPTION

The AD OP-07 is an improved version of the industry-standard OP-07 precision operational amplifier. A guaranteed minimum open-loop voltage gain of 3,000,000 (AD OP-07A) represents an order of magnitude improvement over older designs; this affords increased accuracy in high closed-loop gain applications. Typical input offset voltages as low as $10\mu V$, typical bias currents of 0.7nA, internal compensation and device protection eliminate the need for external components and adjustments. An input offset voltage temperature coefficient of $0.2\mu V/^{\circ}C$ (typ) and long-term stability of $0.2\mu V$ month (typ) eliminate recalibration or loss of initial accuracy.

A true differential operational amplifier, the AD OP-07 has a high common-mode input voltage range ($\pm 13V$, min) common-mode rejection ratio (typically up to 126dB) and high differential input impedance ($50M\Omega$ typ); these features combine to assure high accuracy in noninverting configurations. Such applications include instrumentation amplifiers, where the increased open-loop gain maintains high linearity at high closed-loop gains.

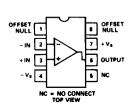
The AD OP-07 is available in five performance grades. The AD OP-07E, AD OP-07C and AD OP-07D are specified for operation over the 0 to +70°C temperature range, while the AD OP-07A and AD OP-07 are specified for -55°C to +125°C operation. All devices are available in either the TO-99 hermetically sealed metal cans or the hermetically sealed cerdip packages, while the industrial grades are also available in plastic 8-pin mini-DIPs, and plastic surface mount (SOIC).

AD OP-07 CONNECTION DIAGRAMS

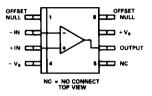
TO-99 (H) Package

Plastic Mini-DIP (N) Package and

and Cerdip (Q) Package



Small Outline (R) Package



PRODUCT HIGHLIGHTS

- Increased open-loop voltage gain (3.0 million, min) results in better accuracy and linearity in high closed-loop gain applications.
- Ultralow offset voltage and offset voltage drift, combined with low input bias currents, allow the AD OP-07 to maintain high accuracy over the entire operating temperature range.
- Internal frequency compensation, ultralow input offset voltage and full device protection eliminate the need for additional components. This reduces circuit size and complexity and increases reliability.
- 4. High input impedances, large common mode input voltage range and high common mode rejection ratio make the AD OP-07 ideal for noninverting and differential instrumentation applications.
- Monolithic construction along with advanced circuit design and processing techniques result in low cost.
- 6. The input offset voltage is trimmed at the wafer stage. Unmounted chips are available for hybrid circuit applications.

SPECIFICATIONS $(T_A = +25^{\circ}C, V_S = \pm 15V, \text{ unless otherwise specified})$

Model		AD OP-07E		AD OP-07C		AD OP-07D				
Parameter	Symbol	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max
OPEN LOOP GAIN	Avo	2,000 1,800 300	5,000 4,500 1,000		1,200 1,000 300	4,000 4,000 1,000		1,200 1,000 300	4,000 4,000 1,000	
OUTPUT CHARACTERISTICS Maximum Output Swing	V _{OM}	±12.5 ±12.0 ±10.5 ±12.0	± 13.0 ± 12.8 ± 12.0 ± 12.6		±12.0 ±11.5	+ 13.0 + 12.8 + 12.0 + 12.6		± 12.0 ± 11.5 + 11.0	± 13.0 ± 12.8 ± 12.6	
Open-Loop Output Resistance	R _O		60			60			60	
FREQUENCY RESPONSE Closed Loop Bandwidth Slew Rate	BW SR		0.6 0.17			0.6 0.17			0.6 0.17	
NPUT OFFSET VOLTAGE Initial Adjustment Range	V _{OS}		30 45 + 4	75 130	1	60 85 + 4	150 250		60 85 ± 4	150 250
Average Drift No External Trim With External Trim Long Term Stability	TCV _{OS} TCV _{OSN} V _{OS} /Time		0.3 0.3 0.3	1.3 1.3 1.5		0.5 0.4 0.4	1.8 1.6 2.0		0.7 0.7 0.5	2.5 2.5 3.0
INPUT OFFSET CURRENT Initial	I _{OS}		0.5 0.9	3.8 5.3		0.8 1.6	6.0 8.0		0.8 1.6	6.0 8.0
Average Drift	TClos		8	35		12	50		12	50
INPUT BIAS CURRENT Initial Average Drift	I _B TCI _B		+ 1.2 + 1.5	±4.0 •5.5		+ 1.8 + 2.2 18	±7.0 +9.0 50		+ 2.0 + 3.0 18	± 12 + 14 50
INPUT RESISTANCE Differential Common Mode	R _{IN} R _{INCM}	15	50 160		8	33 120		7	31 120	
NPUT NOISE Voltage Voltage Density Current Current Density	c _n p-p c _n i _n p-p i _n		0.35 10.3 10.0 9.6 14 0.32	0.6 18.0 13.0 11.0 30 0.80		0.38 10.5 10.2 9.8 15 0.35	0.65 20.0 13.5 11.5 35 0.90		0.38 10.5 10.2 9.8 15 0.35	0.65 20.0 13.5 11.5 35 0.90
			0.14 0.12	0.23 0.17		0.15 0.13	0.27 0.18		0.15 0.13	0.27
INPUT VOLTAGE RANGE Common Mode	CMVR	± 13.0 • 13.0	+ 14.0 + 13.5		± 13.0 + 13.0	+ 14.0 ± 13.5		± 13.0 + 13.0	+ 14.0	
Common-Mode Rejection Ratio	CMRR	106 103	123 123		100 97	120 120		94 94	110 106	
POWER SUPPLY Current, Quiescent Power Consumption	$egin{array}{c} I_Q \ P_D \end{array}$		3.0 90	4.0 120		3.5 105	5.0 150		3.5 105	5.0 150
Rejection Ratio	PSRR	94 90	6.0 107 104	9.0	90 86	6.0 104 100	9.0	90 86	6.0 104 100	9.0
OPERATING TEMPERATURE RANGE	T _{min} , T _{man}	0		+ 70	0		+ 70	0		+ 70
PACKAGE OPTIONS ¹ SOIC (R-8) Plastic Mini-DIP (N-8) Cerdip (Q-8) TO-99 (H-08A)		/	AD OP-07 AD OP-07 AD OP-07	EQ	1	AD OP-07 AD OP-07 AD OP-07 AD OP-07	CN CQ	,	AD OP-07 AD OP-07 AD OP-07	DQ

NOTES

*Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. Additionally, the AD OP-07A offset voltage is guaranteed fully warmed up.

*I.ong-Term Input Offset Voltage Stability refers to the averaged trend line of V_{ON} vs. Time over extended periods of time and is extrapolated from high temperature test data. Excluding the initial hour of operation, changes in V_{ON} during the first 30 operating days are typically 2.5 µV - Parameter is not 100% tested: 90% of units meet this specification.

See Section 20 for package outline information. Specifications subject to change without notice.

AD OP-07A		AD OP-07					
Min	Тур	Max	Min	Тур	Max	Test Conditions	Units
3,000 2,000 300	5,000 4,000 1,000		2,000 1,500 300	5,000 4,000 1,000		$\begin{aligned} &R_1 \geqslant 2k\Omega, V_O = \pm 10V \\ &R_1 \geqslant 2k\Omega, V_O = \pm 10V, T_{min} \text{ to } T_{max} \\ &R_1 = 500\Omega, V_O = \pm 0.5V, V_S = \pm 3V \end{aligned}$	V/mV V/mV V/mV
± 12.5 ± 12.0 ± 10.5 ± 12.0	± 13.0 ± 12.8 ± 12.0 ± 12.6		± 12.5 ± 12.0 ± 10.5 ± 12.0	± 13.0 ± 12.8 ± 12.0 ± 12.6 60		$\begin{aligned} R_{L} &\geqslant 10k\Omega \\ R_{L} &\geqslant 2k\Omega \\ R_{L} &\geqslant 1k\Omega \\ R_{L} &\geqslant 1k\Omega \\ R_{L} &\geqslant 2k\Omega, T_{min} \text{ to } T_{max} \\ V_{O} &= 0, I_{O} = 0 \end{aligned}$	ν ν ν ν
	0.6 0.17			0.6 0.17		$\mathbf{A}_{\mathbf{VCL}} = +1.0$ $\mathbf{R}_1 \geqslant 2\mathbf{k}$	MHz V/μs
	10 25 ±4	25 60 ¹		30 60 ± 4	75 200¹	Note 1 T_{min} to T_{max} $R_p = 20k\Omega$	μV μV mV
	0.2 0.2 0.2	0.6 0.6 1.0		0.3 0.3 0.2	1.3 1.3 1.0	T_{min} to T_{max} $R_P = 20k\Omega$, T_{min} to T_{max} Note 2	μV/°C μV/°C μV/Month
	0.3 0.8 5	2.0 4.0 25		0.4 1.2 8	2.8 5.6 50	T_{min} to T_{max} T_{min} to T_{max}	nA nA pA/^C
	± 0.7 ± 1.0 8	±2.0 ±4.0 25		± 1.0 ± 2.0 13	±3.0 ±6.0	T_{min} to T_{max} T_{min} to T_{max}	п А п А р А /°С
30	80 200		20	60 200			MΩ GΩ
	0.35 10.0 9.6 14 0.32 0.14 0.12	0.6 18.0 13.0 11.0 30 0.80 0.23 0.17		0.35 10.3 10.0 9.6 14 0.32 0.14 0.12	0.6 18.0 13.0 11.0 30 0.80 0.23 0.17	0.1Hz to 10Hz $f_{CD} = 10Hz$ $f_{CD} = 100Hz$ $f_{CD} = 1kHz$ $0.1Hz to 10Hz$ $f_{CD} = 10Hz$ $f_{CD} = 10Hz$ $f_{CD} = 1kHz$	µV p-p nV/√Hz nV/√Hz nV/√Hz pA p-p pA/√Hz pA/√Hz pA/√Hz
± 13.0 ± 13.0	± 14.0 ± 13.5		±13.0 ±13.0	± 14.0 ± 13.5		T _{mun} to T _{max}	v v
110 106	126 123		110 106	126 123		$V_{CM} = \pm CMVR$ $V_{CM} = \pm CMVR, T_{min} \text{ to } T_{max}$	dB dB
100 94	3.0 90 6.0 110 106	4.0 120 8.4	100 94	30 90 6.0 110 106	4.0 120 8.4	$\begin{split} &V_S \approx \pm 15V \\ &V_S \approx \pm 15V \\ &V_S \approx \pm 3V \\ &V_S \approx \pm 3V \\ &V_S \approx \pm 3V \text{ to } \pm 18V \\ &V_S \approx \pm 3V \text{ to } \pm 18V, T_{min} \text{ to } T_{max} \end{split}$	mA mW mW dB dB
- 55		+ 125	- 55		+ 125		℃
	AD OP-07 AD OP-07			AD OP-0 AD OP-0			

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

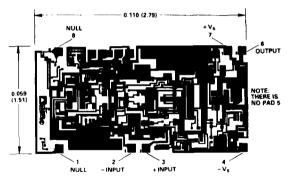
ABSOLUTE MAXIMUM RATINGS

TENOODO I DIVERSI INCO
Supply Voltage ± 22V
Internal Power Dissipation (Note 1) 500mW
Differential Input Voltage ± 30V
Input Voltage
Output Short Circuit Duration Indefinite
Storage Temperature Range65°C to +150°C
Operating Temperature Range
AD OP-07A, AD OP-0755°C to +125°C
AD OP-07E, AD OP-07C, AD OP-07D 0 to +70°C
Lead Temperature Range (Soldering 60sec) + 300°C
NOTE
Note 1: Maximum package power dissipation vs. ambient temperature. Maximum Ambient Derate Above Maximum
Package Type Temperature for Rating Ambient Temperature

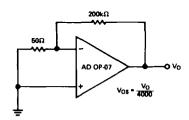
Package Type	Maximum Ambient Temperature for Rating	Derate Above Maximum Ambient Temperature		
TO-99(H)	80°C	7.1m₩/°C		
Mini-DIP(N)	36℃	5.6mW/°C		
Cerdip(Q)	75°C	6.7m\ W /°C		

CHIP DIMENSIONS AND BONDING DIAGRAM

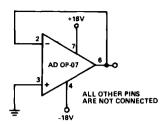
Contact factory for latest dimensions. Dimensions shown in inches and (mm).



THE AD OP 07 IS AVAILABLE IN WAFER-TRIMMED CHIP FORM FOR PRECISION HYBRIDS. CONSULT THE FACTORY FOR DETAILS.



Offset Voltage Test Circuit



Burn-In Circuit

AD OP-07 ORDERING GUIDE¹

Model	Package Options	Temperature Range (°C)	Max Initial Offset (μV)	Max Offset Drift (μV/°C)	
AD OP-07EH	TO-99	0 to + 70	75	1.3	
AD OP-07EN	Mini-DIP	0 to + 70	75	1.3	
AD OP-07EQ	Cerdip	0 to + 70	75	1.3	
AD OP-07CH	TO-99	0 to + 70	150	1.8	
AD OP-07CN	Mini-DIP	0 to + 70	150	1.8	
AD OP-07CQ	Cerdip	0 to + 70	150	1.8	
AD OP-07CR	SOIC	0 to + 70	150	1.8	
AD OP-07DH	TO-99	0 to +70	150	2.5	
AD OP-07DN	Mini-DIP	0 to + 70	150	2.5	
AD OP-07DQ	Cerdip	0 to + 70	150	2.5	
AD OP-07AH	TO-99	- 55 to + 125	25	0.6	
AD OP-07AQ	Cerdip	-55 to +125	25	0.6	
AD OP-07H	TO-99	- 55 to + 125	75	1.3	
AD OP-07Q	Cerdip	- 55 to + 125	75	1.3	

NOTE

A, C and D grade chips are also available. AD OP-07CR available in tape and reel.

Applying the AD OP-07

The AD OP-07 may be directly substituted for other OP-07's as well as 725, 108/208/308, 108A/208A/308A, 714, OP-05 or LM11 devices, with or without removal of external frequency compensation or offset nulling components. If used to replace 741 devices, offset nulling components must be re-

20kΩ +Vs
1 8 0.01μF
AD OP-07

RL

RL

Figure 1. Optional Offset Nulling Circuit and Power Supply Bypassing

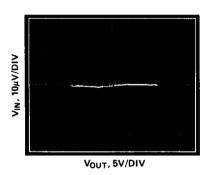
moved (or referenced to +V_S). Input offset voltage of the AD OP-07 is very low, but if additional nulling is required, the circuit shown in Figure 1 is recommended.

The AD OP-07 provides stable operation with load capacitances up to 500pF and $\pm 10V$ swings; larger capacitances should be decoupled with 50Ω resistor.

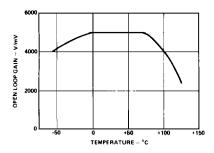
Stray thermoelectric voltages generated by dissimilar metals (thermocouples) at the contacts to the input terminals can prevent realization of the drift performance indicated. Best operation will be obtained when both input contacts are maintained at the same temperature, preferably close to the temperature of the device's package.

Although the AD OP-07 features high power supply rejection, the effects of noise on the power supplies may be minimized by bypassing the power supplies as close to pins 4 and 7 of the AD OP-07 as possible, to load ground with a good-quality $0.01\mu F$ ceramic capacitor as shown in Figure 1.

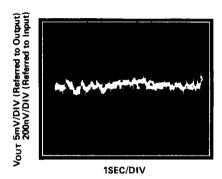
Performance Curves (typical @ $T_A = +25^{\circ}$ C, $V_S = \pm 15$ V, AD OP-07 Grade Device unless otherwise noted)



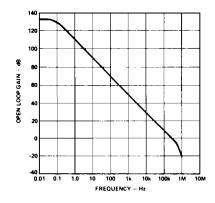
AD OP-07 Open-Loop Gain Curve



Open-Loop Gain vs. Temperature

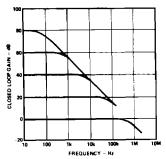


AD OP-07 Low Frequency Noise (See Test Circuit, on the Previous Page)

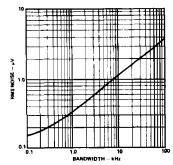


Open-Loop Frequency Response

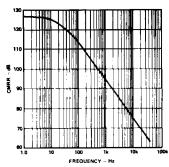
Typical Performance Curves



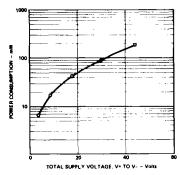
Closed-Loop Response for Various Gain Configurations



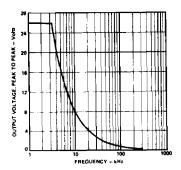
Input Wideband Noise vs. Bandwidth (0.1kHz to Frequency Indicated)



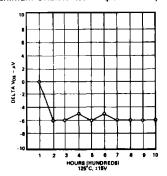
CMRR vs. Frequency



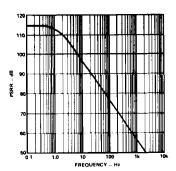
Power Consumption vs. Power Supply



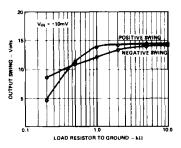
Maximum Undistorted Output vs. Frequency



Offset Voltage vs. Time



PSRR vs. Frequency



Output Voltage vs. Load Resistance