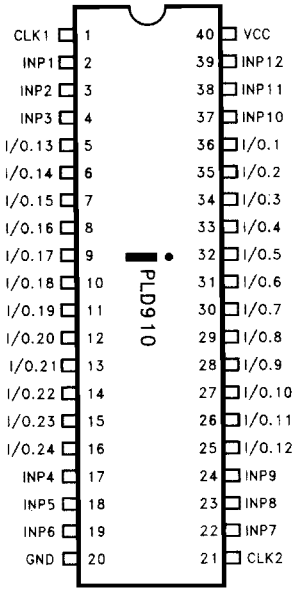
iPLD910
FAST 24-MACROCELL CMOS PLD

Function, Pin, and JEDEC Compatible with EP900, EP910, EP910A, 85C090 and 5C090

- t_{PD} 12 ns, 62.5 MHz w/Feedback, Clock to Output 8 ns
- I_{CC} = 150 mA Max @ 1 MHz
- Programmable Low-Power Option for "Standby" Operation; 60 μA Typ. in Standby Mode
- 24 Macrocells with Programmable I/O Architecture (Register/Combinatorial). Registers Configurable as D/T/JK/RS Types
- Up to 36 Inputs (12 Dedicated and 24 I/O)
- 8 P-terms, Selectable SOP Invert, Clear and OE P-terms for Each Macrocell
- Programmable Clock System with 2 Synchronous Clocks and Asynchronous Clocking Option on all Macrocells
- Extensive Software and Programming Support via Intel and Third-Party Tools
- 1-Micron CMOS IIIE* EPROM Technology
- Programmable Security Bit Allows Total Protection of Proprietary Designs
- 100% Generically Tested Logic Array
- Available in 40-Pin PDIP, CERDIP and 44-Pin PLCC Packages

(See Packaging Spec., Order Number 240800, Package Type N and P)



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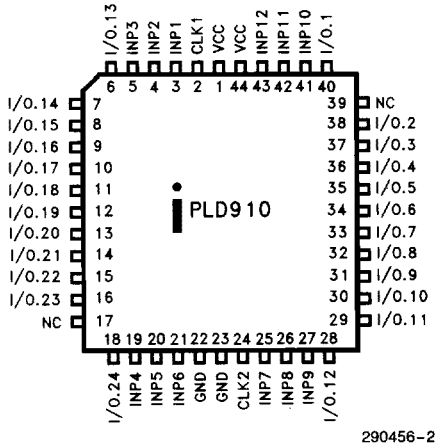

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Figure 1. iPLD910 Pinout Diagrams

*CMOS is a patented process of Intel Corporation.

Refer to the 1994 Programmable Logic Handbook for the complete data sheet on this device.

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